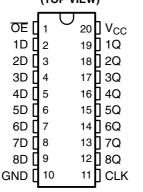
SN54LV574A, SN74LV574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

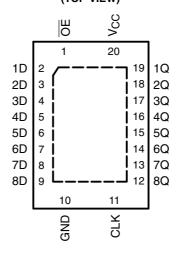
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- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 10 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 >2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

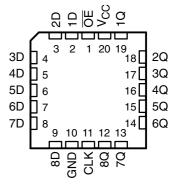
SN54LV574A . . . J OR W PACKAGE SN74LV574A . . . DB, DGV, DW, NS, OR PW PACKAGE (TOP VIEW)



SN74LV574A . . . RGY PACKAGE (TOP VIEW)



SN54LV574A . . . FK PACKAGE (TOP VIEW)



description/ordering information

ORDERING INFORMATION

T _A	PACKA	GE [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	QFN – RGY	Reel of 1000	SN74LV574ARGYR	LV574A
	0010 DW	Tube of 25	SN74LV574ADW	11/5744
	SOIC - DW	Reel of 2000	SN74LV574ADWR	LV574A
	SOP - NS	Reel of 2000	SN74LV574ANSR	74LV574A
4000 +- 0500	SSOP – DB	Reel of 2000	SN74LV574ADBR	LV574A
-40°C to 85°C		Tube of 70	SN74LV574APW	
	TSSOP - PW	Reel of 2000	SN74LV574APWR	LV574A
		Reel of 250	SN74LV574APWT	
	TVSOP - DGV	Reel of 2000	SN74LV574ADGVR	LV574A
	VFBGA – GQN	Reel of 1000	SN74LV574AGQNR	LV574A
CDIP – J		Tube of 20	SNJ54LV574AJ	SNJ54LV574AJ
-55°C to 125°C		Tube of 85	SNJ54LV574AW	SNJ54LV574AW
	LCCC – FK	Tube of 55	SNJ54LV574AFK	SNJ54LV574AFK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



SN54LV574A, SN74LV574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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description/ordering information (continued)

The 'LV574A devices are octal edge-triggered D-type flip-flops designed for 2-V to 5.5-V V_{CC} operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

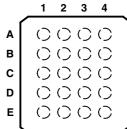
A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

GQN PACKAGE (TOP VIEW)



terminal assignments

	1	2	3	4
Α	1D	ŌĒ	V_{CC}	1Q
В	3D	3Q	2D	2Q
С	5D	4D	5Q	4Q
D	7D	7Q	6D	6Q
Ε	GND	8D	CLK	8Q

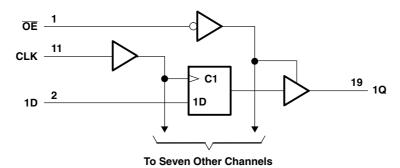
FUNCTION TABLE (each flip-flop)

	INPUTS		OUTPUT
ŌΕ	CLK	D	Q
L	1	Н	Н
L	\uparrow	L	L
L	H or L	Χ	Q_0
Н	X	Χ	Z



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logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, FK, J, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V to 7 V
)	
Voltage range applied to any output	t in the high-impedance	
or power-off state, V _O (see Note	1)	–0.5 V to 7 V
Output voltage range applied in the	high or low state, V _O (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$)		–20 mA
Output clamp current, I _{OK} (V _O < 0)		–50 mA
Continuous output current, IO (VO =	= 0 to V _{CC})	±35 mA
Continuous current through V _{CC} or	GND	±70 mA
Package thermal impedance, θ _{JA} (s	see Note 3): DB package	70°C/W
(5	see Note 3): DGV package	92°C/W
(s	see Note 3): DW package	58°C/W
(s	see Note 3): GQN package	78°C/W
(s	see Note 3): NS package	60°C/W
(s	see Note 3): PW package	83°C/W
(s	see Note 4): RGY package	37°C/W
Storage temperature range, T _{sta} .		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. This value is limited to 5.5 V maximum.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.
- 4. The package thermal impedance is calculated in accordance with JESD 51-5.



SN54LV574A, SN74LV574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 5)

			SN54L	V574A	SN74L	/574A	
			MIN	MAX	MIN	MAX	UNIT
V _{CC}	Supply voltage		2	5.5	2	5.5	V
		V _{CC} = 2 V	1.5		1.5		
١.,		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$.,
V _{IH}	High-level input voltage	V _{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V _{CC} = 2 V		0.5		0.5	
١.,		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$.,
V_{IL}	Low-level input voltage	V _{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
VI	Input voltage		0	5.5	0	5.5	V
.,	O "	High or low state	0	V _{CC}	0	V _{CC}	.,
Vo	Output voltage	3-state	0	5.5	0	5.5	V
		V _{CC} = 2 V		-50		-50	μА
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	3	-2		-2	
I _{OH}	High-level output current	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	0	-8		-8	mA
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	Q	-16		-16	
		V _{CC} = 2 V		50		50	μА
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		2		2	
l _{OL}	Low-level output current	V _{CC} = 3 V to 3.6 V		8		8	mA
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		16		16	
		V _{CC} = 2.3 V to 2.7 V		200		200	
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		100		100	ns/V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		20		20	
T _A	Operating free-air temperature	•	-55	125	-40	85	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMPITIONS	.,	SN54L	V574A	SN7	4LV574A	
PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP MA	X MIN	TYP MAX	UNIT
	$I_{OH} = -50 \mu\text{A}$	2 V to 5.5 V	V _{CC} -0.1		V _{CC} -0.1		
.,	$I_{OH} = -2 \text{ mA}$	2.3 V	2		2] ,
V _{OH}	$I_{OH} = -8 \text{ mA}$	3 V	2.48		2.48		V
	$I_{OH} = -16 \text{ mA}$	4.5 V	3.8	N	3.8		
	$I_{OL} = 50 \mu A$	2 V to 5.5 V		0	1	0.1	
.,,	I _{OL} = 2 mA	2.3 V		0	4	0.4	V
V _{OL}	I _{OL} = 8 mA	3 V	6	0.4	4	0.44]
	I _{OL} = 16 mA	4.5 V	770	0.5	5	0.55	
II	V _I = 5.5 V or GND	0 to 5.5 V	06	<u>+</u>	1	±1	μΑ
l _{OZ}	V _O = V _{CC} or GND	5.5 V	Q.	<u>±</u>	5	±5	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		2	0	20	μΑ
l _{off}	V_{I} or $V_{O} = 0$ to 5.5 V	0			5	5	μΑ
C _i	V _I = V _{CC} or GND	3.3 V		1.8		1.8	pF

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V \pm 0.2 V (unless otherwise noted) (see Figure 1)

	PARAMETER			25°C	SN54LV574A		SN74LV574A		
	PARAMETER		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t _w	Pulse duration	CLK high or low	7		7	100	7		ns
t _{su}	Setup time	High or low before CLK↑	5.5		5.5	JIP.	5.5		ns
t _h	Hold time	Data after CLK↑	2		2		2		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

	DADAMETED		T _A = 25°C S		SN54LV574A		SN74LV574A		LINUT
	PARAMETER		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t _w	Pulse duration	CLK high or low	5		5	10,01	5		ns
t _{su}	Setup time	High or low before CLK↑	3.5		3.5	11/2	3.5		ns
t _h	Hold time	Data after CLK↑	1.5		1.5		1.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

	DADAMETED		T _A = 2	25°C	SN54L	SN54LV574A SN74LV574A			LINIT
	PARAMETER		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t _w	Pulse duration	CLK high or low	5		5	10,01	5		ns
t _{su}	Setup time	High or low before CLK↑	3.5		3.5	11/2	3.5		ns
t _h	Hold time	Data after CLK↑	1.5		1.5		1.5		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V \pm 0.2 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	LOAD	T,	գ = 25°C	;	SN54L\	/574A	SN74LV574A		
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			C _L = 15 pF	60*	100*		50*		50		N 41 1-
f _{max}			C _L = 50 pF	50	85		40	N	40		MHz
t _{pd}	CLK	Q			9.6*	16.6*	1*	20*	1	20	
t _{en}	ŌĒ	Q	C _L = 15 pF		9.2*	16.1*	1* 2	19*	1	19	ns
t _{dis}	ŌĒ	Q			6.5*	12.8*	15	15*	1	15	
t _{pd}	CLK	Q			11.6	19.6	$ \sqrt{Q} $	23	1	23	
t _{en}	ŌĒ	Q	0 50 5		10.9	19	ر الا	22	1	22	
t _{dis}	ŌĒ	Q	$C_L = 50 pF$		8.4	17.5	1	20	1	20	ns
t _{sk(o)}						2				2	

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.



SN54LV574A, SN74LV574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	TO LOAD		T,	_A = 25°C	;	SN54L	V574A	SN74L	/574A	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			C _L = 15 pF	80*	145*		65*		65		N 41 1-
f _{max}			C _L = 50 pF	50	120		45	2	45		MHz
t _{pd}	CLK	Q			6.8*	13.2*	1*	15.5*	1	15.5	
t _{en}	ŌĒ	Q	C _L = 15 pF		6.4*	12.8*	1*	15*	1	15	ns
t _{dis}	ŌĒ	Q			4.8*	13*	1*	15*	1	15	
t _{pd}	CLK	Q			8.1	16.7	27/2	19	1	19	
t _{en}	ŌĒ	Q	0 50 5		7.7	16.3	0 1	18.5	1	18.5	
t _{dis}	ŌĒ	Q	$C_L = 50 pF$		6.1	15	Q 1	17	1	17	ns
t _{sk(o)}						1.5				1.5	

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

242445752	FROM	то	LOAD	T,	_A = 25°C	;	SN54L	V574A	SN74LV574A		
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			C _L = 15 pF	130*	205*		110*		110		
f _{max}			C _L = 50 pF	85	175		75		75		MHz
t _{pd}	CLK	Q			4.8*	8.6*	1*	10*	1	10	
t _{en}	ŌĒ	Q	C _L = 15 pF		4.6*	9*	1*	10.5*	1	10.5	ns
t _{dis}	ŌĒ	Q	1		3.5*	9*	1*	10.5*	1	10.5	
t _{pd}	CLK	Q			5.7	10.6	2	12	1	12	
t _{en}	ŌĒ	Q] [5.5	11	01	12.5	1	12.5	
t _{dis}	ŌĒ	Q	$C_L = 50 \text{ pF}$		4.1	10.1	Q 1	11.5	1	11.5	ns
t _{sk(o)}			1			1				1	

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

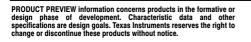
noise characteristics, $V_{CC} = 3.3 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^{\circ}\text{C}$ (see Note 6)

	DADAMETED	SN			
	PARAMETER	MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.7	8.0	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.6	-0.8	V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		2.8		V
V _{IH(D)}	High-level dynamic input voltage	2.31			V
V _{IL(D)}	Low-level dynamic input voltage			0.99	V

NOTE 6: Characteristics are for surface-mount packages only.

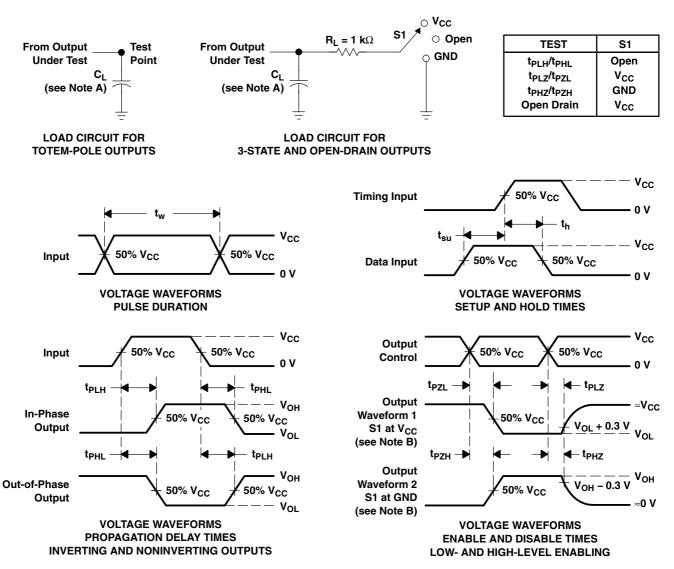
operating characteristics, T_A = 25°C

	PARAMETER	TEST CO	NDITIONS	v_{cc}	TYP	UNIT	
<u> </u>	Power dissination conscitance	Outputs enabled	C ₁ = 50 pF.	f = 10 MHz	3.3 V	20.4	pF
Opd	Power dissipation capacitance	Outputs enabled	$C_L = 50 \text{ pF},$	I = IU IVIIIZ	5 V	23.8	pΓ





PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 3 ns, $t_f \leq$ 3 ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZI} and t_{PZH} are the same as t_{en}.
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LV574ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574ADGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574ADGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574ADGVRG4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	





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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LV574APWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574APWTE4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574APWTG4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LV574ARGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN74LV574ARGYRG4	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN74LV574AZQNR	ACTIVE	BGA MICROSTAR JUNIOR	ZQN	20	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

20-Aug-2011

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV574ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV574ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV574ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LV574ANSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74LV574APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LV574APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LV574ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
SN74LV574AZQNR	BGA MI CROSTA R JUNI OR	ZQN	20	1000	330.0	12.4	3.3	4.3	1.5	8.0	12.0	Q1

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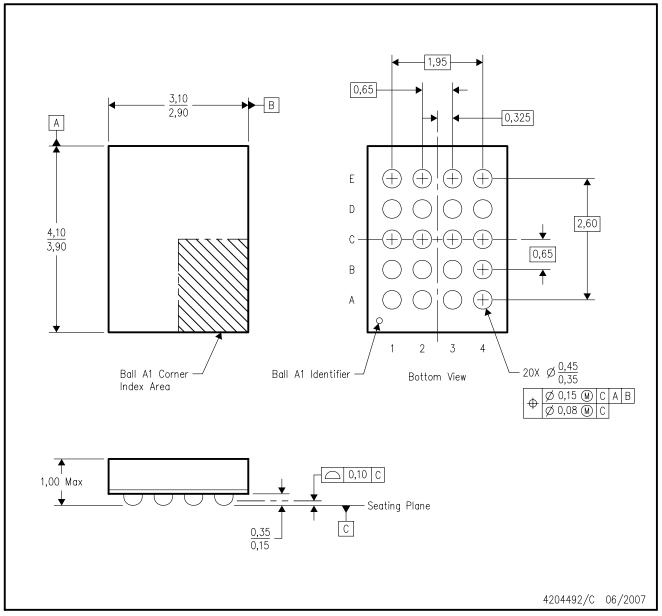


*All dimensions are nominal

All difficultions are florilliar							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV574ADBR	SSOP	DB	20	2000	346.0	346.0	33.0
SN74LV574ADGVR	TVSOP	DGV	20	2000	346.0	346.0	29.0
SN74LV574ADWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74LV574ANSR	SO	NS	20	2000	346.0	346.0	41.0
SN74LV574APWR	TSSOP	PW	20	2000	346.0	346.0	33.0
SN74LV574APWT	TSSOP	PW	20	250	346.0	346.0	33.0
SN74LV574ARGYR	VQFN	RGY	20	3000	346.0	346.0	29.0
SN74LV574AZQNR	BGA MICROSTAR JUNIOR	ZQN	20	1000	340.5	338.1	20.6

ZQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BC-2.
- D. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).



DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194 DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153





NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.



RGY (R-PVQFN-N20)

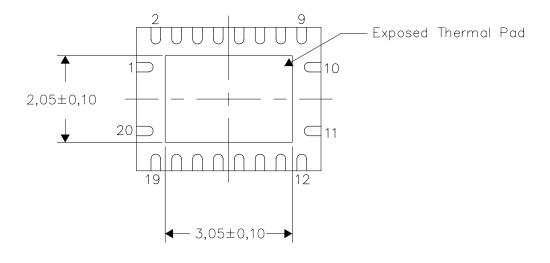
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

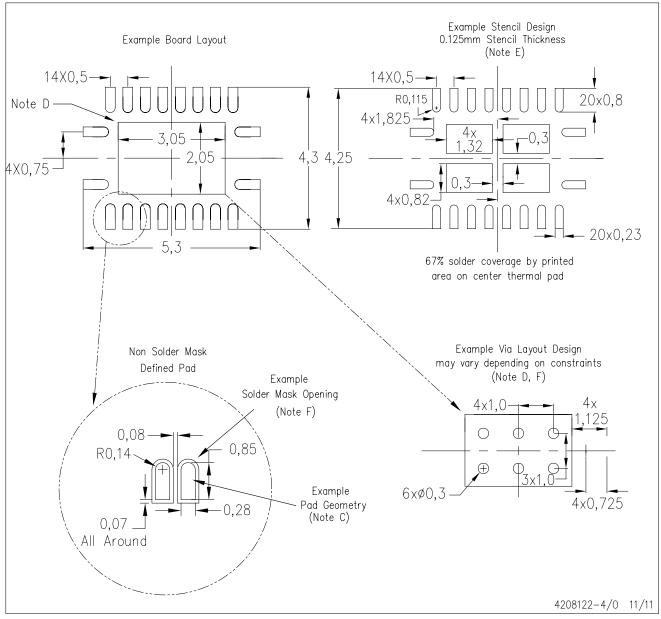
4206353-4/0 11/11

NOTE: All linear dimensions are in millimeters



RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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