## CD74AC175 QUADRUPLE D-TYPE FLIP-FLOP WITH CLEAR

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- AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply Voltage
- Buffered Inputs
- Contains Four Flip-Flops With Double-Rail Outputs
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- ±24-mA Output Drive Current
  - Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

#### **M PACKAGE** (TOP VIEW) CLR [ 16 V<sub>CC</sub> 1Q [ 2 15 4Q 1<u>Q</u> ∏ 3 14 ¶ 4Q 13**∏** 4D 1D 4 2D Π 5 12 3D 11 3Q $2\overline{Q}$ 6 10 T 3Q 2Q [ GND [ 8 9 CLK

### description/ordering information

This positive-edge-triggered D-type flip-flop has a direct clear ( $\overline{\text{CLR}}$ ) input. The CD74AC175 features complementary outputs from each flip-flop.

Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

#### ORDERING INFORMATION

TA	PACKA	GEŤ	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
–55°C to 125°C	SOIC – M	Tube	CD74AC175M	AC175M	
-55 C to 125 C	SOIC - IVI	Tape and reel	CD74AC175M96	AC175W	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

# FUNCTION TABLE (each flip-flop)

INPUTS OUTPUTS			PUTS	
CLR	CLK	D	Q	Q
L	Х	Χ	L	Н
Н	$\uparrow$	Н	Н	L
Н	$\uparrow$	L	L	Н
Н	L	Χ	Q <sub>0</sub>	$\overline{Q}_0$

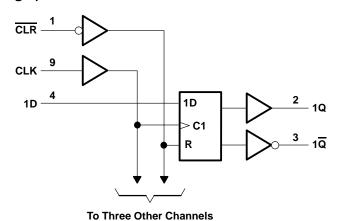


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### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 6 V
Input clamp current, $I_{IK}$ ( $V_I < 0 \text{ V or } V_I > V_{CC}$ ) (see Note 1)	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 V or V <sub>O</sub> > V <sub>CC</sub> ) (see Note 1)	±50 mA
Continuous output current, $I_O$ ( $V_O > 0$ V or $V_O < V_{CC}$ )	±50 mA
Continuous current through V <sub>CC</sub> or GND	±200 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2)	
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

			T <sub>A</sub> = 25°C		–55°C to 125°C		–40°C to 85°C		UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
Vcc	Supply voltage		1.5	5.5	1.5	5.5	1.5	5.5	V	
		V <sub>CC</sub> = 1.5 V	1.2		1.2		1.2			
$V_{IH}$	High-level input voltage	VCC = 3 V	2.1		2.1		2.1		V	
		V <sub>CC</sub> = 5.5 V	3.85		3.85		3.85			
		V <sub>CC</sub> = 1.5 V		0.3		0.3		0.3		
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V		0.9		0.9		0.9	V	
		V <sub>CC</sub> = 5.5 V		1.65		1.65		1.65		
٧ <sub>I</sub>	Input voltage		0	VCC	0	Vcc	0	VCC	V	
٧o	Output voltage		0	VCC	0	Vcc	0	VCC	V	
ІОН	High-level output current	V <sub>CC</sub> = 4.5 V to 5.5 V		-24		-24		-24	mA	
loL	Low-level output current	V <sub>CC</sub> = 4.5 V to 5.5 V		24		24		24	mA	
A+/A	lanut transition rise or fall rate	V <sub>CC</sub> = 1.5 V to 3 V		50		50		50	20/1	
Δt/Δv	Input transition rise or fall rate	$V_{CC} = 3.6 \text{ V to } 5.5 \text{ V}$		20		20		20	ns/V	

NOTE 3: All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		Vcc	T <sub>A</sub> = 25°C		–55°C to 125°C		–40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
			1.5 V	1.4		1.4		1.4		
		I <sub>OH</sub> = -50 μA	3 V	2.9		2.9		2.9		
			4.5 V	4.4		4.4		4.4		
Voн	$V_I = V_{IH}$ or $V_{IL}$	$I_{OH} = -4 \text{ mA}$	3 V	2.58		2.4		2.48		V
		$I_{OH} = -24 \text{ mA}$	4.5 V	3.94		3.7		3.8		
		$I_{OH} = -50 \text{ mA}^{\dagger}$	5.5 V			3.85				
		$I_{OH} = -75 \text{ mA}^{\dagger}$	5.5 V					3.85		
			1.5 V		0.1		0.1		0.1	
		$I_{OL} = 50  \mu A$	3 V		0.1		0.1		0.1	
			4.5 V		0.1		0.1		0.1	
VOL	$V_I = V_{IH}$ or $V_{IL}$	I <sub>OL</sub> = 12 mA	3 V		0.36		0.5		0.44	V
		I <sub>OL</sub> = 24 mA	4.5 V		0.36		0.5		0.44	
		$I_{OL} = 50 \text{ mA}^{\dagger}$	5.5 V				1.65			
		$I_{OL} = 75 \text{ mA}^{\dagger}$	5.5 V						1.65	
lį	V <sub>I</sub> = V <sub>CC</sub> or GND		5.5 V		±0.1		±1		±1	μΑ
Icc	$V_I = V_{CC}$ or GND,	IO = 0	5.5 V		8		160		80	μΑ
C <sub>i</sub>					10		10		10	pF

<sup>†</sup> Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

# timing requirements over recommended operating free-air temperature range, $V_{CC} = 1.5 \text{ V}$ (unless otherwise noted)

			−55° 125		–40°C to 85°C		UNIT	
			MIN	MAX	MIN	MAX		
fclock	Clock frequency			8		9	MHz	
	, Pulse duration	CLR low	50		44		no.	
t <sub>W</sub>		CLK high or low	63		55		ns	
t <sub>su</sub>	Setup time before CLK↑	Data	2		2		ns	
th	Hold time, data after CLK↑		2		2		ns	
t <sub>rec</sub>	Recovery time, before CLK↑	CLR↑	1		1		ns	

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# timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted)

			–55° 125		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
fclock	Clock frequency			71		81	MHz
	W Pulse duration	CLR low	5.6		4.9		no
t <sub>W</sub>		CLK high or low	7		6.1		ns
t <sub>su</sub>	Setup time before CLK↑	Data	2		2		ns
th	Hold time, data after CLK↑		2		2		ns
t <sub>rec</sub>	Recovery time, before CLK↑	CLR↑	1		1		ns

# timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted)

				–55°C to 125°C		–40°C to 85°C	
			MIN	MAX	MIN	MAX	
fclock	Clock frequency			100		114	MHz
	Pulse duration	CLR low	4		3.5		20
t <sub>W</sub>	ruise duration	CLK high or low	5		4.4		ns
t <sub>su</sub>	Setup time before CLK↑	Data	2		2		ns
th	Hold time, data after CLK↑		2	·	2		ns
t <sub>rec</sub>	Recovery time, before CLK↑	CLR↑	1		1		ns

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 1.5 V, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°( 125		–40°C to 85°C		UNIT
	(111 01)	(6611 61)	MIN	MAX	MIN	MAX	
f <sub>max</sub>			8		9		MHz
<sup>t</sup> PLH	CLK	Any Q		153		139	20
<sup>t</sup> PHL	CLK			153		139	ns
<sup>t</sup> PLH	CLR	Any Q		153		139	nc
t <sub>PHL</sub>	CLR	Any Q		153		139	ns

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°C to 125°C		–40°C to 85°C		UNIT
	(1141 01)	(6611 61)	MIN MAX MIN MAX   71 81 M   4.3 17.1 4.4 15.5				
f <sub>max</sub>			71		81		MHz
<sup>t</sup> PLH	CLK	Any Q	4.3	17.1	4.4	15.5	no
<sup>t</sup> PHL	CLK	Ally Q	4.3	17.1	4.4	15.5	ns
<sup>t</sup> PLH	CLR	Any Q	4.3	17.1	4.4	15.5	nc
<sup>t</sup> PHL	CLR	Ally Q	4.3	17.1	4.4	15.5	ns



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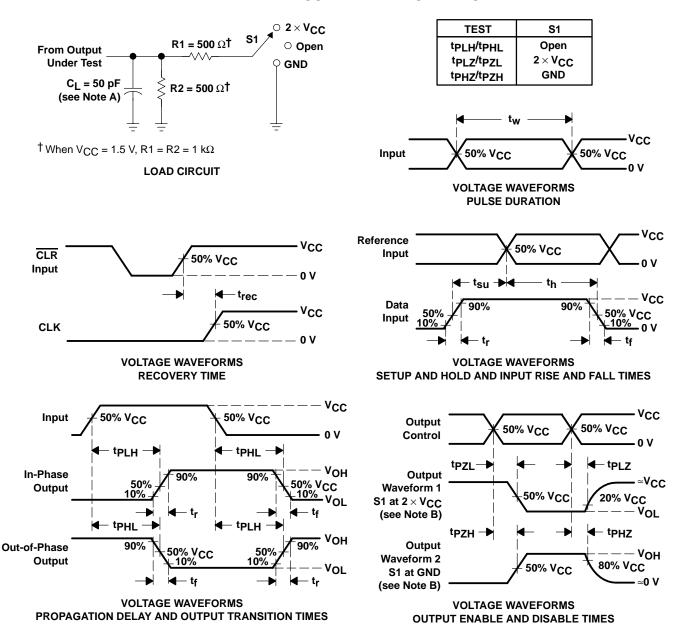
# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°( 125		–40°0 85°		UNIT
	(111 01)	(6611 61)	MIN	MAX	MIN	MAX	
f <sub>max</sub>			100		114		MHz
<sup>t</sup> PLH	CLK	Any Q	3.1	12.2	3.2	11.1	ns
<sup>t</sup> PHL	CLK	Ally Q	3.1	12.2	3.2	11.1	115
<sup>t</sup> PLH	CLR	Any Q	3.1	12.2	3.2	11.1	ns
<sup>t</sup> PHL	CLR	Ally Q	3.1	12.2	3.2	11.1	115

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

	PARAMETER	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	55	pF

### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>L</sub> includes probe and test-fixture capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \ \Omega$ ,  $t_f = 3 \ ns$ ,  $t_f = 3 \ ns$ . Phase relationships between waveforms are arbitrary.
  - D. For clock inputs, f<sub>max</sub> is measured with the input duty cycle at 50%.
  - E. The outputs are measured one at a time with one input transition per measurement.
  - F. tpLH and tpHL are the same as tpd.
  - G. tpzL and tpzH are the same as ten.
  - H. tpLZ and tpHZ are the same as tdis.
  - I. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms







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### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
CD74AC175M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74AC175M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74AC175M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74AC175M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74AC175ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74AC175MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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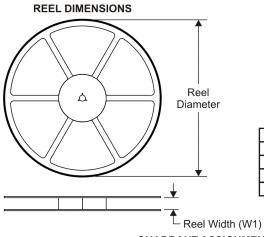
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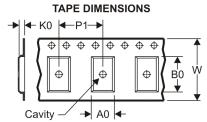
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## PACKAGE MATERIALS INFORMATION

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### TAPE AND REEL INFORMATION





Α0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



### \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC175M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

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### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC175M96	SOIC	D	16	2500	333.2	345.9	28.6

## D (R-PDS0-G16)

### PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



## D (R-PDSO-G16)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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