	SN74F574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS SDFS005A – D3034, SEPTEMBER 1987 – REVISED OCTOBER 1993
ngle	DW OR N PACKAGE (TOP VIEW)
uts	

1D 🛛 2

2D || 3

3D 4

4D 5

5D 6

7D 8

8D 9

GND 10

7

6D ||

19 1Q

18 2Q

17 3Q

16 4Q

15 5Q

14 6Q

13 7Q

12 8Q

11 CLK

- Eight D-Type Flip-Flops in a Sin Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Package Options Include Plastic **Small-Outline Packages and Standard Plastic 300-mil DIPs**

description

This 8-bit flip-flop features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the SN74F574 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs will be set to the logic levels that were set up at the data (D) inputs.

A buffered output enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output enable (\overline{OE}) does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74F574 is characterized for operation from 0°C to 70°C.

(odon mp nop)										
	INPUTS	OUTPUT								
OE	CLK	D	Q							
L	\uparrow	Н	Н							
L	\uparrow	L	L							
L	L	Х	Q ₀ Z							
н	Х	Х	Z							

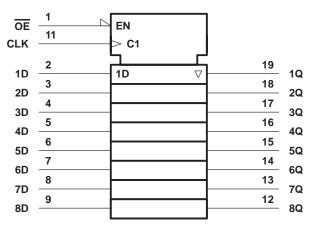
FUNCTION TABLE (each flip-flop)

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

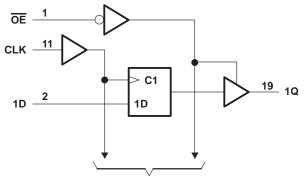
SN74F574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SDFS005A - D3034, SEPTEMBER 1987 - REVISED OCTOBER 1993

logic symbol[†]



logic diagram (positive logic)



To Seven Other Channels

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage range, V _{CC} Input voltage range, V _I (see Note 1)	
Input current range	
Voltage range applied to any output in the disabled or power-off state	
Voltage range applied to any output in the high state	
Current into any output in the low state	
Operating free-air temperature range	
Storage temperature range	

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	V
VIH	High-level input voltage	2			V
VIL	Low-level input voltage			0.8	V
IIК	Input clamp current			- 18	mA
IOH	High-level output current			- 3	mA
I _{OL}	Low-level output current			24	mA
TA	Operating free-air temperature	0		70	°C



SN74F574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS SDFS005A – D3034, SEPTEMBER 1987 – REVISED OCTOBER 1993

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	Т	TEST CONDITIONS				
VIK	V _{CC} = 4.5 V,	l _l = – 18 mA			- 1.2	V
	V _{CC} = 4.5 V	I _{OH} = – 1 mA	2.5	3.4		
VOH	VCC = 4.5 V	I _{OH} = – 3 mA	2.4	3.3		V
	V _{CC} = 4.75 V,	$I_{OH} = -1 \text{ mA to} - 3 \text{ mA}$	2.7			
VOL	V _{CC} = 4.5 V,	I _{OL} = 24 mA		0.35	0.5	V
IOZH	V _{CC} = 5.5 V,	V _O = 2.7 V			50	μΑ
IOZL	V _{CC} = 5.5 V,	$V_{O} = 0.5 V$			-50	μΑ
lj	V _{CC} = 5.5 V,	$V_{I} = 7 V$			0.1	mA
Iн	V _{CC} = 5.5 V,	V _I = 2.7 V			20	μΑ
۱ _{IL}	V _{CC} = 5.5 V,	V _I = 0.5 V			- 0.6	mA
IOS‡	V _{CC} = 5.5 V,	$V_{O} = 0$	- 60		- 150	mA
Iccz	V _{CC} = 5.5 V,	See Note 2		55	86	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$. [‡] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: I_{CCZ} is measured with \overline{OE} at 4.5 V and all other inputs grounded.

timing requirements

			V _{CC} =	= 5 V, 25°C	V _{CC} = 4.5 T _A = MIN t	UNIT	
			MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	100	0	100	MHz
+	Pulse duration	CLK high	7		7		20
t _W		CLK low	6		6		ns
		Data high	2		2		
t _{su}	Setup time before CLK [↑]	Data low	2		2		ns
+.	Hold time after CLK↑	Data high	2		2		20
th	Data low				2		ns

switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CL RL	c = 5 V, = 50 pF = 500 Ω = 25°C	,	V _{CC} = 4.5 C _L = 50 pl R _L = 500 Ω T _A = MIN 1	2,	UNIT
			MIN	TYP	MAX	MIN	MAX	
f _{max}			100			100		MHz
tPLH	CLK	Any Q	3.2	6.1	8.5	3.2	10	ns
^t PHL	OLK	Ally Q	3.2	6.1	8.5	3.2	10	115
^t PZH	ŌĒ	Any Q	1.2	8.6	11.5	1.2	12.5	ns
t _{PZL}	UE	Ally Q	1.2	4.9	7.5	1.2	8.5	115
^t PHZ	ŌĒ	Any Q	1.2	4.9	7	1.2	8	ns
^t PLZ	UL UL		1.2	3.9	5.5	1.2	6.5	115

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74F574DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F574DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F574DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F574DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F574DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F574DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F574N	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74F574NE4	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74F574NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F574NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74F574NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered

at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE OPTION ADDENDUM

18-Sep-2008

to Customer on an annual basis.

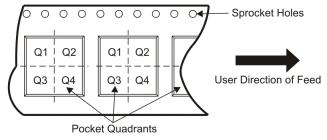
TEXAS INSTRUMENTS www.ti.com

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

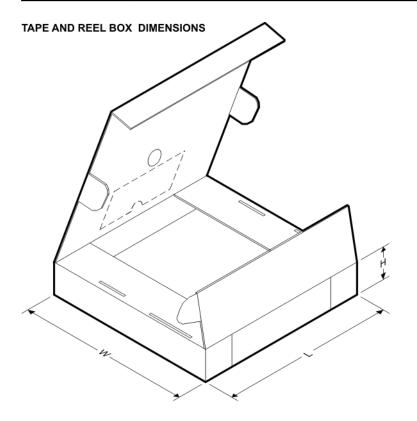


*All dimensions are nominal												
Device	-	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F574DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74F574NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1



PACKAGE MATERIALS INFORMATION

5-Aug-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F574DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74F574NSR	SO	NS	20	2000	346.0	346.0	41.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

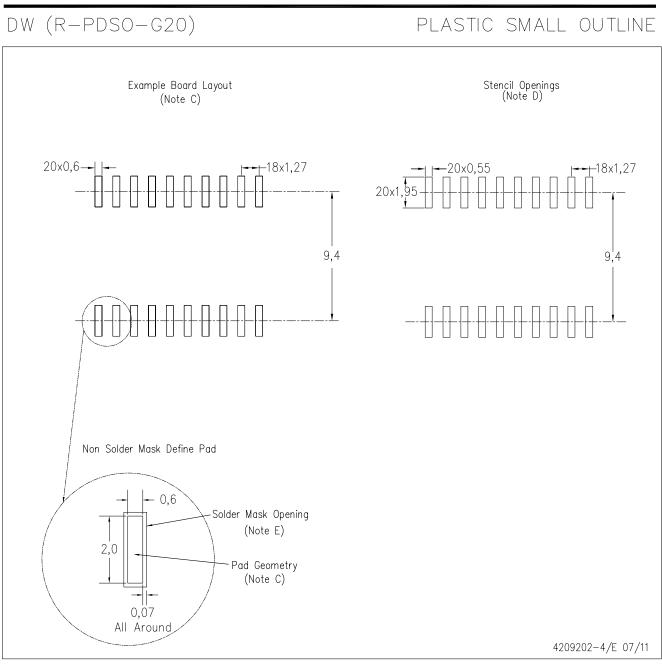
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AC.



LAND PATTERN DATA



NOTES:

A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0-10 Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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