

Data sheet acquired from Harris Semiconductor SCHS134E

February 1998 - Revised September 2003

#### Features

- Hysteresis on Clock Inputs for Improved Noise
  Immunity and Increased Input Rise and Fall Times
- Asynchronous Reset
- Complementary Outputs
- Buffered Inputs
- Typical f<sub>MAX</sub> = 60MHz at V<sub>CC</sub> = 5V, C<sub>L</sub> = 15pF, T<sub>A</sub> = 25<sup>o</sup>C
- Fanout (Over Temperature Range)
  - Standard Outputs ..... 10 LSTTL Loads
  - Bus Driver Outputs ..... 15 LSTTL Loads
- Wide Operating Temperature Range ... -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity: N<sub>IL</sub> = 30%, N<sub>IH</sub> = 30% of V<sub>CC</sub> at V<sub>CC</sub> = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility, V<sub>IL</sub>= 0.8V (Max), V<sub>IH</sub> = 2V (Min)
  - CMOS Input Compatibility, II  $\leq$  1µA at VOL, VOH

# CD54HC73, CD74HC73, CD74HCT73

## Dual J-K Flip-Flop with Reset Negative-Edge Trigger

#### Description

The 'HC73 and CD74HCT73 utilize silicon gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL loads.

These flip-flops have independent J, K, Reset and Clock inputs and Q and  $\overline{Q}$  outputs. They change state on the negative-going transition of the clock pulse. Reset is accomplished asynchronously by a low level input. This device is functionally identical to the HC/HCT107 but differs in terminal assignment and in some parametric limits.

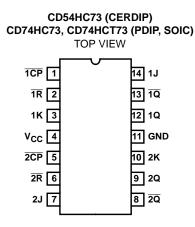
The HCT logic family is functionally as well as pin compatible with the standard LS logic family.

#### Ordering Information

PART NUMBER	TEMP. RANGE ( <sup>O</sup> C)	PACKAGE
CD54HC73F3A	-55 to 125	14 Ld CERDIP
CD74HC73E	-55 to 125	14 Ld PDIP
CD74HC73M	-55 to 125	14 Ld SOIC
CD74HC73MT	-55 to 125	14 Ld SOIC
CD74HC73M96	-55 to 125	14 Ld SOIC
CD74HCT73E	-55 to 125	14 Ld PDIP
CD74HCT73M	-55 to 125	14 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

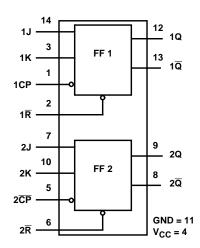
#### Pinout



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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## Functional Diagram



#### TRUTH TABLE

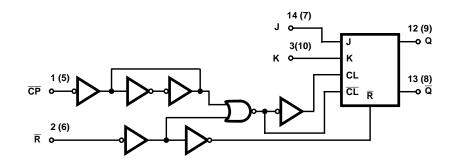
	INP	OUTPUTS					
R	CP	J	к	Q	Q		
L	Х	Х	Х	L H			
н	$\downarrow$	L	L	No Change			
Н	$\downarrow$	Н	L	Н	L		
н	$\downarrow$	L	Н	L H			
н	$\downarrow$	н	Н	Toggle			
н	Н	Х	Х	No Change			

H =High Level (Steady State) L =Low Level (Steady State)

X = Irrelevant

= High-to-Low Transition  $\downarrow$ 

## Logic Diagram



#### **Absolute Maximum Ratings**

DC Supply Voltage, V <sub>CC</sub>
For $V_{l} < -0.5V$ or $V_{l} > V_{CC} + 0.5V$ ±20mA
DC Drain Current, per Output, I <sub>O</sub>
For -0.5V < V <sub>O</sub> < V <sub>CC</sub> + 0.5V±25mA
DC Output Diode Current, IOK
For $V_0 < -0.5V$ or $V_0 > V_{CC} + 0.5V$ ±20mA
DC Output Source or Sink Current per Output Pin, IO
For $V_0 > -0.5V$ or $V_0 < V_{CC} + 0.5V$
DC V <sub>CC</sub> or Ground Current, I <sub>CC</sub> ±50mA

#### **Operating Conditions**

Temperature Range ( $T_A$ )
Supply Voltage Range, V <sub>CC</sub>
HC Types
HCT Types4.5V to 5.5V
DC Input or Output Voltage, VI, VO 0V to VCC
Input Rise and Fall Time
2V
4.5V 500ns (Max)
6V

#### **Thermal Information**

Thermal Resistance (Typical, Note 1)	θ <sub>JA</sub> ( <sup>o</sup> C/W)
E (PDIP) Package	80
M (SOIC) Package	86
Maximum Junction Temperature (Hermetic Package or D	ie) 175 <sup>0</sup> C
Maximum Junction Temperature (Plastic Package)	150 <sup>0</sup> C
Maximum Storage Temperature Range6	5 <sup>o</sup> C to 150 <sup>o</sup> C
Maximum Lead Temperature (Soldering 10s)	
(SOIC - Lead Tips Only)	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

#### **DC Electrical Specifications**

		TEST CONDITIONS			25 <sup>0</sup> C			-40 <sup>0</sup> C T	О 85 <sup>0</sup> С	-55°C TO 125°C		
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	v <sub>cc</sub> (v)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES												
High Level Input	V <sub>IH</sub>	-	-	2	1.5	-	-	1.5	-	1.5	-	V
Voltage				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input	V <sub>IL</sub>	-	-	2	-	-	0.5	-	0.5	-	0.5	V
Voltage				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output V <sub>OH</sub> Voltage CMOS Loads	V <sub>IH</sub> or	-0.02	2	1.9	-	-	1.9	-	1.9	-	V	
		VIL	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output			-	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output	V <sub>OL</sub>	V <sub>IH</sub> or	0.02	2	-	-	0.1	-	0.1	-	0.1	V
Voltage CMOS Loads		VIL	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output			-	-	-	-	-	-	-	-	-	V
Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	lı	V <sub>CC</sub> or GND	-	6	-	-	±0.1	-	±1	-	±1	μA

#### DC Electrical Specifications (Continued)

			ST ITIONS			25 <sup>0</sup> C		-40 <sup>0</sup> C 1	O 85°C	-55°C T	0 125 <sup>0</sup> C	
PARAMETER	SYMBOL	V <sub>I</sub> (V)	I <sub>O</sub> (mA)	V <sub>CC</sub> (V)	MIN	ТҮР	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	Icc	V <sub>CC</sub> or GND	0	6	-	-	4	-	40	-	80	μA
HCT TYPES												•
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	Ι	V <sub>CC</sub> and GND	-	5.5	-		±0.1	-	±1	-	±1	μA
Quiescent Device Current	Icc	V <sub>CC</sub> or GND	0	5.5	-	-	4	-	40	-	80	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 2)	V <sub>CC</sub> - 2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

#### NOTE:

2. For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

#### **HCT Input Loading Table**

INPUT	UNIT LOADS
All	0.3
NOTE: Unit Load is Alea limit spe	cified in DC Electrical Specifica-

NOTE: Unit Load is  $\Delta I_{CC}$  limit specified in DC Electrical Specifications table, e.g., 360µA max at 25°C.

	HC TYPES	HCT TYPES
Input Level	V <sub>CC</sub>	3V
VS	50% V <sub>CC</sub>	1.3V

### NOTE: Transition times and propagation delay times

### Prerequisite For Switching Specifications

MIN MAX 100 -	MIN 120	MAX	
	120		
	120		
		-	ns
20 -	24	-	ns
17 -	20	-	ns
100 -	120	-	ns
20 -	24	-	ns
17 -	20	-	ns
20	0 -	0 - 24	0 - 24 -

		TEST	v <sub>cc</sub>		25 <sup>0</sup> C		-40 <sup>0</sup> C T	O 85°C	-55°C T	O 125 <sup>0</sup> C	
PARAMETER	SYMBOL	CONDITIONS	(V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
Setup Time, J, K to CP	t <sub>SU</sub>	C <sub>L</sub> = 50pF	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
Hold Time, J, K to CP	t <sub>H</sub>	C <sub>L</sub> = 50pF	2	3	-	-	3	-	3	-	ns
			4.5	3	-	-	3	-	3	-	ns
			6	3	-	-	3	-	3	-	ns
Removal Time	t <sub>REM</sub>	-C <sub>L</sub> = 50pF	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
CP Frequency	f <sub>MAX</sub>	C <sub>L</sub> = 50pF	2	6	-	-	5	-	4	-	MHz
			4.5	30	-	-	25	-	20	-	MHz
		C <sub>L</sub> = 15pF	5	-	60	-	-	-	-	-	MHz
		C <sub>L</sub> = 50pF	6	35	-	-	29	-	23	-	MHz
HCT TYPES											
CP Pulse Width	t <sub>w</sub>	$C_L = 50 pF$	4.5	16	-	-	20	-	24	-	ns
R Pulse Width	t <sub>w</sub>	CL = 50pF	4.5	18	-	-	23	-	27	-	ns
Setup Time, J, K to $\overline{CP}$	t <sub>SU</sub>	CL = 50pF	4.5	16	-	-	20	-	24	-	ns
Hold Time, J, K to $\overline{CP}$	t <sub>H</sub>	CL = 50pF	4.5	3	-	-	3	-	3	-	ns
Removal Time	t <sub>REM</sub>	CL = 50pF	4.5	12	-	-	15	-	18	-	ns
CP Frequency	f <sub>MAX</sub>	CL = 50pF	4.5	30	-	-	25	-	20	-	MHz
		CL = 15pF	5	-	60	-	-	-	-	-	MHz

### Prerequisite For Switching Specifications (Continued)

## Switching Specifications Input $t_r$ , $t_f = 6ns$

		TEST	EST V <sub>CC</sub>		25 <sup>0</sup> C			O 85°C	-55°C TO 125°C		
PARAMETER	SYMBOL	CONDITIONS	(V)	MIN	ТҮР	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES				-	-	-		-	-		
Propagation Delay, CP to Q	t <sub>PLH</sub> , t <sub>PHL</sub>	$C_L = 50 pF$	2	-	-	160	-	200	-	240	ns
			4.5	-	-	32	-	40	-	48	ns
		CL = 15pF	5	-	13	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	28	-	34	-	41	ns
Propagation Delay, $\overline{CP}$ to $\overline{Q}$	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	160	-	200	-	240	ns
			4.5	-	-	32	-	40	-	48	ns
		C <sub>L</sub> = 15pF	5	-	13	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	28	-	34	-	41	ns
Propagation Delay,	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	145	-	180	-	220	ns
$\overline{R}$ to Q, $\overline{Q}$			4.5	-	-	29	-	36	-	44	ns
		C <sub>L</sub> = 15pF	5	-	12	-	-	-	-	-	ns
		C <sub>L</sub> = 50pF	6	-	-	25	-	31	-	38	ns
Output Transition Time	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	2	-	-	75	-	95	18	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns

		TEST CONDITIONS	V <sub>CC</sub> (V)		25 <sup>0</sup> C		-40°C TO 85°C		-55°C TO 125°C			
PARAMETER	SYMBOL			MIN	ТҮР	МАХ	MIN	MAX	MIN	MAX	UNITS	
Input Capacitance	Cl	-	-	-	-	10	-	10	-	10	pF	
Power Dissipation Capacitance (Notes 3, 4)	C <sub>PD</sub>	-	5	-	28	-	-	-	-	-	pF	
HCT TYPES		•										
Propagation Delay, $\overline{CP}$ to Q	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	38	-	48	-	57	ns	
Propagation Delay, $\overline{CP}$ to $\overline{Q}$	t <sub>PLH</sub> , t <sub>PHL</sub>	CL = 50pF	4.5	-	-	36	-	45	-	54	ns	
Propagation Delay, $\overline{R}$ to Q, $\overline{Q}$	t <sub>PLH</sub> , t <sub>PHL</sub>	CL = 50pF	4.5	-	-	34	-	43	-	51	ns	
Output Transition Time	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	4.5	-	-	15	-	19	-	22	ns	
Input Capacitance	Cl	-	-	-	-	10	-	10	-	10	pF	
Power Dissipation Capacitance (Notes 3, 4)	C <sub>PD</sub>	-	5	-	28	-	-	-	-	-	pF	

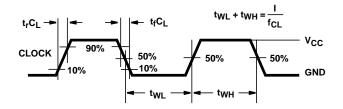
#### Switching Specifications Input tr, tf = 6ns (Continued)

NOTES:

3. C<sub>PD</sub> is used to determine the dynamic power consumption, per flip-flop.

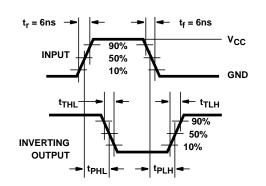
4.  $P_D = C_{PD} V_{CC}^2 f_i + \Sigma C_L V_{CC}^2 f_o$  where  $f_i$  = input frequency,  $f_o$  = output frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

## Test Circuits and Waveforms

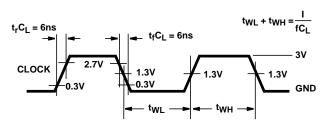


NOTE: Outputs should be switching from 10% V<sub>CC</sub> to 90% V<sub>CC</sub> in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

# FIGURE 2. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

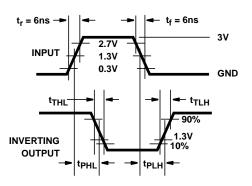




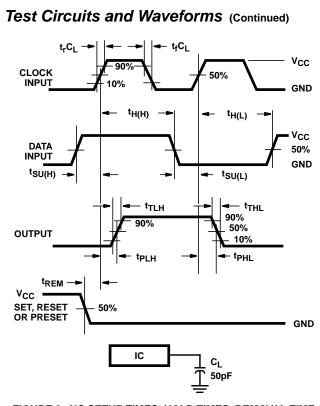


NOTE: Outputs should be switching from 10% V<sub>CC</sub> to 90% V<sub>CC</sub> in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

# FIGURE 3. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH









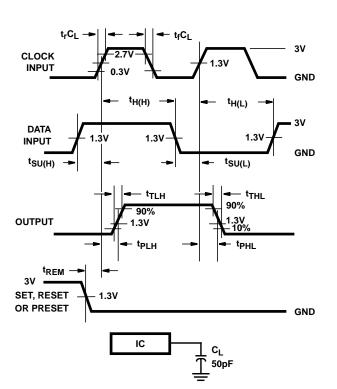


FIGURE 7. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS



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#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-8515301CA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Call TI	
CD54HC73F	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
CD54HC73F3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
CD74HC73E	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC73EE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HC73M	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC73M96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC73M96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC73M96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC73ME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC73MG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC73MT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC73MTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HC73MTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT73E	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT73EE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
CD74HCT73M	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT73ME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
CD74HCT73MG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:



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5-Sep-2011

ACTIVE: Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF CD54HC73, CD74HC73 :

• Catalog: CD74HC73

• Military: CD54HC73

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

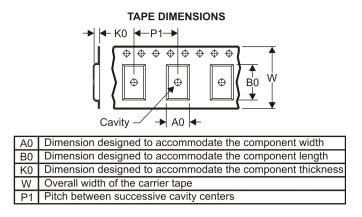
# PACKAGE MATERIALS INFORMATION

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#### TAPE AND REEL INFORMATION





## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC73M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC73MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TEXAS INSTRUMENTS

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# PACKAGE MATERIALS INFORMATION

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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC73M96	SOIC	D	14	2500	346.0	346.0	33.0
CD74HC73MT	SOIC	D	14	250	346.0	346.0	33.0

J (R-GDIP-T\*\*) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- $\triangle$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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