SCLS307B- JANUARY 1996 - REVISED JANUARY 2003

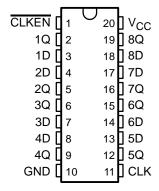
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80-μA Max I_{CC}
- Typical t_{pd} = 12 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 μA Max
- Eight Flip-Flops With Single-Rail Outputs
- Clock Enable Latched to Avoid False Clocking
- Applications Include:
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators

description/ordering information

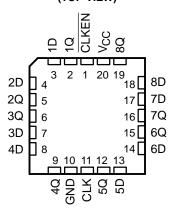
These devices are positive-edge-triggered octal D-type flip-flops with an enable input. The 'HC377 devices are similar to the 'HC273 devices, but feature a latched clock-enable (CLKEN) input instead of a common clear.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse, if CLKEN is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output. These devices are designed to prevent false clocking by transitions at CLKEN.

SN54HC377 . . . J OR W PACKAGE SN74HC377 . . . DW, N, OR NS PACKAGE (TOP VIEW)



SN54HC377 . . . FK PACKAGE (TOP VIEW)



ORDERING INFORMATION

TA	PACKAG	GE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube	SN74HC377N	SN74HC377N
4000 1- 0500	0010 014	Tube	SN74HC377DW	110077
–40°C to 85°C	SOIC - DW	Tape and reel	SN74HC377DWR	HC377
	SOP - NS	Tape and reel	SN74HC377NSR	HC377
	CDIP – J	Tube	SNJ54HC377J	SNJ54HC377J
-55°C to 125°C	CFP – W	Tube	SNJ54HC377W	SNJ54HC377W
	LCCC - FK	Tube	SNJ54HC377FK	SNJ54HC377FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



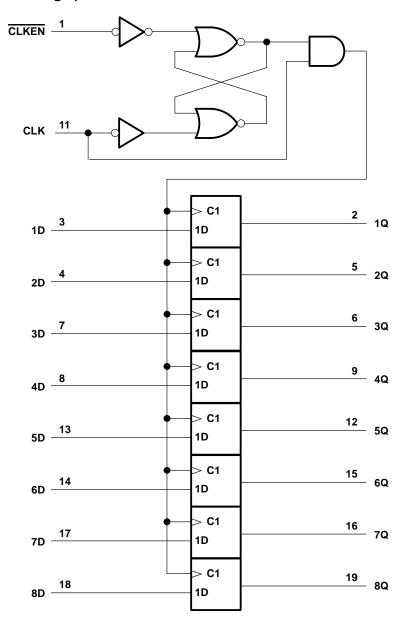
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



FUNCTION TABLE (each flip-flop)

II	INPUTS								
CLKEN	CLK	D	Q						
Н	Х	Χ	Q_0						
L	\uparrow	Н	Н						
L	\uparrow	L	L						
Х	L	Χ	Q_0						

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 7 V
Input clamp current, $I_{ K }(V_1 < 0 \text{ or } V_1 > V_{CC})$ (see Note 1).	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package	e 58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

			SN	N54HC37	7	SN	174HC37	7	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2	5	6	2	5	6	V
		V _{CC} = 2 V	1.5			1.5			
ViH	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			V
		VCC = 6 V	4.2			4.2			
		V _{CC} = 2 V			0.5			0.5	
٧ _{IL}	V _{IL} Low-level input voltage	V _{CC} = 4.5 V			1.35			1.35	V
		VCC = 6 V			1.8			1.8	
٧ _I	Input voltage		0		VCC	0		VCC	V
٧o	Output voltage		0		VCC	0		VCC	V
		V _{CC} = 2 V			1000			1000	
Δt/Δν	Input transition rise/fall time	V _{CC} = 4.5 V			500			500	ns
		$V_{CC} = 6 V$			400			400	
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

SN54HC377, SN74HC377 OCTAL D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				Т	A = 25°C	;	SN54H	C377	SN74H	C377	
PARAMETER	TEST CO	ONDITIONS	vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V	1.9	1.998		1.9		1.9		
		$I_{OH} = -20 \mu A$	4.5 V	4.4	4.499		4.4		4.4		
∨он	VI = VIH or VIL		6 V	5.9	5.999		5.9		5.9		V
		$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
		$I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.8		5.2		5.34		
			2 V		0.002	0.1		0.1		0.1	
		I _{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	
VOL	VI = VIH or VIL		6 V		0.001	0.1		0.1		0.1	V
		I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		$I_{OL} = 5.2 \text{ mA}$	6 V		0.15	0.26		0.4		0.33	
lį	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
Icc	$V_I = V_{CC}$ or 0,	IO = 0	6 V			8		160		80	μΑ
C _i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			.,	T _A = 1	25°C	SN54H	C377	SN74H	C377											
			vcc	MIN	MAX	MIN	MAX	MIN	MAX	UNIT										
			2 V		5		3		4											
fclock	Clock frequency	4.5 V		25		16		20	MHz											
		6 V		29		19		23												
			2 V	100		150		125												
t _w	Pulse duration, CLK high o	r low	4.5 V	20		30		25		ns										
			6 V	17		25		21												
			2 V	100		150		125												
		D	4.5 V	20		30		25												
	0 - t t t - t 0 ()		6 V	17		25		21												
t _{su}	Setup time before CLK↑	CLKEN high or low	2 V	100		150		125		ns										
	CLKEN high or low		CLKEN high or low	CLKEN high or low		CLKEN high or low		20		30		25								
			6 V	17		25		21												
		CLKEN inactive or active, data	2 V	5		5		5												
th	Hold time after CLK↑					CLKEN inactive or active, data 4.5 V 5	5		5											
			6 V	5		5		5												



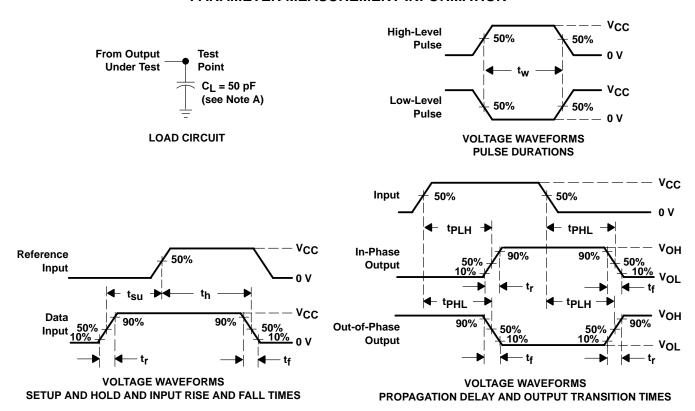
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

DADAMETER	FROM	то	.,	T,	4 = 25°C	;	SN54H	IC377	SN74HC377		
PARAMETER	(INPUT)	(OUTPUT)	vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V	5	11		3		4		
f _{max}			4.5 V	25	54		16		20		MHz
		6 V	29	64		19		23			
			2 V		56	160		240		200	
t _{pd}	CLK	Any	4.5 V		15	32		48		40	ns
·			6 V		12	27		41		34	
			2 V		38	75		110		95	
t _t		Any	4.5 V		8	15		22		19	ns
			6 V		6	13		19		16	

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per flip-flop	No load	30	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and test-fixture capacitance.

- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50~\Omega$, $t_f = 6$ ns, $t_f = 6$ ns.
- C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



5-Sep-2011

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-87807012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8780701RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
SN54HC377J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SN74HC377DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC377DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC377DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC377DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC377DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC377DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC377N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74HC377NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74HC377NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC377NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC377NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54HC377FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54HC377J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.



PACKAGE OPTION ADDENDUM

5-Sep-2011

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54HC377, SN74HC377:

Catalog: SN74HC377

Military: SN54HC377

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications



TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC377DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74HC377NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC377DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74HC377NSR	SO	NS	20	2000	346.0	346.0	41.0

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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