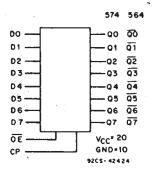
Data sheet acquired from Harris Semiconductor SCHS292



## Octal D-Type Flip-Flop, 3-State Positive-Edge-Triggered

CD54/74AC/ACT564 - Inverting CD54/74AC/ACT574 - Non-Inverting

## Type Features:

- Buffered inputs
- Typical propagation delay: 6.5 ns @ V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25° C, C<sub>L</sub> = 50 pF

**FUNCTIONAL DIAGRAM** 

The RCA-CD54/74AC564 and CD54/74AC574 and the CD54/74ACT564 and CD54/74ACT574 octal D-type, 3-state, positive-edge-triggered flip-flops use the RCA ADVANCED CMOS technology. The eight flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). The Output Enable ( $\overline{OE}$ ) controls the 3-state outputs and is independent of the register operation. When the Output Enable ( $\overline{OE}$ ) is HIGH, the outputs are in the high-impedance state. The CD54/74AC/ACT564 and CD54/74AC/ACT574 share the same pin configurations; the CD54/74AC/ACT564, however, has inverted outputs and the CD54/74AC/ACT574 has non-inverted outputs.

The CD74AC/ACT564 and CD74AC/ACT574 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT564 and CD54AC/ACT574, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

## **Family Features:**

- Exceeds 2-kV ESD Protection MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- ± 24-mA output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

#### TRUTH TABLE

	INPUTS	OUTPUTS			
013			564	574	
OE	СР	Dn	Qn	Qn	
_L		Н	L	Н	
L		L	Н	L	
L	L	Х	QΘ	QO	
Н	X	Х	Z	Z	

H = High level (steady state)

L = Low level (steady state)

X = Don't care

\_/ = Transition from low to high level

QO = The level of Q before the indicated steady-state input conditions were established

QO = The level of Q before the indicated steady-state input conditions were established.

Z = High impedance

This data sheet is applicable to the CD54/74AC574 and CD54/74AC574. The CD54/74AC564 and CD54/74ACT564 were not acquired from Harris Semiconductor.

MAXIMUM RATINGS, Absolute-Maximum Values:
DC SUPPLY-VOLTAGE (Vcc) -0.5 to 6 V
DC INPUT DIODE CURRENT, $I_{ik}$ (for $V_i < -0.5 \text{ V or } V_i > V_{cc} + 0.5 \text{ V}$ )
DC OUTPUT DIODE CURRENT, $l_{OK}$ (for $V_0 < -0.5$ V or $V_0 > V_{CC} + 0.5$ V)
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, $I_0$ (for $V_0 > -0.5$ V or $V_0 < V_{cc} + 0.5$ V) $\pm 50$ mA
DC V <sub>∞</sub> or GROUND CURRENT (I <sub>∞</sub> or I <sub>GND</sub> )
POWER DISSIPATION PER PACKAGE (PD):
For $T_A = -55$ to $+100$ °C (PACKAGE TYPE E)
For T <sub>A</sub> = +100 to +125°C (PACKAGE TYPE E)
For $T_A = -55$ to $+70^{\circ}$ C (PACKAGE TYPE M)
For T <sub>A</sub> = +70 to +125°C (PACKAGE TYPE M) Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T <sub>A</sub> ):55 to +125°C
STORAGE TEMPERATURE (T <sub>stg</sub> )65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 $\pm$ 1/32 in. (1.59 $\pm$ 0.79 mm) from case for 10 s maximum+265° C
Unit inserted into PC board min, thickness 1/16 in. (1.59 mm) with solder contacting lead tips only +300°C
*For up to 4 outputs per device; add $\pm$ 25 mA for each additional output.

## **RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

		1101170		
CHARACTERISTIC		MIN.	MAX.	UNITS
Supply-Voltage Range, Vcc*:				
(For $T_A = Full Package-Temperature Range)$			l	
AC Types		1.5	5.5	V
ACT Types		4.5	5.5	V
DC Input or Output Voltage, V <sub>1</sub> , V <sub>0</sub>		0	Vcc	V
Operating Temperature, T <sub>A</sub> :		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv				
at 1.5 V to 3 V (AC Types)	į	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)		0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)		0	10	ns/V

<sup>\*</sup>Unless otherwise specified, all voltages are referenced to ground.

## TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC/ACT564

CD54/74AC/ACT574

## STATIC ELECTRICAL CHARACTERISTICS: AC Series

•			•			AMBIEN	T TEMP	RATUR	E (T <sub>A</sub> ) - °	С	
CHARACTERIST	ICS	TEST CONDITIONS		v <sub>cc</sub>	+	+25		o +85	-55 to +125		UNITS
		(V)	l <sub>o</sub> (mA)	(V)	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input				1.5	1.2	_	1.2	_	1.2	1	
Voltage	V <sub>IH</sub>			3	2.1	_	2.1	<u> </u>	2.1	_	1 v
				5.5	3.85		3.85		3.85	_	1
Low-Level Input				1.5	_	0.3	T -	0.3	_	0.3	
Voltage	VIL			3	_	0.9		0.9	_	0.9	l v
				5.5	1 -	1.65	_	1.65		1.65	1
High-Level Output		· · · · · · · · · · · · · · · · · · ·	-0.05	1.5	1.4	_	1.4		1.4		,
Voltage	V <sub>OH</sub>	V <sub>IH</sub>	-0.05	3	2.9		2.9	_	2.9	Τ_	1
		or	-0.05	4.5	4.4		4.4	_	4.4	_	1
		V <sub>IL</sub>	-4	3	2.58	_	2.48	_	2.4		v
	-		-24	4.5	3.94		3.8	_	3.7		1
			-75	5.5			3.85		_	_	1
		#. * {	-50	5.5		_	_	_	3.85	_	1
Low-Level Output			0.05	1.5	_	0.1		0.1	_	0.1	
Voltage	Vol	V <sub>IH</sub>	0.05	3	_	0.1	_	0.1	_	0.1	
		or	0.05	4.5		0.1	<b>-</b>	0.1	_	0.1	v
		V <sub>IL</sub>	12	3	_	0.36	_	0.44		0.5	
			24	4.5	_	0.36	_	0.44	_	0.5	
		<i>s</i>	75	5.5	_	_	_	1.65	_		
		#, * {	50	5.5	_	_	_	_	_	1.65	
Input Leakage Current	I <sub>1</sub>	V <sub>∞</sub> or GND		5.5	-	±0.1		±1	_	±1	μΑ
3-State Leakage		V <sub>IH</sub>									
Current	loz	or									
		VıL									
		V <sub>o</sub> =		5.5	_	±0.5	_	±5		±10	μΑ
		Vcc							·	, ,	
		or									
		GND	ļ			."					
Quiescent Supply Current, MSI	loc	V <sub>cc</sub> or GND	0	5.5		8		80		160	μΑ

<sup>#</sup>Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
\*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

		,	* 1			AMBIEN	T TEMPE	RATURE	(T <sub>A</sub> ) - °	С	J
CHARACTERIST	ICS	TEST COI	NDITIONS	V <sub>cc</sub>	+	25	-40 to +85		-55 to +125		UNITS
		V <sub>1</sub> l <sub>o</sub> (mA)		(V)	MIN.	MAX.	MIN.	MAX.	1 1 1		
High-Level Input Voltage	V <sub>IH</sub>			4.5 to 5.5	2	_	2	_	2	_	٧
Low-Level Input Voltage	ViL			4.5 to 5.5	_	0.8	_	0.8		0.8	v
High-Level Output		V <sub>IH</sub>	-0.05	4.5	4.4	1 _	4.4	_	4.4	_	
Voltage	VoH	or 	-24	4.5	3.94	_	3.8		3.7		v
· ·		VIL.	-75	5.5			3.85				1 *
		#, * {	-50	5.5	_	_		_	3.85	_	]
Low-Level Output		V <sub>IH</sub>	0.05	4.5		±0.1		±.1		±.1	
Voltage	Voltage Vol	or	24	4.5		0.36		0.44		0.5	V
		Vil S	75	5.5	_			1.65	_	-	]
		#, * {	50	5.5			_		_	1.65	
Input Leakage Current	ŀı	V <sub>cc</sub> or GND		5.5	_	±0.1	_	±1		±1	μΑ
3-State Leakage Current	l <sub>oz</sub>	V <sub>IH</sub> or V <sub>IL</sub>									
		V <sub>O</sub> = V <sub>CC</sub> or GND		5.5	. <del>_</del>	±0.5	<del></del>	±5		±10	μΑ
Quiescent Supply Current, MSI	lcc	V <sub>∞</sub> or GND	0	5.5		8	<u> </u>	80		160	μΑ
Additional Quiescent Current per Input Pi TTL Inputs High 1 Unit Load	Supply in ΔI <sub>CC</sub>	V <sub>cc</sub> -2.1		4.5 to 5.5	—	2.4		2.8	_	3	mA

<sup>#</sup>Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

## **ACT INPUT LOADING TABLE**

INPUT	UNIT LOADS*
D, <del>ŌE</del>	0.7
CP	1.17

<sup>\*</sup>Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

<sup>\*</sup>Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

## PREREQUISITE FOR SWITCHING: AC Series

			AMBI	ENT TEMP	ERATURE (	TA) -°C		
CHARACTERISTICS	SYMBOL	(V)	-40 to +85		-55 to +125		UNITS	
· ·			MIN.	MAX.	MIN.	MAX.		
Clock Pulse Width	tw	1.5 3.3* 5†	44 4.9 3.5	=	50 5.6 4	=	ns	
Setup Time Data to Clock	tsu	1.5 3.3 5	2 2 2	=	2 2 2		ns	
Hold Time Data to Clock	ţ <b>t</b> H	1.5 3.3 5	2 2 2	=	2 2 2	_ , 	ns	
Maximum Clock Frequency	f <sub>MAX</sub>	1.5 3.3 5	11 101 143		10 89 125	_ _ _	MHz	

\*3.3 V: min. is @ 3 V †5 V: min. is @ 4.5 V

## SWITCHING CHARACTERISTICS: AC Series; $t_{rr}$ , $t_{t}$ = 3 ns, $C_{L}$ = 50 pF

			AMBI	ENT TEMP	ERATURE (	T <sub>A</sub> ) -°C	
CHARACTERISTICS	SYMBOL	V <sub>cc</sub> (V)	-40 to +85		-55 (	UNITS	
	1	(*)	MIN.	MAX.	MIN.	MAX.	1
Propagation Delays: Clock to Q AC574	t <sub>PLH</sub>	1.5 3.3* 5†	- 4 2.9	123 13.7 9.8	3.8 2.7	135 15.1 10.8	ns
Clock to Q AC564	t <sub>PLH</sub> t <sub>PHL</sub>	1.5 3.3 5	- 4.1 2.9	128 14.4 10.3	_ 4 2.8	141 15.8 11.3	ns
Output Enable to Q, ₫	t <sub>PZL</sub> t <sub>PZH</sub>	1.5 3.3 5	5.6 3.7	165 19.2 13.2	 5.5 3.6	181 21.8 14.5	ns
Output Disable to Q, Q	t <sub>PLZ</sub>	1.5 3.3 5	4.7 3.7	165 16.5 13.2	4.5 3.6	181 18.1 14.5	ns
Power Dissipation Capacitance	C <sub>PO</sub> §	_	67	Тур.	67	Тур.	pF
Min. (Valley) V <sub>OH</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OHV</sub> See . Fig. 1	5	4 Typ. @ 25°C			v	
Max. (Peak) V <sub>OL</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C			v	
Input Capacitance	Cı		_	10	_	10	pF
3-State Output Capacitance	Co	_		15		15	pF

\*3.3 V: min. is @ 3.6 V max. is @ 3 V †5 V: min. is @ 5.5 V max. is @ 4.5 V

§C<sub>PD</sub> is used to determine the dynamic power consumption, per flip flop.

 $P_D = C_{PO} V_{CC}^2 f_i + \sum V_{CC}^2 f_O C_L$  where  $f_i = input$  frequency

fo = output frequency C<sub>L</sub> = output load capacitance

V<sub>cc</sub> = supply voltage.

Technical Data.

# CD54/74AC564, CD54/74AC574 CD54/74ACT564, CD54/74ACT574

PREREQUISITE FOR SWITCHING: ACT Series

		V <sub>cc</sub> (V)	AMBI	I			
CHARACTERISTICS	SYMBOL		-40 to +85		-55 to +125		UNITS
			MIN.	MAX.	MIN.	MAX.	
Clock Pulse Width	tw	5†	3.9	_	4.5	_	ns
Setup Time Data to Clock	t <sub>su</sub>	5	2	<u> </u>	2	_	ns
Hold Time Data to Clock	t <sub>H</sub>	5	2.6		3	-	ns
Maximum Clock Frequency	fmax	5	125		110		MHz

†5 V: min. is @ 4.5 V

## SWITCHING CHARACTERISTICS: ACT Series; t,, t, = 3 ns, CL = 50 pF

			AMBIENT TEMPE		RATURE (	Γ <sub>A</sub> ) -° C	
CHARACTERISTICS	SYMBOL	V <sub>cc</sub>	-40 to +85		-55 to +125		UNITS
		(V)	MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Clock to Q ACT574	тецн тенц	5†	2.9	10.2	2.8	11.2	ns
Clock to Q ACT564	t <sub>PLH</sub> t <sub>PHL</sub>	5	3	10.6	2.9	11.7	ns
Output Enable and Disable to Q ACT574	tplz tpHz tpZL tpZH	5	3.7	13.2	3.6	14.5	ns
Output Enable and Disable to Q ACT564	tplz tpHz tpżl tpzH	5	3.7	13.2	3.6	14.5	ns
Power Dissipation Capacitance	C <sub>PO</sub> §		67	Тур	67	Тур.	pF
Min. (Valley) V <sub>он</sub> During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>онv</sub> See Fig. 1	5	4 Typ. @ 25° C		V		
Max. (Peak) Vol. During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C			V	
Input Capacitance	Cı			10		10	ρF
3-State Output Capacitance	Со	<u> </u>		15		15	pF

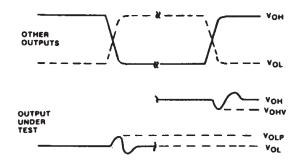
†5 V: min. is @ 5.5 V max. is @ 4.5 V

 $\S{C_{PD}}$  is used to determine the dynamic power consumption, per flip flop.  $P_D = C_{PD} \ V_{CC}^2 \ f_i + \Sigma \ V_{CC}^2 \ f_0 \ C_L + V_{CC} \ \Delta I_{CC}$  where  $f_i =$  input frequency

 $f_0$  = output frequency  $C_L$  = output load capacitance

 $V_{cc} = supply voltage.$ 

#### PARAMETER MEASUREMENT INFORMATION



- VOHY AND VOLP ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
   INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS:
- PRR  $\leq$  1 MHz,  $t_{\rm f}$  = 3 ns,  $t_{\rm f}$  = 3 ns, SKEW 1 ns.
- 3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED.
  IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 µF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MH2 BANDWIDTH.

9205-42406

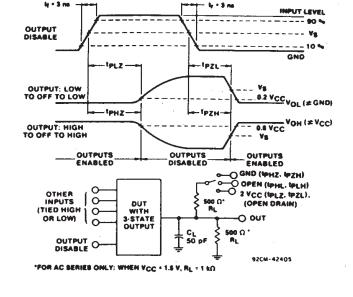
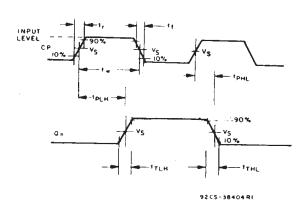
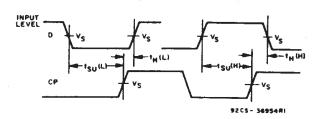
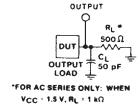


Fig. 1 - Simultaneous switching transient waveforms.

Fig. 2 - Three-state propagation delay waveforms and test circuit.







	CD54/74AC	CD54/74ACT
Input Level	V <sub>cc</sub>	3 V
Input Switching Voltage, Vs	0.5 V <sub>cc</sub>	1.5 V
Output Switching Voltage, Vs	0.5 V <sub>cc</sub>	0.5 V <sub>CC</sub>

Fig. 3 - Propagation delays times and test circuit.

## PACKAGE OPTION ADDENDUM

www.ti.com 15-Oct-2009

#### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD54AC574F3A	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
CD54ACT574F3A	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
CD74AC574E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74AC574EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74AC574M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC574M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC574M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC574M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC574ME4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC574MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT574E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74ACT574EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74ACT574M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT574M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT574M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT574M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT574ME4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT574MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



## PACKAGE OPTION ADDENDUM

www.ti.com 15-Oct-2009

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

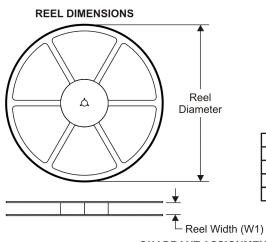
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## TAPE AND REEL INFORMATION



# TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



## \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC574M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CD74ACT574M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1





\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC574M96	SOIC	DW	20	2000	346.0	346.0	41.0
CD74ACT574M96	SOIC	DW	20	2000	346.0	346.0	41.0

## 14 LEADS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

## PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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