



description/ordering information

The 'AHC74 dual positive-edge-triggered devices are D-type flip-flops.

A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

ORDERING INFORMATION

T _A	PACKA	GE [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	QFN – RGY	Tape and reel	SN74AHC74RGYR	HA74
	PDIP – N	Tube	SN74AHC74N	SN74AHC74N
	SOIC – D	Tube	SN74AHC74D	AHC74
	5010 - 0	Tape and reel	SN74AHC74DR	AHC74
–40°C to 85°C	SOP – NS	Tape and reel	SN74AHC74NSR	AHC74
	SSOP – DB	Tape and reel	SN74AHC74DBR	HA74
	TSSOP – PW	Tube	SN74AHC74PW	11074
	1550P - PW	Tape and reel	SN74AHC74PWR	HA74
	TVSOP – DGV	Tape and reel	SN74AHC74DGVR	HA74
	CDIP – J	Tube	SNJ54AHC74J	SNJ54AHC74J
–55°C to 125°C	CFP – W	Tube	SNJ54AHC74W	SNJ54AHC74W
	LCCC – FK	Tube	SNJ54AHC74FK	SNJ54AHC74FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



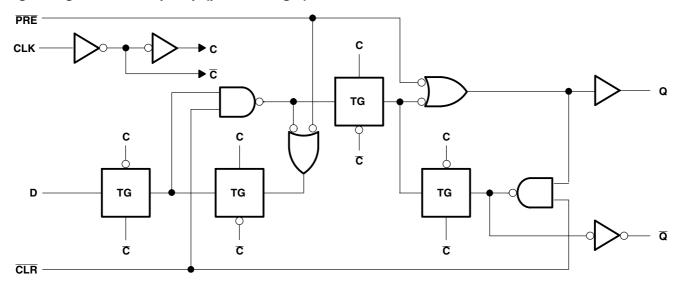
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	FUNCTION TABLE (each flip-flop)										
	INPUTS OUTPUTS										
PRE	CLR	CLK	D	Q	Q						
L	Н	Х	Х	Н	L						
н	L	х	Х	L	Н						
L	L	х	Х	H†	H†						
н	Н	\uparrow	Н	Н	L						
н	Н	\uparrow	L	L	Н						
н	Н	L	Х	Q ₀	\overline{Q}_0						

[†] This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

logic diagram, each flip-flop (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. The package thermal impedance is calculated in accordance with JESD 51-7.
 - 3. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 4)

			SN54A	HC74	SN74A	HC74	
			MIN	MAX	MIN	MAX	UNIT
V _{CC}	Supply voltage		2	5.5	2	5.5	V
		$V_{CC} = 2 V$	1.5		1.5		
VIH	High-level input voltage	$V_{CC} = 3 V$	2.1		2.1		V
		V _{CC} = 5.5 V	3.85		3.85		
		$V_{CC} = 2 V$		0.5		0.5	
VIL	Low-level input voltage	$V_{CC} = 3 V$		0.9		0.9	V
		V _{CC} = 5.5 V		1.65		1.65	
VI	Input voltage		0	5.5	0	5.5	V
Vo	Output voltage		0	V_{CC}	0	V _{CC}	V
		$V_{CC} = 2 V$		-50		-50	μA
l _{OH}	High-level output current	$V_{CC}=3.3~V\pm0.3~V$		-4		-4	
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		-8		-8	mA
		$V_{CC} = 2 V$		50		50	μA
l _{OL}	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4		4	
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		8		8	mA
		$V_{CC}=3.3~V\pm0.3~V$		100		100	
$\Delta t / \Delta v$	Input transition rise or fall rate	$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		20		20	ns/V
T _A	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			T,	ק = 25°C	;	SN54A	HC74	SN74A	HC74	
PARAMETER	TEST CONDITIONS	v _{cc}	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		2 V	1.9	2		1.9		1.9		
	l _{OH} = -50 μA	3 V	2.9	3		2.9		2.9		
V _{OH}		4.5 V	4.4	4.5		4.4		4.4		V
	$I_{OH} = -4 \text{ mA}$	3 V	2.58			2.48		2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		
		2 V			0.1		0.1		0.1	
	l _{OL} = 50 μA	3 V			0.1		0.1		0.1	
V _{OL}		4.5 V			0.1		0.1		0.1	V
	I _{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I _{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
l _l	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*		±1	μA
I _{CC}	$V_{I} = V_{CC} \text{ or } GND, \qquad I_{O} = 0$	5.5 V			2		20		20	μA
Ci	$V_I = V_{CC}$ or GND	5 V		2	10				10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC} = 0 V$.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

			T _A = 25°C SN54AHC74		HC74	SN74A			
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
	Data a danatian	PRE or CLR low	6		7		7		
tw	Pulse duration	CLK	6		7		7		ns
		Data	6		7		7		
t _{su}	Setup time before CLK↑	PRE or CLR inactive	5		5		5		ns
t _h	Hold time, data after CLK^\uparrow		0.5		0.5		0.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

			T _A = 25°C		SN54AHC74		SN74AHC74		
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT
	Dulas duration	PRE or CLR low	5		5		5		
t _w	Pulse duration	CLK	5		5		5		ns
	Coture times hofered OLIC	Data	5		5		5		
t _{su}	Setup time before CLK [↑]	PRE or CLR inactive	3		3		3		ns
t _h	Hold time, data after CLK^\uparrow		0.5		0.5		0.5		ns



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switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

	•		, ,	-	•						
DADAMETED	FROM	то	LOAD	T	_A = 25°C	;	SN54A	HC74	SN74A	HC74	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	ТҮР	MAX	MIN	MAX	MIN	MAX	UNIT
4			C _L = 15 pF	80*	125*		70*		70		N 41 1-
f _{max}			C _L = 50 pF	50	75		45		45		MHz
t _{PLH}		0	0 15 -5		7.6*	12.3*	1*	14.5*	1	14.5	
t _{PHL}	PRE or CLR	Q or Q	C _L = 15 pF		7.6*	12.3*	1*	14.5*	1	14.5	ns
t _{PLH}		0	0 15 55		6.7*	11.9*	1*	14*	1	14	
t _{PHL}	CLK	Q or Q	C _L = 15 pF		6.7*	11.9*	1*	14*	1	14	ns
t _{PLH}		0	0 50 55		10.1	15.8	1	18	1	18	
t _{PHL}	PRE or CLR	Q or Q	C _L = 50 pF		10.1	15.8	1	18	1	18	ns
t _{PLH}	CLK	Q or Q	C _I = 50 pF		9.2	15.4	1	17.5	1	17.5	
t _{PHL}	ULK		CL = 50 pF		9.2	15.4	1	17.5	1	17.5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

	FROM	то	LOAD	Т	A = 25°C	;	SN54A	HC74	SN74A	HC74	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	ТҮР	MAX	MIN	MAX	MIN	MAX	UNIT
			C _L = 15 pF	130*	170*		110*		110		N#1-
f _{max}			C _L = 50 pF	90	115		75		75		MHz
t _{PLH}		0	0 15 -5		4.8*	7.7*	1*	9*	1	9	
t _{PHL}	PRE or CLR	Q or Q	C _L = 15 pF		4.8*	7.7*	1*	9*	1	9	ns
t _{PLH}	CLK	0	0 15 -5		4.6*	7.3*	1*	8.5*	1	8.5	
t _{PHL}	ULK	Q or Q	C _L = 15 pF		4.6*	7.3*	1*	8.5*	1	8.5	ns
t _{PLH}	PRE or CLR	0	0 50 55		6.3	9.7	1	11	1	11	
t _{PHL}	PRE of CLR	Q or Q	C _L = 50 pF		6.3	9.7	1	11	1	11	ns
t _{PLH}	CLK	Q or Q	C _I = 50 pF		6.1	9.3	1	10.5	1	10.5	20
t _{PHL}	ULK		$O_L = 50 \text{ pr}$		6.1	9.3	1	10.5	1	10.5	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 5)

		SN74A	HC74	
	PARAMETER	MIN	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.8	V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}	4.7		V
V _{IH(D)}	High-level dynamic input voltage	3.5		V
V _{IL(D)}	Low-level dynamic input voltage		1.5	V

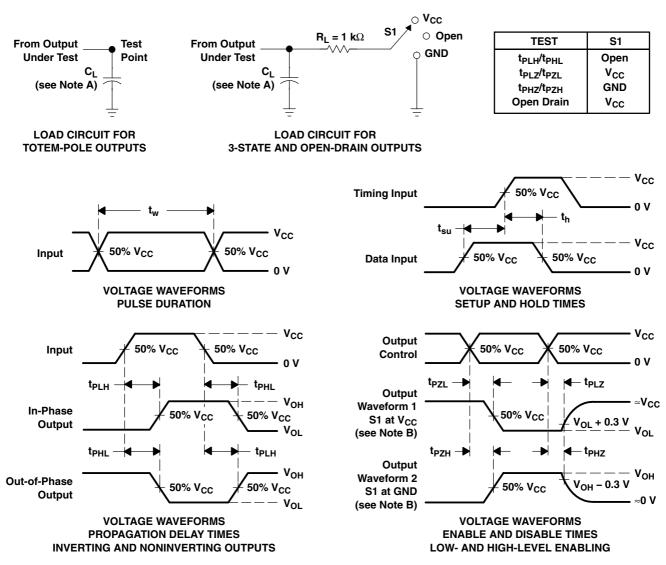
NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5 V$, $T_A = 25^{\circ}C$

	PARAMETER	TEST C	ONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load,	f = 1 MHz	32	pF



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PARAMETER MEASUREMENT INFORMATION

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_Q = 50 Ω , t_f \leq 3 ns, t_f \leq 3 ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms





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5-Sep-2011

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-9686001Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9686001QCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Call TI	
5962-9686001QDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Call TI	
SN74AHC74D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHC74DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI	
SN74AHC74DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHC74DBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHC74DBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHC74DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHC74DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHC74DGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHC74DGVRE4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHC74DGVRG4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHC74DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHC74DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHC74DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHC74N	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AHC74NE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AHC74NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



5-Sep-2011

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74AHC74NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHC74NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHC74PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHC74PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHC74PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHC74PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	
SN74AHC74PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHC74PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHC74PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHC74RGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN74AHC74RGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SNJ54AHC74FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54AHC74J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SNJ54AHC74W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.



5-Sep-2011

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above. Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54AHC74, SN74AHC74 :

Catalog: SN74AHC74

in homogeneous material)

Enhanced Product: SN74AHC74-EP, SN74AHC74-EP

• Military: SN54AHC74

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications

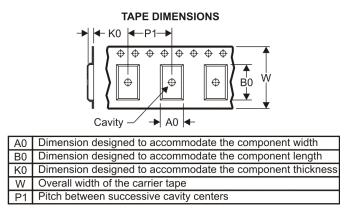
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC74DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74AHC74DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC74DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC74NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC74PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC74RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

30-Jul-2010



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC74DBR	SSOP	DB	14	2000	346.0	346.0	33.0
SN74AHC74DGVR	TVSOP	DGV	14	2000	346.0	346.0	29.0
SN74AHC74DR	SOIC	D	14	2500	346.0	346.0	33.0
SN74AHC74NSR	SO	NS	14	2000	346.0	346.0	33.0
SN74AHC74PWR	TSSOP	PW	14	2000	346.0	346.0	29.0
SN74AHC74RGYR	VQFN	RGY	14	3000	346.0	346.0	29.0

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB



LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N**) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



MECHANICAL DATA

PLASTIC SMALL-OUTLINE

MPDS006C - FEBRUARY 1996 - REVISED AUGUST 2000

DGV (R-PDSO-G**)

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins MO-153

14/16/20/56 Pins – MO-194



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



A. An integration of the information o

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153



LAND PATTERN DATA



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA



- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- earrow Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
- The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.



RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

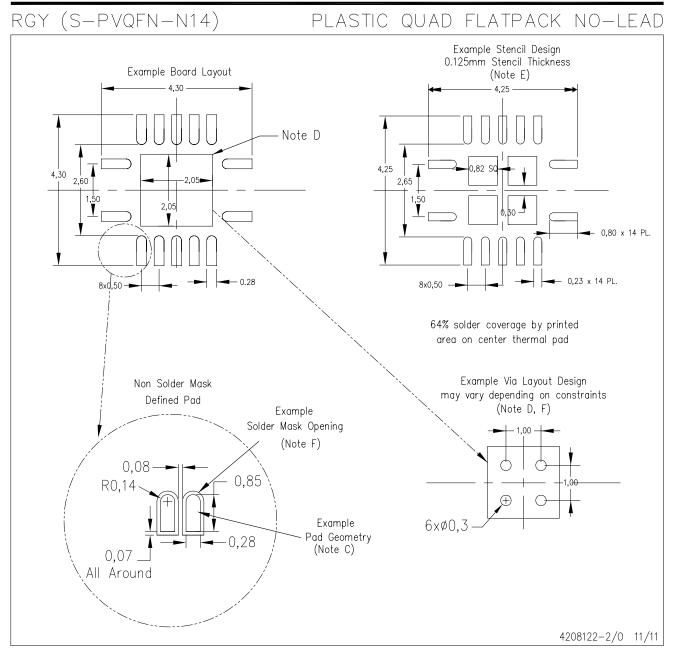
For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com.

- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



MECHANICAL DATA

MSSO002E - JANUARY 1995 - REVISED DECEMBER 2001

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150



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