SN54AHCT374, SN74AHCT374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS241L - OCTOBER 1995 - REVISED JULY 2003

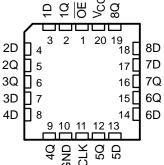
- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17

SN54AHCT374 . . . J OR W PACKAGE SN74AHCT374 . . . DB, DGV, DW, N, NS, OR PW PACKAGE (TOP VIEW)

ŌĒ [1	U	20] v _{cc}
1Q [2		19	8Q
1D [3		18] 8D
2D [4		17] 7D
2Q [5		16] 7Q
3Q [6		15] 6Q
3D [7		14] 6D
4D [8		13] 5D
4Q [9		12] 5Q
GND [10		11	CLK

- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54AHCT374 ... FK PACKAGE (TOP VIEW)



description/ordering information

The 'AHCT374 devices are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

ORDERING INFORMATION

TA	PACK	AGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	PDIP – N	Tube	SN74AHCT374N	SN74AHCT374N	
	SOIC - DW	Tube	SN74AHCT374DW	AHCT374	
	SOIC - DW	Tape and reel	SN74AHCT374DWR	AUC13/4	
–40°C to 85°C	SOP - NS	Tape and reel	SN74AHCT374NSR	AHCT374	
SSOP – DB		Tape and reel	SN74AHCT374DBR	HB374	
	TSSOP – PW	Tube	SN74AHCT374PW	HB374	
	1330F - FW	Tape and reel	SN74AHCT374PWR	пвэ/4	
	TVSOP - DGV	Tape and reel	SN74AHCT374DGVR	HB374	
	CDIP – J		SNJ54AHCT374J	SNJ54AHCT374J	
–55°C to 125°C	CFP – W	Tube	SNJ54AHCT374W	SNJ54AHCT374W	
	LCCC – FK	Tube	SNJ54AHCT374FK	SNJ54AHCT374FK	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



SN54AHCT374, **SN74AHCT374** OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS241L - OCTOBER 1995 - REVISED JULY 2003

description/ordering information (continued)

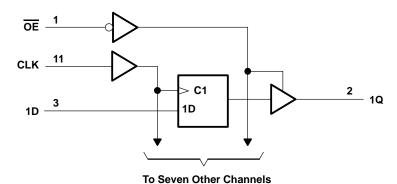
OE does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE (each flip-flop)

	INPUTS		OUTPUT
E	CLK	D	Q
L	1	Н	Н
L	\uparrow	L	L
L	H or L	Χ	Q_0
Н	Χ	Χ	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	Supply voltage range, V_{CC}	DB package DGV package DW package N package NS package PW package	-0.5 V to 7 V -0.5 V to V _{CC} + 0.5 V -20 mA -20 mA -25 mA -25 mA -70°C/W -92°C/W -58°C/W -69°C/W -60°C/W -83°C/W
Storage temperature range, T _{stg} –65°C to 150°C	Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



SCLS241L - OCTOBER 1995 - REVISED JULY 2003

recommended operating conditions (see Note 3)

		SN54AHCT:		SN74AH	SN74AHCT374	
		MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
VI	Input voltage	0	5.5	0	5.5	V
Vo	Output voltage	0	VCC	0	VCC	V
ЮН	High-level output current		-8		-8	mA
loL	Low-level output current		8		8	mA
Δt/Δν	Input transition rise or fall rate		20		20	ns/V
TA	Operating free-air temperature	- 55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST COMPITIONS	vcc	T,	Δ = 25°(2	SN54AH	CT374	SN74AH	CT374	UNIT
PARAMETER	TEST CONDITIONS	vcc vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	ONIT
Vou	$I_{OH} = -50 \mu A$	4.5 V	4.4	4.5		4.4		4.4		V
VOH	$I_{OH} = -8 \text{ mA}$	4.5 V	3.94			3.8		3.8		1 '
Voi	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
VOL	I _{OL} = 8 mA	4.5 V			0.36		0.44		0.44	V
lį	$V_I = 5.5 \text{ V or GND}$	0 V to 5.5 V			±0.1		±1*		±1	μΑ
loz	$V_O = V_{CC}$ or GND, $V_I = V_{IH}$ or V_{IL}	5.5 V			±0.25		±2.5		±2.5	μΑ
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40		40	μΑ
∆l _{CC} †	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C _i	V _I = V _{CC} or GND	5 V		4	10				10	pF
Co	$V_O = V_{CC}$ or GND	5 V		9					, and the second	pF

 $^{^{\}star}$ On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C MIN MAX		SN54AH	CT374	SN74AH	UNIT	
				MIN	MAX	MIN	MAX	UNIT
t _W	Pulse duration, CLK high or low	6.5		6.5		6.5		ns
t _{su}	Setup time, data before CLK↑	2.5		2.5		2.5		ns
th	Hold time, data after CLK↑	2.5		2.5		2.5		ns



[†] This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or VCC.

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SCLS241L - OCTOBER 1995 - REVISED JULY 2003

switching characteristics over recommended free-air temperature operating range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T	_A = 25°(3	SN54AI	HCT374	SN74AH	CT374	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
f			C _L = 15 pF	90**	140**		80**		80		MHz
f _{max}			C _L = 50 pF	85	130		75		75		IVITIZ
^t PLH	CLK	Q	C 15 pE		5.6**	9.4**	1**	10.5**	1	10.5	ns
^t PHL	CLK	Q	C _L = 15 pF		5.6**	9.4**	1**	10.5**	1	10.5	116
^t PZH	ŌĒ	Q	C 15 pE		6.5**	10.2**	1**	11.5**	1	11.5	20
^t PZL	UE .	L Q	C _L = 15 pF		6.5**	10.2**	1**	11.5**	1	11.5	ns
^t PHZ	ŌĒ	Q	C _I = 15 pF		6.2**	10.2**	1**	11**	1	11	ns
tPLZ	OE	~	ω OL - 10 pi		6.2**	10.2**	1**	11**	1	11	115
t _{PLH}	CLK	Q	C: 50 pF		6.4	10.4	1	11.5	1	11.5	
^t PHL	CLK	Q	C _L = 50 pF		6.4	10.4	1	11.5	1	11.5	ns
^t PZH	ŌĒ	Q	C: - 50 pF		7.3	11.2	1	12.5	1	12.5	no
^t PZL	OE	Q	$C_L = 50 pF$		7.3	11.2	1	12.5	1	12.5	ns
^t PHZ	ŌĒ	Q	C: - 50 pF		7	11.2	1	12	1	12	no
t _{PLZ}	OE	٧	C _L = 50 pF		7	11.2	1	12	1	12	ns
^t sk(o)			C _L = 50 pF			1***				1	ns

^{**} On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 5 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^{\circ}\text{C}$ (see Note 4)

	PARAMETER	SN7	374	UNIT	
	PARAMETER	MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.8	1.2	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.8	-1.2	V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}	3.8			V
VIH(D)	High-level dynamic input voltage	2			V
V _{IL(D)}	Low-level dynamic input voltage			0.8	V

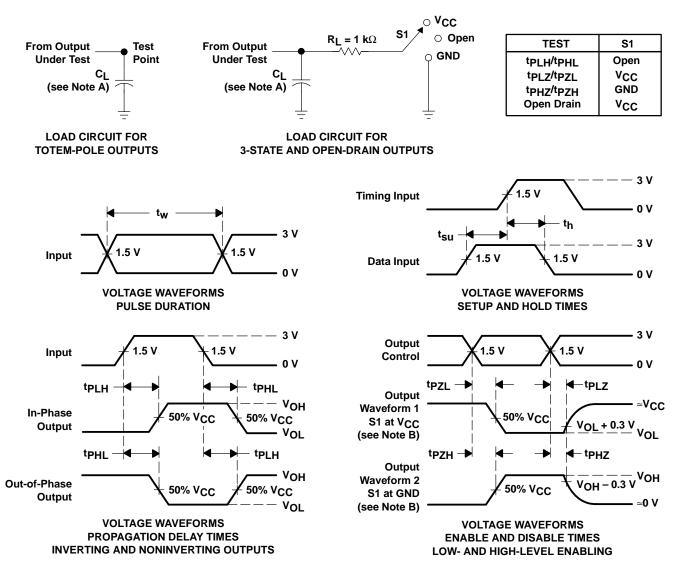
NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST C	ONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load,	f = 1 MHz	27	pF

^{***} On products compliant to MIL-PRF-38535, this parameter does not apply.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq 3$ ns. $t_f \leq 3$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms





5-Sep-2011

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-9686501Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9686501QRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
5962-9686501QSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
SN74AHCT374DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	
SN74AHCT374DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT374DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT374DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT374DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT374DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT374DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT374DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT374DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT374DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT374N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AHCT374NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AHCT374PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT374PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT374PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT374PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	
SN74AHCT374PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



5-Sep-2011

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74AHCT374PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AHCT374PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54AHCT374FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54AHCT374J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SNJ54AHCT374W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54AHCT374, SN74AHCT374:

Catalog: SN74AHCT374



5-Sep-2011

• Military: SN54AHCT374

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT374DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHCT374DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74AHCT374PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT374DBR	SSOP	DB	20	2000	346.0	346.0	33.0
SN74AHCT374DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74AHCT374PWR	TSSOP	PW	20	2000	346.0	346.0	33.0

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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