## SN54F374, SN74F374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SDFS077A - D2932, MARCH 1987 - REVISED OCTOBER 1993

- Eight D-Type Flip-Flops in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

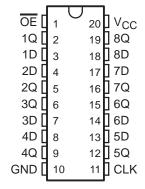
#### description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

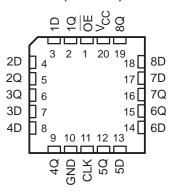
The eight flip-flops of the 'F374 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

SN54F374 . . . J PACKAGE SN74F374 . . . DB, DW, OR N PACKAGE (TOP VIEW)



SN54F374 . . . FK PACKAGE (TOP VIEW)



The output enable  $(\overline{OE})$  input does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74F374 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54F374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74F374 is characterized for operation from 0°C to 70°C.

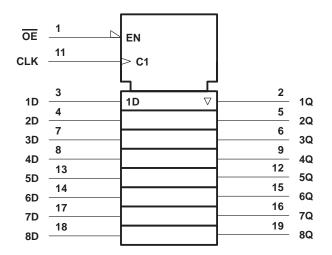
# FUNCTION TABLE (each flip-flop)

		INPUTS		OUTPUT
O	Ε	CLK	D	Q
		1	Н	Н
	L	$\uparrow$	L	L
	L	H or L	Χ	$Q_0$
H	1	Х	Χ	Z

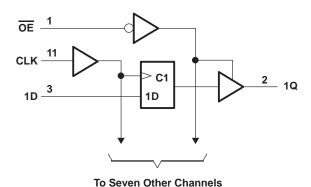


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## logic symbol†



## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>		
Input voltage range, V <sub>I</sub> (see Note 1) .		
Input current range		–30 mA to 5 mA
Voltage range applied to any output in	the disabled or power-off state .	
Voltage range applied to any output in	the high state	$-0.5 \text{ V to V}_{\text{CC}}$
Current into any output in the low state	: SN54F374	40 mA
	SN74F374	48 mA
Operating free-air temperature range:	SN54F374	–55°C to 125°C
	SN74F374	0°C to 70°C
Storage temperature range		65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

		S	N54F374	4	S	N74F374	1	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			8.0	V
lıK	Input clamp current			-18			-18	mA
ІОН	High-level output current			-3			-3	mA
IOL	Low-level output current			20			24	mA
TA	Operating free-air temperature	-55		125	0		70	°C



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## SN54F374, SN74F374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			S	N54F37	4	S	N74F374	1	
PARAMETER	TES	ST CONDITIONS	MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
VIK	$V_{CC} = 4.5 \text{ V},$	I <sub>I</sub> = –18 mA			-1.2			-1.2	V
	V 45V	$I_{OH} = -1 \text{ mA}$	2.5	3.4		2.5	3.4		
Voн	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -3 \text{ mA}$	2.4	3.3		2.4	3.3		V
	$V_{CC} = 4.75 \text{ V},$	$I_{OH} = -1 \text{ mA to } -3 \text{ mA}$				2.7			
V	V 45V	I <sub>OL</sub> = 20 mA		0.3	0.5				V
V <sub>OL</sub>	$V_{CC} = 4.5 \text{ V}$	I <sub>OL</sub> = 24 mA					0.35	0.5	V
lozh	V <sub>CC</sub> = 5.5 V,	$V_0 = 2.7 \text{ V}$			50			50	μΑ
lozL	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V			-50			-50	μΑ
lį	V <sub>CC</sub> = 5.5 V,	$V_I = 7 V$			0.1			0.1	mA
lіН	$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = 2.7 V			20			20	μΑ
I <sub>IL</sub>	$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = 0.5 V			- 0.6			- 0.6	mA
los <sup>‡</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0	-60		-150	-60		-150	mA
ICCZ	V <sub>CC</sub> = 5.5 V,	See Note 2		55	86		55	86	mA

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

#### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V <sub>CC</sub> = T <sub>A</sub> = 'F3	25°C	SN54	F374	SN74	F374	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		0	100	0	60	0	70	MHz
	Pode a dometica	CLK high	7		7		7		
t <sub>W</sub>	Pulse duration	CLK low	6		6		6		ns
	Octor for a data before OUKA	High	2		2.5		2		
t <sub>su</sub>	Setup time, data before CLK↑	Low	2		2		2		ns
4.	Hold time data after OLKA	High	2		2		2		
th	Hold time, data after CLK↑	Low	2		2.5		2		ns

<sup>‡</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. NOTE 2: I<sub>CCZ</sub> is measured with  $\overline{\text{OE}}$  at 4.5 V and all other inputs grounded.

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## switching characteristics (see Note 3)

PARAMETER	PARAMETER FROM (INPUT)		C <sub>I</sub> R <sub>I</sub>	$V_{CC} = 5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = 25^{\circ}C$			$V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX <sup>†</sup>			
				′F374		SN54	F374	SN74	F374	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			100			60		70		MHz
<sup>t</sup> PLH	CLK	Q	3.2	6.1	8.5	3.2	10.5	3.2	10	
<sup>t</sup> PHL	CLK	α	3.2	6.1	8.5	3.2	11	3.2	10	ns
<sup>t</sup> PZH	ŌĒ	0	1.2	8.6	11.5	1.2	14	1.2	12.5	
t <sub>PZL</sub>	OE	Q	1.2	5.4	7.5	1.2	10	1.2	8.5	ns
<sup>t</sup> PHZ	ŌĒ	0	1.2	4.9	7	1.2	8	1.2	8	ns
tPLZ	OE	Q	1.2	3.9	5.5	1.2	7.5	1.2	6.5	110

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. NOTE 3: Load circuits and waveforms are shown in Section 1.



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#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-9759001Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9759001QRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
5962-9759001QRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
5962-9759001QSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
5962-9759001QSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
JM38510/34105B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/34105B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/34105BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
JM38510/34105BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
JM38510/34105BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	
JM38510/34105BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	
M38510/34105B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/34105B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/34105BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
M38510/34105BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
M38510/34105BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	
M38510/34105BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	
SN54F374J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SN54F374J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SN74F374DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	
SN74F374DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	
SN74F374DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F374DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F374DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F374DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F374DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74F374DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F374DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F374DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F374DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F374DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F374DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F374DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F374DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F374DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F374DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F374DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F374DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F374DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F374N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74F374N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74F374N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	
SN74F374N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	
SN74F374NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74F374NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74F374NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	





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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74F374NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F374NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F374NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F374NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74F374NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54F374FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54F374FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54F374J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SNJ54F374J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SNJ54F374W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	
SNJ54F374W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



## **PACKAGE OPTION ADDENDUM**

25-Jan-2012

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#### OTHER QUALIFIED VERSIONS OF SN54F374, SN74F374:

Military: SN54F374

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications



#### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F374DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74F374DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74F374NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1





\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F374DBR	SSOP	DB	20	2000	346.0	346.0	33.0
SN74F374DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74F374NSR	SO	NS	20	2000	346.0	346.0	41.0

## 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# W (R-GDFP-F20)

## CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

## PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

#### **28 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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