

Dual-Channel, 10-/12-Bit, 500-MSPS Digital-to-Analog Converters (DACs)

Check for Samples: DAC3152, DAC3162

FEATURES

- Low Power: 270 mW at 500 MSPS
- LVDS Input Data Bus
 - Interleaved DDR Data Load
- High DC Accuracy: ±0.25 LSB DNL (10-bit),
 ± 0.5 LSB INL (12-bit)
- Low Latency: 1.5 Clock Cycles
- Simple Control: No Software Required
- Differential Scalable Output: 2 mA to 20 mA
- On-Chip 1.2-V Reference
- 1.8-V and 3.3-V DC Supplies
- Space Saving Package: 48-pin 7-mm x 7-mm QFN

APPLICATIONS

- Cellular Base Stations
- Wideband Communications
- Medical Instrumentation
- Test and Measurement

DESCRIPTION

The DAC3152/DAC3162 is a low-power, low-latency, high-dynamic-range, dual-channel, 10-/12-bit, pin-compatible family of digital-to-analog converters (DACs) with a sample rate as high as 500 MSPS.

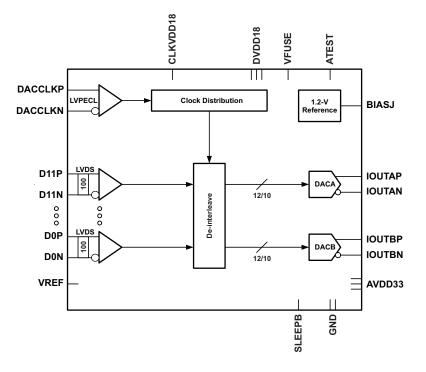
The device simplicity (no software required), low latency, and low power simplify the design of complex systems. The DACs interface seamlessly with the high-performance TRF370333 analog quadrature modulator for direct upconversion architectures.

Digital data for both DAC channels is interleaved through a single LVDS data bus with on-chip termination. The high input rate of the devices allows the processing of wide-bandwidth signals.

The devices are characterized for operation over the entire industrial temperature range of -40° C to 85° C and are available in a small 48-pin 7-mm × 7-mm QFN package.

The low power, small size, speed, superior crosstalk, simplicity, and low latency of the DAC3152/DAC3162 make them an attractive fit for a variety of applications.

FUNCTIONAL BLOCK DIAGRAM



A

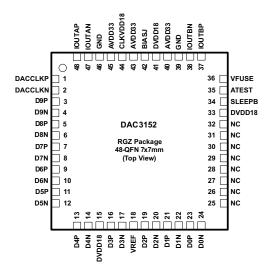
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DAC3152 PINOUT AND PIN FUNCTIONS

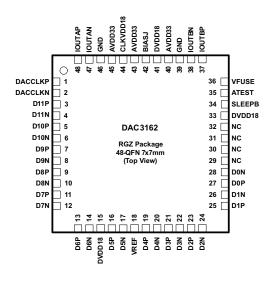


PIN FUNCTIONS

	PIN		DESCRIPTION						
NAME	NO.	1/0	DESCRIPTION						
ATEST	35	0	Factory use only. Leave unconnected for normal operation.						
AVDD33	40, 43, 45	-	Analog supply voltage (3.3 V)						
BIASJ	42	0	Full-scale output current bias. For 20-mA full-scale output current, connect a 960-Ω resistor to GND.						
CLKVDD18	44	-	Internal clock buffer supply voltage (1.8 V) This supply can be shared with DIGVDD18.						
D[90]P	3, 5, 7, 9, 11, 13,	ı	LVDS positive-input data bits 0 through 9. Each positive/negative LVDS pair has an internal 100-Ω termination resistor. Data format relative to DACCLKP/N clock is double data rate (DDR) with two data transfers per DACCLKP/N clock cycle. Dual-channel data is interleaved on this bus.						
	16, 19, 21, 23		D9P is most-significant data bit (MSB) – pin 3						
			D0P is least-significant data bit (LSB) – pin 23						
	4, 6, 8, 10, 12,		LVDS negative-input data bits 0 through 9. (See D[9:0]P description)						
D[90]N	14, 17, 20, 22,	1	D9N is most-significant data bit (MSB) – pin 4						
	24		D0N is least-significant data bit (LSB) – pin 24						
DACCLKP	1	I	Positive external LVPECL clock input with a self-bias of approximately CLKVDD18/2. Input data is latched on both edges of DACCLKP/N (double data rate). The LVPECL clock signal should be AC coupled.						
DACCLKN	2	I	Complementary external LVPECL clock input (see the DACCLKP description). The LVPECL clock signal should be AC coupled.						
DVDD18	15, 33, 41	_	Digital supply voltage (1.8 V). This supply can be shared with CLKVDD18.						
GND	39, 46, Thermal pad	-	Pins 39 and 46 and the thermal pad located on the bottom of the QFN package are ground for all supplies.						
IOUTAP	48	0	A-channel DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full-scale current sink and the least-positive voltage on the IOUTAP pin. Similarly, a 0x3FF data input results in a 0-mA current sink and the most-positive voltage on the IOUTAP pin.						
IOUTAN	47	0	A-channel DAC complementary current output. IOUTAN has the opposite behavior of the IOUTAP described for IOUTAP. An input data value of 0x0000 results in a 0-mA sink and the most-positive voltage on the IOUTAN pin.						
IOUTBP	37	0	B-channel DAC current output. See the IOUTAP description.						
IOUTBN	38	0	B-channel DAC complementary current output. See the IOUTAN description.						
NC	25–32	_	No connect. Leave unconnected for normal operation.						
SLEEPB	34	1	Connect to GND to put the device in sleep mode or to AVDD for active mode. Internal pullup						
VFUSE	36	-	Digital supply voltage (1.8 V). This supply pin is also used for factory fuse programming. Connect to DVDD18 pins for normal operation.						
VREF	18	I/O	Factory use only. Connect to a 0.1-µF decoupling capacitor to GND.						



DAC3162 PINOUT AND PIN FUNCTIONS



PIN FUNCTIONS

	PIN								
NAME	NO.	1/0	DESCRIPTION						
ATEST	35	0	Factory use only. Leave unconnected for normal operation.						
AVDD33	40, 43, 45	-	Analog supply voltage (3.3 V)						
BIASJ	42	0	Full-scale output current bias. For 20-mA full-scale output current, connect a 960-Ω resistor to GND.						
CLKVDD18	44	-	Internal clock buffer supply voltage (1.8 V) This supply can be shared with DIGVDD18.						
D[110]P	3, 5, 7, 9, 11, 13, 16, 19, 21, 23,	_	LVDS positive-input data bits 0 through 11. Each positive/negative LVDS pair has an internal 100-Ω termination resistor. Data format relative to DACCLKP/N clock is double data rate (DDR) with two data transfers per DACCLKP/N clock cycle. Dual channel data is interleaved on this bus.						
	25, 27		D11P is most-significant data bit (MSB) – pin 3						
			D0P is least-significant data bit (LSB) – pin 27						
	4, 6, 8, 10, 12,		LVDS negative-input data bits 0 through 11. (See D[11:0]P description)						
D[110]N	14, 17, 20, 22,	- 1	D11N is most-significant data bit (MSB) – pin 4						
	24, 26, 28		D0N is least-significant data bit (LSB) – pin 28						
DACCLKP	1	I	Positive external LVPECL clock input with a self-bias of approximately CLKVDD18/2. Input data is latched on both edges of DACCLKP/N (double data rate). The LVPECL clock signal should be AC coupled.						
DACCLKN	2	1	Complementary external LVPECL clock input (see the DACCLKP description). The LVPECL clock signal should be AC coupled.						
DVDD18	15, 33, 41	-	Digital supply voltage (1.8 V) This supply can be shared with CLKVDD18.						
GND	39, 46, Thermal pad	-	Pins 39, 46 and the thermal pad located on the bottom of the QFN package are ground for all supplies.						
IOUTAP	48	0	A-channel DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full-scale current sink and the least-positive voltage on the IOUTAP pin. Similarly, a 0xFFF data input results in a 0-mA current sink and the most-positive voltage on the IOUTAP pin.						
IOUTAN	47	0	A-channel DAC complementary current output. IOUTAN has the opposite behavior of the IOUTAP described for IOUTAP. An input data value of 0x0000 results in a 0-mA sink and the most-positive voltage on the IOUTAN pin.						
IOUTBP	37	0	B-channel DAC current output. See the IOUTAP description.						
IOUTBN	38	0	B-channel DAC complementary current output. See the IOUTAN description.						
NC	25–32	-	No connect. Leave unconnected for normal operation.						
SLEEPB	34	_	Connect to GND to put the device in sleep mode or to AVDD for active mode. Internal pullup.						
VFUSE	36	-	Digital supply voltage (1.8 V). This supply pin is also used for factory fuse programming. Connect to DVDD18 pins for normal operation.						
VREF	18	I/O	Factory use only. Connect to a 0.1-µF decoupling capacitor to GND.						



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		V	ALUE	LINUT
		MIN	MAX 2.3 2.3 4 DVDD18 + 0.5 CLKVDD18 + 0.5 V AVDD33 + 0.7 V AVDD33 + 0.7 V ±20 ±30 85 150	UNII
	DVDD18, CLKVDD18	-0.5	2.3	V
Supply-voltage range ⁽²⁾	VFUSE	-0.5	2.3	V
	AVDD33	-0.5 2.3 -0.5 2.3 -0.5 4 -0.5 4 -0.5 DVDD18 + 0.5 -0.5 CLKVDD18 + 0.5 V -0.5 AVDD33 + 0.7 V -1 AVDD33 + 0.7 V ±20 ±30 -40 85	4	V
	D[110]P/N	-0.5	DVDD18 + 0.5	V
Pin-voltage range ⁽²⁾	DACCLKP/N	-0.5	CLKVDD18 + 0.5 V	V
Pin-voitage range	BIASJ, SLEEPB	-0.5	AVDD33 + 0.7 V	V
	IOUTAP/N, IOUTBP/N	MIN MAX -0.5 2.3 V -0.5 2.3 V -0.5 4 V -0.5 DVDD18 + 0.5 V -0.5 CLKVDD18 + 0.5 V -0.5 AVDD33 + 0.7 V V -1 AVDD33 + 0.7 V V ±20 m ±30 m -40 85	V	
Peak input current (any i	nput)		±20	mA
Peak total input current (all inputs)		±30	mA
Operating free-air tempe	rature range, T _A	-40	−40 85 °C	
Storage temperature ran	ge, T _{stg}	-65	150	°C

⁽¹⁾ Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

	THERMAL METRIC ⁽¹⁾⁽²⁾	DAC3152 DAC3162	UNIT
		RGZ (48 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	28.9	
θ_{JCtop}	Junction-to-case (top) thermal resistance	14.9	
θ_{JB}	Junction-to-board thermal resistance	5.62	90/11/
Ψлт	Junction-to-top characterization parameter	0.3	°C/W
ΨЈВ	Junction-to-board characterization parameter	5.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.7	

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

⁽²⁾ Measured with respect to GND

⁽²⁾ For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.



ELECTRICAL CHARACTERISTICS – DC SPECIFICATION

DVDD18 = CLKVDD18 = 1.8 V, AVDD33 = 3.3 V, f_{DAC} = 500 MSPS, f_{OUT} = 1 MHz over recommended operating free-air temperature range, IOUT_{FS} = 20 mA (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	0	AC3152		DAC3162			UNIT
	PARAMETER	1EST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	
Resolution			10			12			Bits
DC ACCURA	ACY								
DNL	Differential nonlinearity			±0.1			±0.4		LSB
INL	Integral nonlinearity			±0.15			±0.5		LSB
ANALOG OL	JTPUT ⁽¹⁾								
	Gain error			±1.6			±1.6		%FSR
	Gain mismatch			±0.2			±0.2		%FSR
	Full-scale output current		2		20	2		20	mA
	Output compliance range		AVDD - 0.5	,	AVDD + 0.5	AVDD - 0.5		AVDD + 0.5	V
	Output resistance			300			300		kΩ
	Output capacitance			5			5		pF
REFERENCE	E								
V _{REF}	Internal reference voltage		1.14	1.2	1.26	1.14	1.2	1.26	V
TEMPERATI	URE COEFFICIENTS								
	Gain drift			±60			±60		ppm/°C
	Reference-voltage drift			±41			±41		ppm/°C
POWER SUF	PPLY	,			*				
	AVDD33		3	3.3	3.6	3	3.3	3.6	V
	CLKVDD18, DVDD18		1.7	1.8	1.9	1.7	1.8	1.9	V
PSRR	Power-supply rejection ratio	DC tested		±0.1			±0.1		%FSR/V
POWER COI	NSUMPTION								
		f _{DAC} = 500 MSPS, f _{OUT} = 10 MHz		270	310		278	320	mW
P _{DIS}	Power dissipation	Power-down mode: no clock, DAC on sleep mode, static data pattern		16	23		17	25	mW
I _(AVDD33)	Analog supply current			55	65		56	65	mA
I _(DVDD18) I _(CLKVDD)	Digital and clock supply current			50	55		53	63	mA
	Operating range		-40	25	85	-40	25	85	°C

⁽¹⁾ Measured differentially across IOUTAP/N or IOUTBP/N with 25 Ω each to AVDD.



ELECTRICAL CHARACTERISTICS – DIGITAL SPECIFICATIONS

DVDD18 = CLKVDD18 = 1.8 V, AVDD33 = 3.3 V, f_{DAC} = 500 MSPS, f_{OUT} = 1 MHz over recommended operating free-air temperature range, IOUT_{FS} = 20 mA (unless otherwise noted)

	DADAMETED	TEST COMPITIONS		DAC3152		DAC3162			UNIT	
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNII	
LVDS INP	UTS: DIGITAL INPUT DATA ⁽¹⁾	!			•					
$V_{A,B+}$	Logic-high differential input voltage threshold		150	400		150	400		mV	
$V_{A,B-}$	Logic-low differential input voltage threshold			-400	-150		-400	-150	mV	
V _{COM}	Input common mode		0.9	1.2	1.5	0.9	1.2	1.5	V	
Z _T	Internal termination		85	110	135	85	110	135	Ω	
C _L	LVDS input capacitance			2			2		pF	
f _{INTERL}	Interleaved LVDS data rate				1000			1000	MSPS	
f _{DATA}	Input data rate (per DAC)			·	500			500	MSPS	
CLOCK IN	PUT: DACCLKP/N									
	Duty cycle		40%		60%	40%		60%		
	Differential voltage		0.2	1		0.2	1		V	
	Clock frequency			·	500			500	MHz	
CMOS INT	ERFACE: SLEEPB		•		•			•		
V _{IH}	High-level input voltage		2			2			V	
V _{IL}	Low-level input voltage				0.8			0.8	V	
I _{IH}	High-level input current		-40	·	40	-40		40	μA	
I _{IL}	Low-level input current		-40		40	-40		40	μA	
Cı	CMOS Input capacitance			2			2		pF	
DIGITAL IN	NPUT DATA TIMING SPECIFICATIONS: DO	JBLE EDGE LATCHING								
t _{s(DATA)}	Setup time, valid to either edge of DACCLKP/N		200			200			ps	
t _{h(DATA)}	Hold time, valid after either edge of DACCLKP/N		200			200			ps	

⁽¹⁾ See LVDS INPUTS section for terminology.



ELECTRICAL CHARACTERISTICS – AC SPECIFICATIONS

 $DVDD18 = CLKVDD18 = 1.8 \text{ V, AVDD33} = 3.3 \text{ V, } \\ f_{DAC} = 500 \text{ MSPS, } \\ f_{OUT} = 1 \text{ MHz over recommended operating free-air temperature range, } \\ IOUT_{FS} = 20\text{mA (unless otherwise noted)} \\$

	DADAMETER	TECT COMPITIONS	D.	AC3152		DAC3162				
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT	
ANALOG O	UTPUT (1)	'			'					
f _{DAC}	Maximum DAC rate		500			500			MSPS	
t _{s(DAC)}	Output settling time to 0.1%	Transition: Code 0x0000 to 0xFFFF		10			10		ns	
t _{r(IOUT)}	Output rise time, 10% to 90%			220			220		ps	
$t_{f(IOUT)}$	Output fall time, 90% to 10%			220			220		ps	
	Latency			1.5			1.5		DAC clock cycles	
Power-up	DAC wake-up time	IOUT current settling to 1% of IOUT _{FS} .		2			2		μs	
time	DAC sleep time	IOUT current settling to less than 1% of IOUT _{FS} .		2			2		μs	
AC PERFOR	RMANCE ⁽²⁾									
		f_{DAC} = 500 MSPS, f_{OUT} = 10 MHz		78			79			
SFDR	Spurious-free dynamic range, single tone at 0 dBFS	f_{DAC} = 500 MSPS, f_{OUT} = 20 MHz		74			74		dBc	
		f _{DAC} = 500 MSPS, f _{OUT} = 70 MHz		59			60			
		f_{DAC} = 500 MSPS, f_{OUT} = 10 ± 0.5 MHz		91			93			
IMD3	Third-order two-tone intermodulation distortion, each tone at –12 dBFS	f _{DAC} = 500 MSPS, f _{OUT} = 20 ± 0.5 MHz		85			86		dBc	
		f _{DAC} = 500 MSPS, f _{OUT} = 70 ± 0.5 MHz		62			62			
NSD	Noise spectral density, single tone at	f_{DAC} = 500 MSPS, f_{OUT} = 10 MHz		-145			-155		dDo/Lla	
NOD	0 dBFS	f_{DAC} = 500 MSPS, f_{OUT} = 70 MHz		-140			-140		dBc/Hz	
ACLR ⁽³⁾	Adjacent-channel leakage ratio,	f _{DAC} = 491.52 MSPS, f _{OUT} = 30 MHz		68			76		-10 -	
	single carrier	f _{DAC} = 491.52 MSPS, f _{OUT} = 70 MHz		67			70		dBc	
	Channel isolation	f _{DAC} = 500 MSPS, f _{OUT} = 10 MHz		90			90		dBc	

Measured differentially across IOUTAP/N or IOUTBP/N with 25 Ω each to AVDD.

 ^{(2) 4:1} transformer output termination, 50-Ω doubly terminated load.
 (3) Single carrier, W-CDMA with 3.84 MHz BW, 5-MHz spacing, centered at IF, PAR = 12 dB. TESTMODEL 1, 10 ms



Typical Characteristics

 $DVDD18 = CLKVDD18 = 1.8 \text{ V, AVDD33} = 3.3 \text{ V, } \\ f_{DAC} = 500 \text{ MSPS, } \\ f_{OUT} = 1 \text{ MHz, } \\ I_{OUTfs} = 20 \text{ mA (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz, } \\ I_{OUTfs} = 20 \text{ mA (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz, } \\ I_{OUTfs} = 20 \text{ mA (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz, } \\ f_{OUT} = 1 \text{ M$

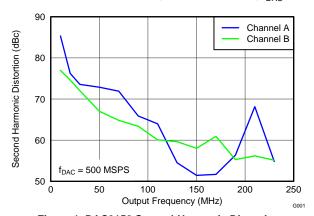


Figure 1. DAC3152 Second-Harmonic Distortion vs Frequency

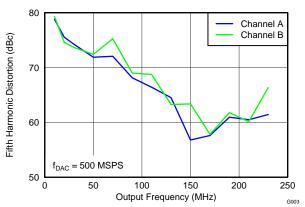


Figure 3. DAC3152 Fifth-Harmonic Distortion vs Frequency

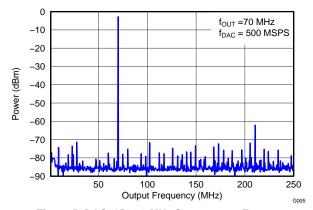


Figure 5. DAC3152 70-MHz Spectrum vs Frequency

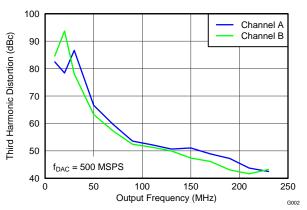


Figure 2. DAC3152 Third-Harmonic Distortion vs Frequency

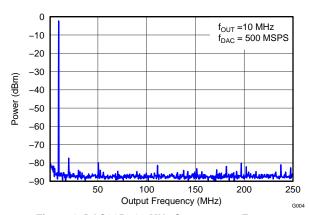


Figure 4. DAC3152 10-MHz Spectrum vs Frequency

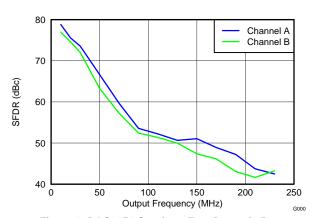


Figure 6. DAC3152 Spurious-Free Dynamic Range vs Frequency



DVDD18 = CLKVDD18 = 1.8 V, AVDD33 = 3.3 V, f_{DAC} = 500 MSPS, f_{OUT} = 1 MHz, I_{OUTfs} = 20 mA (unless otherwise noted)

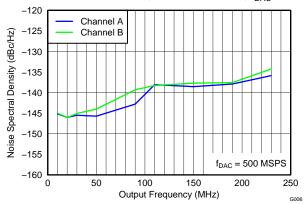


Figure 7. DAC3152 Noise Spectral Density vs Frequency

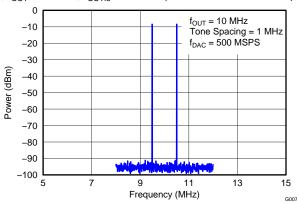


Figure 8. DAC3152 10-MHz Two-Tone Spectrum vs Frequency

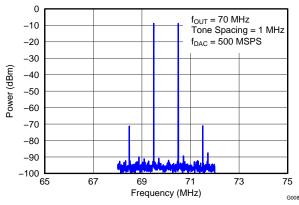


Figure 9. DAC3152 70-MHz Two-Tone Spectrum vs Frequency

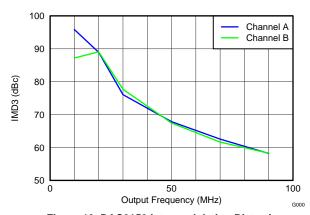


Figure 10. DAC3152 Intermodulation Distortion vs Frequency

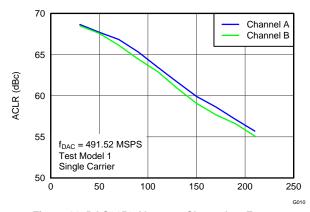


Figure 11. DAC3152 Alternate Channel vs Frequency

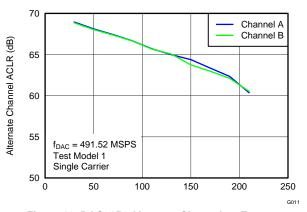


Figure 12. DAC3152 Alternate Channel vs Frequency



 $DVDD18 = CLKVDD18 = 1.8 \text{ V}, \text{ AVDD33} = 3.3 \text{ V}, \text{ } \\ f_{DAC} = 500 \text{ MSPS}, \text{ } \\ f_{OUT} = 1 \text{ MHz}, \text{ } \\ I_{OUTfs} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz}, \text{ } \\ I_{OUTfs} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz}, \text{ } \\ I_{OUTfs} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz}, \text{ } \\ I_{OUTfs} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz}, \text{ } \\ I_{OUTfs} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz}, \text{ } \\ I_{OUTfs} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz}, \text{ } \\ I_{OUTfs} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz}, \text{ } \\ I_{OUTfs} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz}, \text{ } \\ I_{OUTfs} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz}, \text{ } \\ I_{OUTfs} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz}, \text{ } \\ I_{OUTfs} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz}, \text{ } \\ I_{OUTfs} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz}, \text{ } \\ I_{OUTfs} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz}, \text{ } \\ I_{OUTfs} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz}, \text{ } \\ I_{OUTfs} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz}, \text{ } \\ I_{OUTfs} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz}, \text{ } \\ I_{OUTfs} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz}, \text{ } \\ I_{OUTfs} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz}, \text{ } \\ I_{OUTfs} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 1 \text{ MHz}, \text{ } \\ I_{OUTfs} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ f_{OUT} = 20 \text{ mA} \text{ (u$

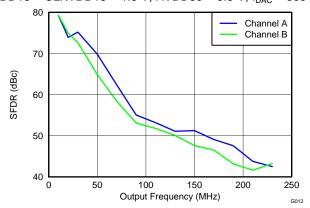


Figure 13. DAC3162 Spurious-Free Dynamic Range vs Frequency

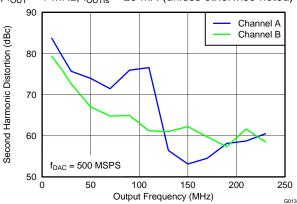


Figure 14. DAC3162 Second-Harmonic Distortion vs Frequency

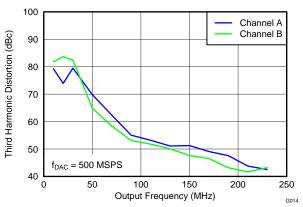


Figure 15. DAC3162 Third-Harmonic Distortion vs Frequency

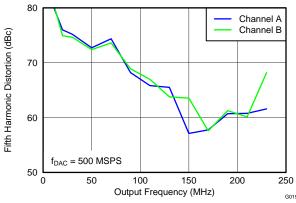


Figure 16. DAC3162 Fifth-Harmonic Distortion vs Frequency

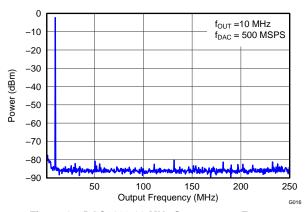


Figure 17. DAC3162 10-MHz Spectrum vs Frequency

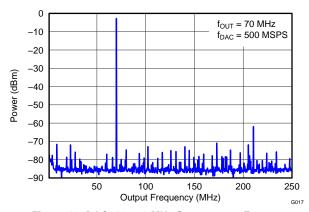


Figure 18. DAC3162 70-MHz Spectrum vs Frequency



DVDD18 = CLKVDD18 = 1.8 V, AVDD33 = 3.3 V, f_{DAC} = 500 MSPS, f_{OUT} = 1 MHz, I_{OUTfs} = 20 mA (unless otherwise noted)

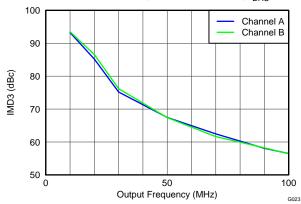


Figure 19. DAC3152 Intermodulation Distortion vs Frequency

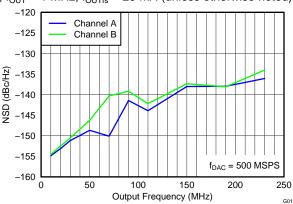


Figure 20. DAC3162 Noise Spectral Density vs Frequency

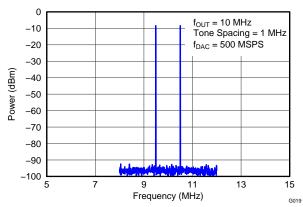


Figure 21. DAC3162 10-MHz Two-Tone Spectrum vs Frequency

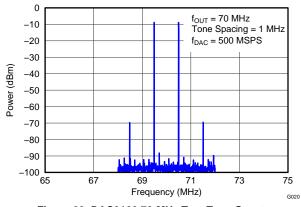


Figure 22. DAC3162 70-MHz Two-Tone Spectrum vs Frequency

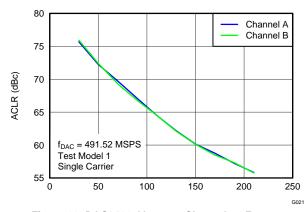


Figure 23. DAC3162 Alternate Channel vs Frequency

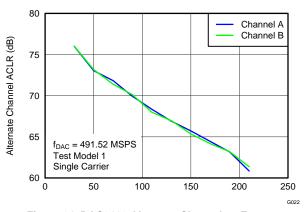


Figure 24. DAC3162 Alternate Channel vs Frequency



 $DVDD18 = CLKVDD18 = 1.8 \text{ V}, \text{ AVDD33} = 3.3 \text{ V}, \text{ } \\ f_{DAC} = 500 \text{ MSPS}, \text{ } \\ f_{OUT} = 1 \text{ MHz}, \text{ } \\ I_{OUTfs} = 20 \text{ mA} \text{ (unless otherwise noted)} \\ I_{OUTfs} = 20$

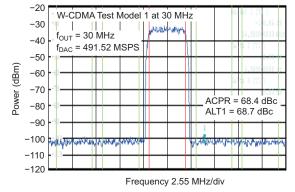


Figure 25. DAC3152 30-MHz WCDMA vs Frequency

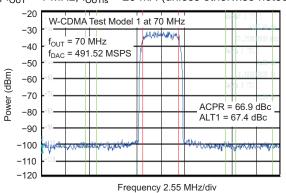


Figure 26. DAC3152 70-MHz WCDMA vs Frequency

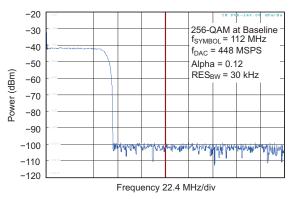


Figure 27. DAC3152 QAM vs Frequency

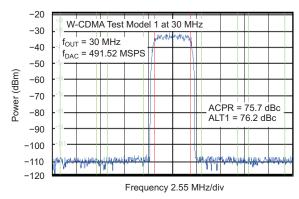


Figure 28. DAC3162 30-MHz WCDMA vs Frequency

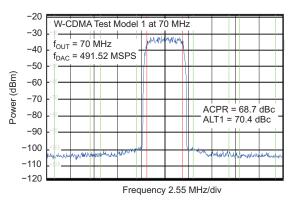


Figure 29. DAC3162 70-MHz WCDMA vs Frequency

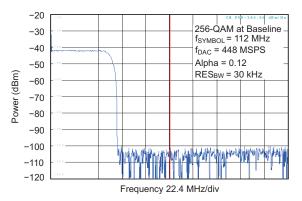


Figure 30. DAC3162 QAM vs Frequency



DEFINITION OF SPECIFICATIONS

Adjacent-Carrier Leakage Ratio (ACLR): Defined for a 3.84-Mcps 3GPP W-CDMA input signal measured in a 3.84-MHz bandwidth at a 5-MHz offset from the carrier with a 12-dB peak-to-average ratio.

Analog and Digital Power-Supply Rejection Ratio (APSRR, DPSRR): Defined as the percentage error in the ratio of the delta IOUT and delta supply voltage normalized with respect to the ideal IOUT current.

Differential Nonlinearity (DNL): Defined as the variation in analog output associated with an ideal 1-LSB change in the digital input code.

Gain Drift: Defined as the maximum change in gain, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

Gain Error: Defined as the percentage error (in FSR%) for the ratio between the measured full-scale output current and the ideal full-scale output current.

Integral Nonlinearity (INL): Defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Intermodulation Distortion (IMD3): The two-tone IMD3 is defined as the ratio (in dBc) of the third-order intermodulation distortion product to either fundamental output tone.

Offset Drift: Defined as the maximum change in dc offset, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

Offset Error: Defined as the percentage error (in FSR%) for the ratio between the measured mid-scale output current and the ideal mid-scale output current.

Output Compliance Range: Defined as the minimum and maximum allowable voltage at the output of the current-output DAC. Exceeding this limit may result in reduced reliability of the device or adversely affecting distortion performance.

Reference Voltage Drift: Defined as the maximum change of the reference voltage in ppm per degree Celsius from the value at ambient (25°C) to values over the full operating temperature range.

Noise Spectral Density (NSD): Defined as the difference of power (in dBc) between the output tone signal power and the noise floor of 1 Hz bandwidth within the first Nyquist zone, excluding harmonics.

Signal-to-Noise Ratio (SNR): Defined as the ratio of the rms value of the fundamental output signal to the RMS sum of all other spectral components below the Nyquist frequency, including noise, but excluding the first six harmonics and dc.



DATA INTERFACE

The parallel-port data interface to the device consists of a single LVDS bus that accepts interleaved A and B data with up to 12-bit resolution. Data is sampled by the LVPECL double-data-rate (DDR) clock DACCLK. DACCLK is additionally used for the data conversion process, and hence a low-jitter source is recommended. Setup and hold requirements must be met for proper sampling.

The interleaved data for channels A and B is interleaved in the form A0, B0, A1, B1... into the data bus. Data into the device is formatted according to the diagram shown in Figure 31.

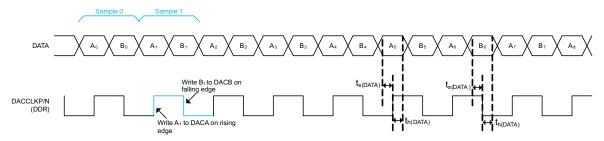


Figure 31. Data Transmission Format

CLOCK INPUT

The DAC clock (DACCLKP/N) is an internally biased differential input that for optimal performance should be driven by a low-jitter clock source. The DACCLK signal is used for both data latching (in DDR format) and as the data conversion clock. Figure 32 shows an equivalent circuit for the DAC input clock.

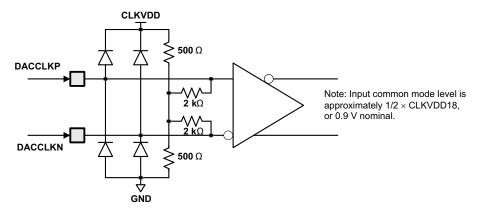


Figure 32. DACCLKP/N Equivalent Input Circuit



The preferred configuration for driving the DACCLK input consists of a differential ECL/PECL source as shown in Figure 33. Although not optimal due to the limited signal swing, an LVDS source can also be used to drive the clock input.

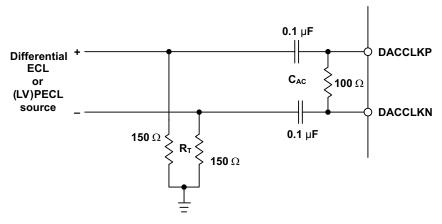


Figure 33. Preferred Clock Input Configuration With a Differential ECL/PECL Clock Source

A single-ended clock, such as a clean sinusoid or a 1.8 V LVCMOS signal (for low-rate operation), can also be used to drive the clock if configured as in the input circuits of Figure 34 and Figure 35.

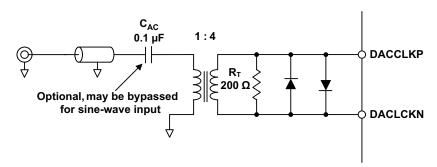


Figure 34. Clock Input Configuration Using 50-Ω Cable Input

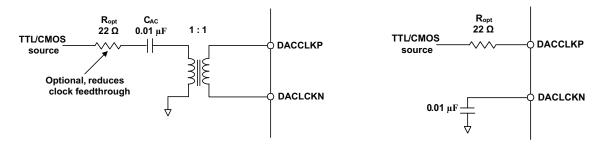


Figure 35. Clock Input Configuration With a Single-Ended TTL/CMOS Clock



DATA INPUTS

The input data LVDS pairs (D[11:0]P/N) have the input configuration shown in Figure 36. Figure 37 shows the typical input levels and common-mode voltage used to drive these inputs.

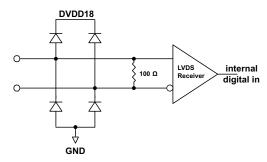


Figure 36. D[13:0]P/N LVDS Input Configuration

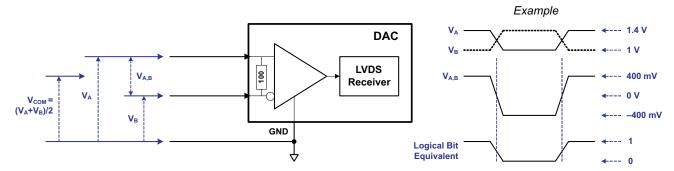


Figure 37. LVDS Data Input Levels

Table 1.

Applied	Applied Voltages Resulting Differential Voltage			Logical Bit Binary Equivalent	
V_{A}	V _B	V _{A,B}	V _{COM}	biliary Equivalent	
1.4 V	1 V	400 mV	4.0.1/	1	
1 V	1.4 V	–400 mV	1.2 V	0	
1.2 V	0.8 V	400 mV	4.1/	1	
0.8 V	1.2 V	–400 mV	1 V	0	

CMOS INPUT

Figure 38 shows a schematic of the SLEEPB equivalent CMOS digital inputs. See the specification table for logic thresholds. The pullup circuitry is approximately equivalent to 100 k Ω .

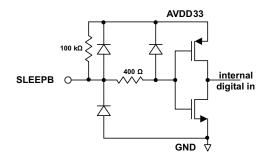


Figure 38. SLEEPB Digital Equivalent Input



REFERENCE OPERATION

The DAC3152/DAC3162 uses a band-gap reference and control amplifier for biasing the full-scale output current. The full-scale output current is set by applying an external resistor R_{BIAS} to pin BIASJ. The bias current I_{BIAS} through resistor R_{BIAS} is defined by the on-chip band-gap reference voltage and control amplifier. The default full-scale output current equals 16 times this bias current and can thus be expressed as:

$$IOUT_{FS} = 16 \times I_{BIAS} = 16 \times V_{BG} / R_{BIAS}$$

The band-gap reference voltage delivers an accurate voltage of 1.2 V. The full-scale output current can be adjusted from 20 mA down to 2 mA by varying resistor RBIAS. The internal control amplifier has a wide input range, supporting the full-scale output current range of 20 dB. The recommended value for R_{BIAS} is 960 Ω , which results in a full-scale output current of 20 mA.

DAC TRANSFER FUNCTION

The DAC outputs of the DAC3152/DAC3162 consist of a segmented array of NMOS current sinks, capable of sinking a full-scale output current up to 20 mA. Differential current switches direct the current to either one of the complementary output nodes IOUTP or IOUTN. Complementary output currents enable differential operation, thus canceling out common-mode noise sources (digital feed-through, on-chip and PCB noise), dc offsets, and even-order distortion components, and increasing signal output power by a factor of four.

The full-scale output current is set using external resistor R_{BIAS} in combination with an on-chip band-gap voltage reference source (1.2 V) and control amplifier. Current I_{BIAS} through resistor R_{BIAS} is mirrored internally to provide a maximum full-scale output current equal to 16 times I_{BIAS} .

The relation between IOUTP and IOUTN can be expressed as:

Current flowing into a node is denoted as – current, and current flowing out of a node as + current. Because the output stage is a current sink, the current flows from AVDD33 into the IOUTP and IOUTN pins. The output current flow in each pin driving a resistive load can be expressed as:

$$IOUTP = IOUT_{FS} \times ((2^N - 1) - CODE) / 2^N$$

 $IOUTN = IOUT_{FS} \times CODE / 2^N$

where CODE is the decimal representation of the DAC data input word and N is the DAC bit resolution.

For the case where IOUTP and IOUTN drive resistor loads R_L directly, this translates into single-ended voltages at IOUTP and IOUTN:

```
VOUTP = AVDD - | IOUTP | \times R_L
VOUTN = AVDD - | IOUTN | \times R_L
```

Assuming that the data is full scale (2^N-1) in offset binary notation) and the R_L is 25 Ω , the differential voltage between pins IOUTP and IOUTN can be expressed as:

```
VOUTP = AVDD - | - 0 mA | \times 25 \Omega = 3.3 V
VOUTN = AVDD - | -20 mA | \times 25 \Omega = 2.8 V
VDIFF = VOUTP - VOUTN = 0.5 V
```

Note that care should be taken not to exceed the compliance voltages at nodes IOUTP and IOUTN, which would lead to increased signal distortion.



ANALOG CURRENT OUTPUTS

The DAC outputs can be easily configured to drive a doubly terminated $50-\Omega$ cable using a properly selected RF transformer. Figure 39 and Figure 40 show the $50-\Omega$ doubly terminated transformer configuration with 1:1 and 4:1 impedance ratios, respectively. Note that the center tap of the primary input of the transformer must be connected to AVDD to enable a dc current flow. Applying a 20-mA full-scale output current leads to a 0.5-Vpp output for a 1:1 transformer and a 1-Vpp output for a 4:1 transformer. The low dc impedance between IOUTP or IOUTN and the transformer center tap sets the center of the ac signal to AVDD, so the 1-Vpp output for the 4:1 transformer results in an output between AVDD – 0.5 V and AVDD + 0.5 V.

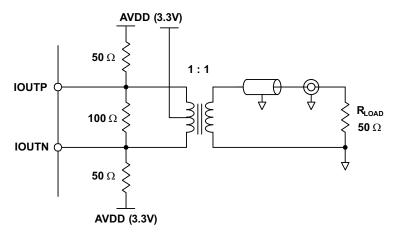


Figure 39. Driving a Doubly Terminated 50-Ω Cable Using a 1:1 Impedance-Ratio Transformer

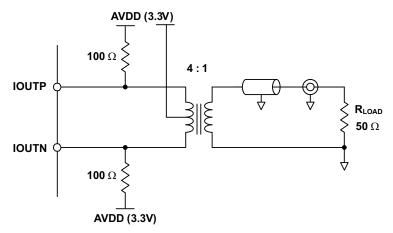


Figure 40. Driving a Doubly Terminated 50-Ω Cable Using a 4:1 Impedance-Ratio Transformer



PASSIVE INTERFACE TO ANALOG QUADRATURE MODULATORS

A common application in communication systems is to interface the DAC to an IQ modulator like the TRF3703 family of modulators from Texas Instruments. The input of the modulator is generally of high impedance and requires a specific common-mode voltage. A simple resistive network can be used to maintain $50-\Omega$ load impedance for the DAC3152/DAC3162 and also provide the necessary common-mode voltages for both the DAC and the modulator.

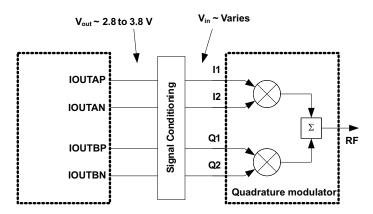


Figure 41. DAC3152/DAC3162 to Analog Quadrature Modulator Interface

The DAC3152/DAC3162 has a maximum 20-mA full-scale output and a voltage compliance range of AVDD \pm 0.5 V. The TRF3703 IQ modulator family has three common-mode voltage options: 1.5 V, 1.7 V, and 3.3 V, and the TRF370417 IQ modulator has a 1.7-V common mode.

Figure 42 shows the recommended passive network to interface the DAC to the TRF370317, which has a common-mode voltage of 1.7 V. The network generates the 3.3-V common mode required by the DAC output and 1.7 V at the modulator input, while still maintaining a $50-\Omega$ load for the DAC.

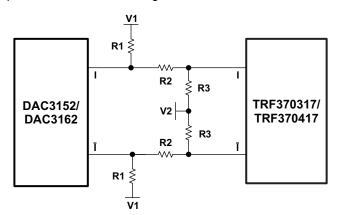


Figure 42. DAC3152/DAC3162 to TRF370317 or TRF370417 Interface

If V1 is set to 5 V and V2 is set to -5 V, the corresponding resistor values are R1 = 57 Ω , R2 = 80 Ω , and R3 = 336 Ω . The loss developed through R2 is about -1.86 dB. When there is no -5-V supply available and V2 is set to 0 V, the resistor values are R1 = 66 Ω , R2 = 101 Ω , and R3 = 107 Ω . The loss with these values is -5.76 dB.

Figure 43 shows the recommended network for interfacing with the TRF370333, which requires a common mode of 3.3 V. This is the simplest interface, as there is no voltage shift. With V1 = 5 V and V2 = 0 V, the resistor values are R1 = 66Ω and R3 = 208Ω .

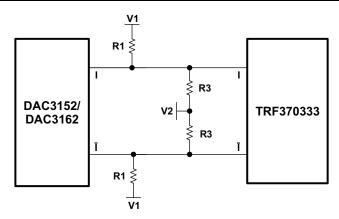


Figure 43. DAC3152/DAC3162 to TRF370333 Interface

In most applications, a baseband filter is required between the DAC and the modulator to eliminate the DAC images. This filter can be placed after the common-mode biasing network. For the DAC-to-modulator network shown in Figure 44, R2 and the filter load R4 must be considered into the DAC impedance. The filter must be designed for the source impedance created by the resistor combination of R3 || (R2 + R1). The effective impedance seen by the DAC is affected by the filter termination resistor, resulting in R1 || (R2 + R3 || (R4/2)).

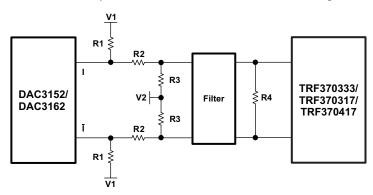


Figure 44. DAC to Modulator Interface With Filter

Factoring in R4 into the DAC load, a typical interface to the TRF370317 with V1 = 5 V and V2 = 0 V results in the following values: R1 = 72 Ω , R2 = 116 Ω , R3 = 124 Ω and R4 = 150 Ω . This implies that the filter must be designed for 75- Ω input and output impedance (single-ended impedance). The common-mode levels for the DAC and modulator are maintained at 3.3 V and 1.7 V, and the DAC load is 50 Ω . The added load of the filter termination causes the signal to be attenuated by -10.8 dB.

A filter can be implemented in a similar manner to interface with the TRF370333. In this case, it is much simpler to balance the loads and common-mode voltages, due to the absence of R2. An added benefit is that there is no loss in this network. With V1 = 5 V and V2 = 0 V, the network can be designed such that R1 = 115 Ω , R3 = 681 Ω , and R4 = 200 Ω . This results in a filter impedance of R1 || R2 = 100 Ω , and a DAC load of R1 || R3 || (R4/2), which is equal to 50 Ω . R4 is a differential resistor and does not affect the common-mode level created by R1 and R3. The common-mode voltage is set at 3.3 V for a full-scale current of 20 mA.

For more information on how to interface the DAC3152/DAC3162 to an analog quadrature modulator, see the application reports *Passive Terminations for Current Output DACs* (SLAA399) and *Design of Differential Filters for High-Speed Signal Chains* (SLWA053).



POWER-UP SEQUENCE

The following start-up sequence is recommended to power up the DAC3152/DAC3162:

- Supply 1.8 V to DVDD18 and CLKVDD18 simultaneously, and 3.3 V to AVDD33. Within AVDD33, the
 multiple AVDD33 pins should be powered up simultaneously. The 1.8-V and 3.3-V supplies can be powered
 up simultaneously or in any order.
 - There are no specific requirements on the ramp rate for the supplies.
- Provide the DAC clock to the DACCLKP/N inputs.
- Toggle the SLEEPB pin for a minimum 25-ns low pulse duration.
- Provide the LVDS data inputs.

REVISION HISTORY

Cł	nanges from Original (November 2010) to Revision A	Page
<u>.</u>	Deleted the DAC3172 device	1
Cł	nanges from Revision A (November 2010) to Revision B	Page
•	Changed Feature bullet From: High DC Accuracy: ±1 LSB DNL, ±2 LSB INL To: High DC Accuracy: ±0.25 LSB DNI (10-bit), ± 0.5 LSB INL (12-bit)	
•	Added text "The LVPECL clock signal should be AC coupled" to Pin DACCLKP and DACCLKN descriptions	2
•	Added text "The LVPECL clock signal should be AC coupled" to Pin DACCLKP and DACCLKN descriptions	3
•	Added values to the Thermal Information table	4
•	Changed the ELECTRICAL CHARACTERISTICS – DC SPECIFICATION table	5
•	Added Min and Max values to V _{COM} - Internal common mode	6
•	Added Min and Max values to Z _T - Internal termination	<mark>6</mark>
•	Changed the AC Performance Typical values for DAC3152 and DAC3162	
•	Added the Typical Characteristics section	8
<u>•</u>	Replaced Signal to Noise Ratio (SNR) with Noise Spectral Density (NSD)	13
Cl	nanges from Revision B (December 2011) to Revision C	Page
•	Changed the CLOCK INPUT: DACCLKP/N - Differential voltage MIN value From: 0.4V To: 0.2V for both devices	6
•	Deleted Note 2 From the DIGITAL SPECIFICATIONS table- Driving the clock input with a differential voltage lower than 1 V results in degraded performance.	6





25-Feb-2012

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
DAC3152IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DAC3152IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DAC3162IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DAC3162IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

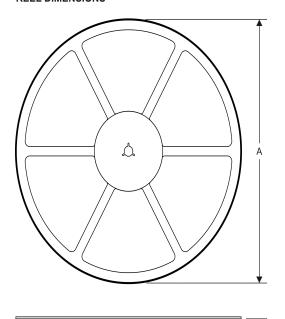
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

www.ti.com 24-Feb-2012

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

All differsions are norminal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC3152IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
DAC3152IRGZT	VQFN	RGZ	48	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
DAC3162IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
DAC3162IRGZT	VQFN	RGZ	48	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

www.ti.com 24-Feb-2012



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC3152IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
DAC3152IRGZT	VQFN	RGZ	48	250	336.6	336.6	28.6
DAC3162IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
DAC3162IRGZT	VQFN	RGZ	48	250	336.6	336.6	28.6



- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-220.



4206354-5/R 08/11

RGZ (S-PVQFN-N48)

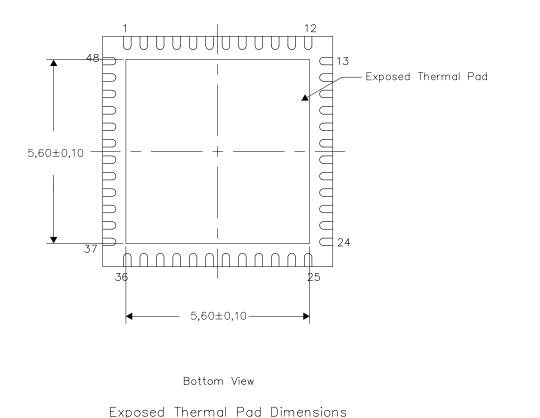
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

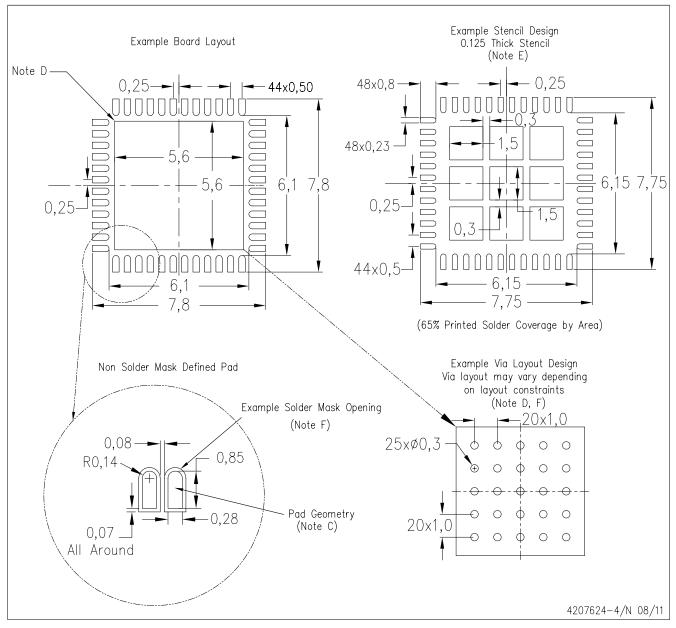


NOTE: All linear dimensions are in millimeters



RGZ (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com https://www.ti.com.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

Applications

Automotive and Transportation www.ti.com/automotive

e2e.ti.com

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

		•	
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video

RFID <u>www.ti-rfid.com</u>
OMAP Mobile Processors www.ti.com/omap

Products

Audio

Wireless Connectivity www.ti.com/wirelessconnectivity

www.ti.com/audio

TI E2E Community Home Page

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2012, Texas Instruments Incorporated