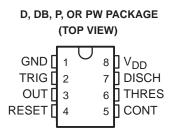
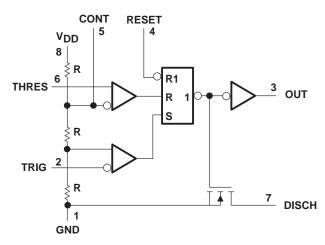
- **Very Low Power Consumption** 1 mW Typ at $V_{DD} = 5 \text{ V}$
- Capable of Operation in Astable Mode
- **CMOS Output Capable of Swinging Rail**
- **High Output-Current Capability** Sink 100 mA Tvp Source 10 mA Typ
- **Output Fully Compatible With CMOS, TTL,** and MOS
- **Low Supply Current Reduces Spikes During Output Transitions**
- Single-Supply Operation From 1 V to 15 V
- Functionally Interchangeable With the **NE555: Has Same Pinout**
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883C, Method 3015.2

description

The TLC551 is a monolithic timing circuit fabricated using the TI LinCMOS™ process. The



functional block diagram



RESET can override TRIG, which can override THRES.

timer is fully compatible with CMOS, TTL, and MOS logic and operates at frequencies up to 2 MHz. Compared to the NE555 timer, this device uses smaller timing capacitors because of its high input impedance. As a result, more accurate time delays and oscillations are possible. Power consumption is low across the full range of power supply voltage.

Like the NE555, the TLC551 has a trigger level equal to approximately one-third of the supply voltage and a threshold level equal to approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal (CONT). When the trigger input (TRIG) falls below the trigger level, the flip-flop is set and the output goes high. If TRIG is above the trigger level and the threshold input (THRES) is above the threshold level, the flip-flop is reset and the output is low. The reset input (RESET) can override all other inputs and can be used to initiate a new timing cycle. If RESET is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between DISCH and GND. All unused inputs should be tied to an appropriate logic level to prevent false triggering.

While the CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the TLC551 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE555.

The TLC551C is characterized for operation from 0°C to 70°C.



This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either supply voltage or ground. Specific guidelines for handling devices of this type are contained in the publication Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies available from Texas Instruments.

LinCMOS is a trademark of Texas Instruments Incorporated.



AVAILABLE OPTIONS

		PACKA	AGED DEVICES			
TA	V _{DD} RANGE	SMALL OUTLINE (D)	SSOP (DB)	PLASTIC DIP (P)	TSSOP (PW)	CHIP FORM (Y)
0°C to 70°C	1 V to 16 V	TLC551CD	TLC551CDBLE	TLC551CP	TLC551CPWLE	TLC551Y

The D package is available taped and reeled. Add the suffix R (e.g., TLC551CDR). The DB and PW packages are only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TLC551CDBLE). Chips are tested at 25°C.

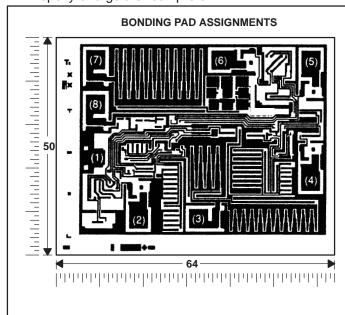
FUNCTION TABLE

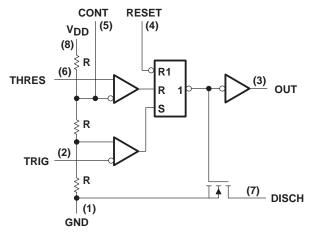
RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<min< td=""><td>Irrelevant</td><td>Irrelevant</td><td>Low</td><td>On</td></min<>	Irrelevant	Irrelevant	Low	On
>MAX	<min< td=""><td>Irrelevant</td><td colspan="2">Irrelevant High O</td></min<>	Irrelevant	Irrelevant High O	
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<min< td=""><td colspan="2">As previously established</td></min<>	As previously established	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

TLC551Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC551. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.





RESET can override TRIG, which can override THRES.

CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

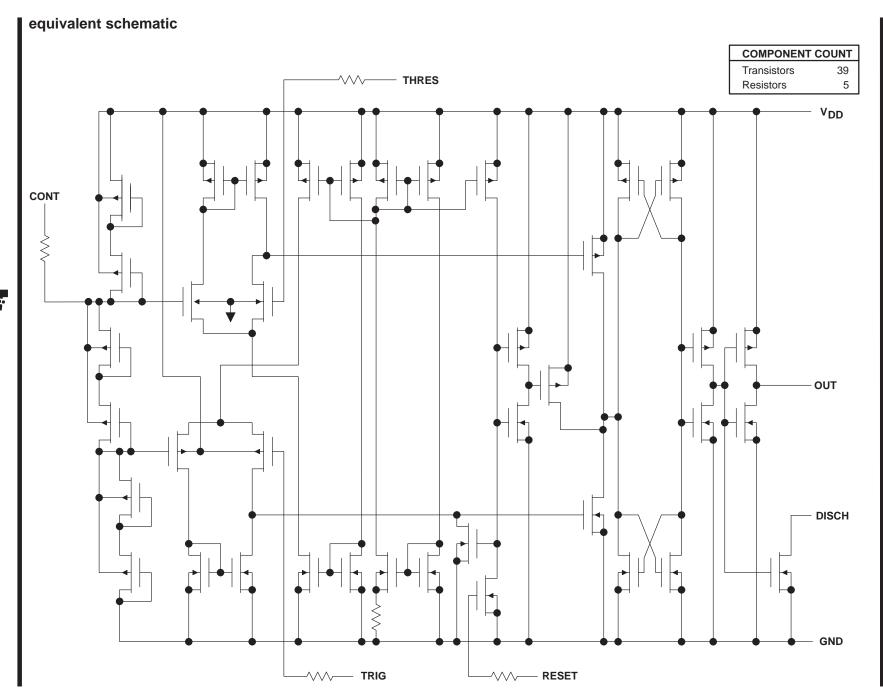
T_Jmax = 150°C

TOLERANCES ARE $\pm 10\%$.

ALL DIMENSIONS ARE IN MILS.

PIN (1) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.





SLFS044B - FEBRUARY 1984 - REVISED SEPTEMBER 1997

TLC551, TLC551Y LinCMOS™ TIMERS SLFS044B - FEBRUARY 1984 - REVISED SEPTEMBER 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{DD} (see Note 1)	
Input voltage range, V _I (any input)	0.3 to V _{DD}
Sink current, discharge or output	150 mĀ
Source current, output, I _O	15 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Operating free-air temperature range	

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network GND.

DISSIPATION RATING TABLE

PACKAGE	$T_{\mbox{\scriptsize A}} \le 25^{\circ}\mbox{\scriptsize C}$ POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW
DB	525 mW	4.2 mW/°C	336 mW
Р	1000 mW	8.0 mW/°C	640 mW
PW	525 mW	4.2 mW/°C	336 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V _{DD}	1	15	V
Operating free-air temperature range, T _A	0	70	°C



electrical characteristics at specified free-air temperature, $V_{\mbox{DD}}$ = 1 V

	PARAMETER	TEST CONDITIONS	T _A †	MIN	TYP	MAX	UNIT	
VIT	Threshold voltage		25°C	0.475	0.67	0.85	V	
٧١١	Threshold voltage		Full range	0.45		0.875	·	
ΙΙΤ	Threshold current		25°C		10		pА	
'11	Threshold current		70°C		75		PΛ	
VI(TRIG)	Trigger voltage		25°C	0.15	0.33	0.425	V	
VI(TRIG)	Thigger voltage		Full range	0.1		0.45	V	
li(TDIO)	Trigger current		25°C		10		pА	
l(TRIG)	rngger current		70°C		75		PΛ	
\/\\\DE0ET\	Reset voltage		25°C	0.4	0.7	1	V	
VI(RESET)	Neset voltage		Full range	0.3		1	Ů	
lupeoet)	Reset current		25°C		10		pА	
I(RESET)	Neset current		70°C		75		PΛ	
	Control voltage (open circuit) as a percentage of supply voltage		70°C		66.7%			
	Discharge switch on-stage voltage	ΙΟΙ = 100 μΑ	25°C		0.02	0.15	V	
	Discharge switch on-stage voltage	100 μΑ	Full range			0.2	V	
	Discharge switch off-stage voltage		25°C		0.1		nA	
	Discharge switch on-stage voltage		70°C		0.5		na I	
Vон	High-level output voltage	I _{OH} = -10 μA	25°C	0.6	0.98		V	
VOH	High-level output voltage		Full range	0.6			v	
VOL	Low-level output voltage	I _{OL} = 100 μA	25°C		0.03	0.2	V	
*OL	Low level output voltage	10L = 100 μΑ	Full range			0.25	v	
IDD	Supply current	See Note 2	25°C		15	100	μΑ	
טטין	очрру очноп	300 NOIO 2	Full range			150	μΑ	

[†] Full range is 0°C to 70°C.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.

electrical characteristics at specified free-air temperature, $V_{DD} = 2 V$

	PARAMETER	TEST CONDITIONS	T _A †	MIN	TYP	MAX	UNIT	
\/. -	Threshold voltage		25°C	0.95	1.33	1.65	V	
VIT	Theshold voltage		Full range	0.85		1.75	V	
1	Threshold current		25°C		10		pА	
ΊΤ	Threshold current		70°C		75		PΑ	
V _I (TDIO)	Trigger voltage		25°C	0.4	0.67	0.95	V	
VI(TRIG)	Trigger voltage		Full range	0.3		1.05	V	
luttoro)	Trigger current		25°C		10		pА	
l(TRIG)	rrigger current		70°C		75		PΑ	
\/\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	Reset voltage		25°C	0.4	1.1	1.5	V	
VI(RESET)	Reset voltage		Full range	0.3		1.8	V	
lupeoet)	Reset current		25°C		10		pА	
I(RESET)	Reset current		70°C		75		PΑ	
	Control voltage (open circuit) as a percentage of supply voltage		70°C		66.7%			
	Discharge quitab en etera valtage	1 m A	25°C		0.03	0.2	V	
	Discharge switch on-stage voltage	I _{OL} = 1 mA	Full range			0.25	V	
	Discharge quitab off store valtage		25°C		0.1		nA	
	Discharge switch off-stage voltage		70°C		0.5		IIA	
V	High-level output voltage	Jan - 200 u A	25°C	1.5	1.9		V	
VOH	riign-ievel output voitage	I _{OH} = -300 μA	Full range	1.5			V	
\/o.	Low-level output voltage	lou – 1 mA	25°C		0.07	0.3	V	
VOL	Low-level output voltage	I _{OL} = 1 mA	Full range			0.35	V	
Inn	Supply current	See Note 2	25°C		65	250], [
IDD	очрріу сипепі	See Note 2	Full range			400	μΑ	

[†] Full range is 0°C to 70°C.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.



electrical characteristics at specified free-air temperature, $V_{DD} = 5 \text{ V}$

	PARAMETER	TEST CONDITIONS	T _A †	MIN	TYP	MAX	UNIT
\/	Threshold voltage		25°C	2.8	3.3	3.8	V
VIT	meshold voltage		Full range	2.7		3.9	V
li-	Threshold current		25°C		10		pА
ΙΙΤ	The should current		70°C		75		PΛ
\/(\TD(0)	Trigger voltage		25°C	1.36	1.66	1.96	V
VI(TRIG)	mgger voltage		Full range	1.26		2.06	V
li/TDIC)	Trigger current		25°C		10		pА
l(TRIG)	rrigger current		70°C		75		PΛ
VI(RESET)	Reset voltage		25°C	0.4	1.1	1.5	V
VI(RESET)	Neset voltage		Full range	0.3		1.8	V
l(RESET)	Reset current		25°C		10		pА
"I(KESET)	Neget current		70°C		75		P ² ·
	Control voltage (open circuit) as a percentage of supply voltage		70°C		66.7%		
	Discharge switch on stage voltage	lo 10 m/	25°C		0.14	0.5	V
	Discharge switch on-stage voltage	I _{OL} = 10 mA	Full range			0.6	V
	Discharge switch off-stage voltage		25°C		0.1		nA
	Discharge switch on-stage voltage		70°C		0.5		IIA
VOH	High-level output voltage	I _{OH} = -1 mA	25°C	4.1	4.8		V
VOH	Tigit level output voltage	IOH - TIIIA	Full range	4.1			V
		I _{OL} = 8 mA	25°C		0.21	0.4	
		IOL = 0 IIIA	Full range			0.5	
VOL	Low-level output voltage	I _{OL} = 5 mA	25°C		0.13	0.3	V
V OL	Low level output voltage	IOL = 3 IIIA	Full range			0.4	
		I _{OL} = 3.2 mA	25°C		0.08	0.3	
		10L = 3.2 IIIA	Full range			0.35	
Inn	Supply current	See Note 2	25°C		170	350	μΑ
IDD	очрру синент	OGG NOTE 2	Full range			500	μΛ

[†]Full range is 0°C to 70°C.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

	PARAMETER	TEST CONDITIONS	T _A †	MIN	TYP	MAX	UNIT
\/	Throbald voltage		25°C	9.45		10.55	V
VIT	Threshold voltage		Full range	9.35		10.65	V
1	Threehold surrent		25°C		10		A
lΤ	Threshold current		70°C		75		pА
\/.(==\c)	Trigger veltage		25°C	4.65	5	5.35	V
VI(TRIG)	Trigger voltage		Full range	4.55		5.45	V
li(TDIO)	Trigger current		25°C		10		pА
l(TRIG)	riigger current		70°C		75		pΑ
VI(RESET)	Reset voltage		25°C	0.4	1.1	1.5	V
VI(RESET)	Neset voltage		Full range	0.3		1.8	V
lupeoet)	Reset current		25°C		10		pА
I(RESET)	Neset Current		70°C		75		PΛ
	Control voltage (open circuit) as a percentage of supply voltage		70°C		66.7%		
	Discharge quitch on stone voltage	1 100 mA	25°C		0.77	1.7	V
	Discharge switch on-stage voltage	I _{OL} = 100 mA	Full range			1.8	V
	Discharge quitab off stage voltage		25°C		0.1		nA
	Discharge switch off-stage voltage		70°C		0.5		IIA
		I _{OH} = -10 mA	25°C	12.5	14.2		
		10H = - 10 IIIA	Full range	12.5			
Vон	High-level output voltage	I _{OH} = -5 mA	25°C	13.5	14.6		V
VOH	riigii-ievei output voitage	10H = -3 IIIA	Full range	13.5			V
		I _{OH} = -1 mA	25°C	14.2	14.9		
		IOH = = 1 IIIA	Full range	14.2			
		I _{OL} = 100 mA	25°C		1.28	3.2	
		IOL = 100 IIIA	Full range			3.6	
Voi	Low-level output voltage	I _{OL} = 50 mA	25°C		0.63	1	V
VOL	Low-level output voltage	IOL = 30 IIIA	Full range			1.3	
		I _{OL} = 10 mA	25°C		0.12	0.3	
		10L = 10 111A	Full range			0.4	
IDD	Supply current	See Note 2	25°C		360	600	μΑ
† Full rongo is		OCC NOTE 2	Full range			800	μΛ

[†] Full range is 0°C to 70°C.

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Initial error of timing interval‡	$V_{DD} = 5 \text{ V to } 15 \text{ V},$	$R_A = R_B = 1 \text{ k}\Omega \text{ to } 100 \text{ k}\Omega,$		1%	3%	
	Supply voltage sensitivity of timing interval	C _T = 0.1 μF, See Note 3			0.1	0.5	%/V
t _r	Rise time, output pulse	$R_{I} = 10 M\Omega$	C _I = 10 pF		20	75	no
tf	Fall time, output pulse	K[= 10 10152,	CL = 10 pr		15	60	ns
f _{max}	Maximum frequency in astable mode	$R_A = 470 \Omega,$ $C_T = 200 pF$	$R_B = 200 \Omega$, See Note 3	1.2	1.8		MHz

[‡] Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process

NOTE 3: R_A , R_B , and C_T are as defined in Figure 3.



electrical characteristics at V_{DD} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIT	Threshold voltage		2.8	3.3	3.8	V
ΙΙΤ	Threshold current			10		рА
V _I (TRIG)	Trigger voltage		1.36	1.66	1.96	V
I _I (TRIG)	Trigger current			10		pА
V _I (RESET)	Reset voltage		0.4	1.1	1.5	V
I(RESET)	Reset current			10		pА
	Control voltage (open circuit) as a percentage of supply voltage			66.7%		
	Discharge switch on-state voltage	I _{OL} = 10 mA		0.14	0.5	V
	Discharge switch off-state current			0.1		nA
Vон	High-level output voltage	I _{OH} = – 1 mA	4.1	4.8		V
		I _{OL} = 8 mA		0.21	0.4	
VOL	Low-level output voltage	$I_{OL} = 5 \text{ mA}$		0.13	0.3	V
		I _{OL} = 3.2 mA		0.08	0.3	
I_{DD}	Supply current	See Note 2		170	350	μΑ

NOTE 2: These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.

TYPICAL CHARACTERISTICS

DISCHARGE SWITCH ON-STATE RESISTANCE vs

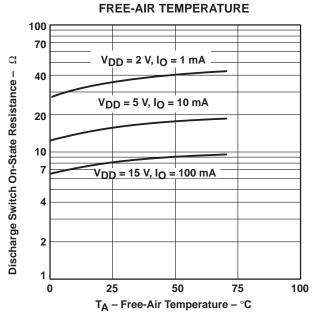


Figure 1

PROPAGATION DELAY TIMES (TO DISCHARGE OUTPUT FROM TRIGGER AND THRESHOLD SHORTED TOGETHER)

SUPPLY VOLTAGE

SUPPLY VOLTAGE

SUPPLY VOLTAGE

IO(on) ≥ 1 mA
CL ≈ 0
TA = 25°C

The state of th

Figure 2

8

10 12 14

V_{DD} – Supply Voltage – V



0 2

18 20

[‡]The effects of the load resistance on these values must be taken into account separately.

APPLICATION INFORMATION

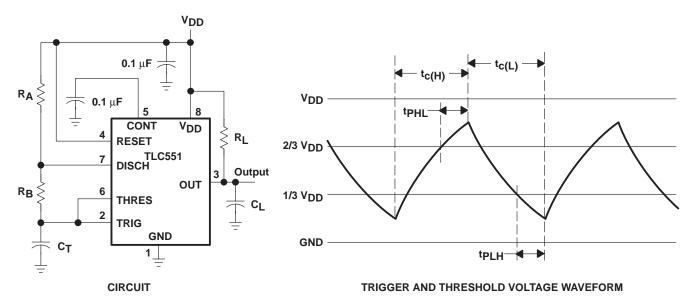


Figure 3. Astable Operation

Connecting TRIG to THRES, as shown in Figure 3, causes the timer to run as a multivibrator. The capacitor C_T charges through R_A and R_B to the threshold voltage level (approximately 0.67 V_{DD}) and then discharges through R_B only to the value of the trigger voltage level (approximately 0.33 V_{DD}). The output is high during the charging cycle ($t_{C(L)}$) and low during the discharge cycle ($t_{C(L)}$). The duty cycle is controlled by the values of R_A , and R_B , and C_T , as shown in the equations below.

$$\begin{array}{l} t_{c(H)} \approx C_T \; (R_A \, + \, R_B) \; \text{In 2} \; \; (\text{In 2} = 0.693) \\ t_{c(L)} \approx C_T \; R_B \; \text{In 2} \\ \text{Period} = t_{c(H)} \, + \, t_{c(L)} \approx C_T \; (R_A \, + \, 2R_B) \; \text{In 2} \\ \text{Output driver duty cycle} = \frac{t_{c(L)}}{t_{c(H)} \, + \, t_{c(L)}} \approx 1 - \frac{R_B}{R_A \, + \, 2R_B} \\ \text{Output waveform duty cycle} = \frac{t_{c(H)}}{t_{c(H)} \, + \, t_{c(L)}} \approx \frac{R_B}{R_A \, + \, 2R_B} \end{array}$$

The 0.1-μF capacitor at CONT in Figure 3 decreases the period by about 10%.

The formulas shown above do not allow for any propagation delay times from TRIG and THRES to DISCH. These delay times add directly to the period and create differences between calculated and actual values that increase with frequency. In addition, the internal on-state resistance r_{on} during discharge adds to R_{B} to provide another source of timing error in the calculation when R_{B} is very low or r_{on} is very high.

APPLICATION INFORMATION

The equations below provide better agreement with measured values.

$$t_{c(H)} = C_{T} (R_{A} + R_{B}) \ln \left[3 - \exp\left(\frac{-t_{PLH}}{C_{T} (R_{B} + r_{on})}\right) \right] + t_{PHL}$$

$$t_{c(L)} = C_{T} (R_{B} + r_{on}) \ln \left[3 - \exp\left(\frac{-t_{PHL}}{C_{T} (R_{A} + R_{B})}\right) \right] + t_{PLH}$$

These equations and those given earlier are similar in that a time constant is multiplied by the logarithm of a number or function. The limit values of the logarithmic terms must be between In 2 at low frequencies and In 3 at extremely high frequencies. For a duty cycle close to 50%, an appropriate constant for the logarithmic terms can be substituted

with good results. Duty cycles less than 50% $\frac{t_{c(H)}}{t_{c(H)}+t_{c(L)}}$ require that $\frac{t_{c(H)}}{t_{c(L)}}$ <1 and possibly R_A \leq r_{on}. These

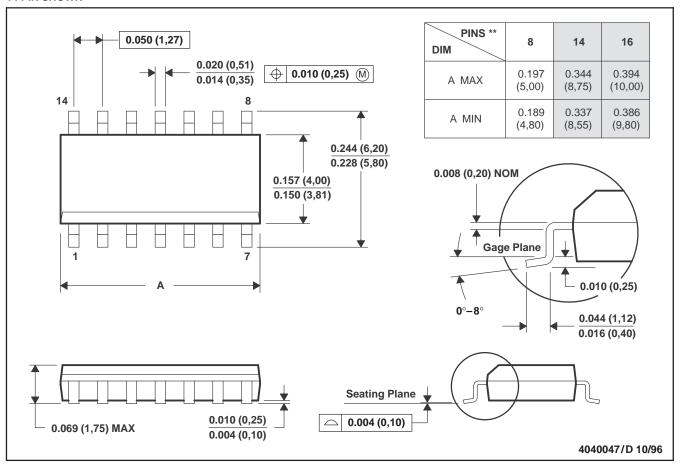
conditions can be difficult to obtain.

In monostable applications, the trip point of the trigger input can be set by a voltage applied to CONT. An input voltage between 10% and 80% of the supply voltage from a resistor divider with at least 500-µA bias provides good results.

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



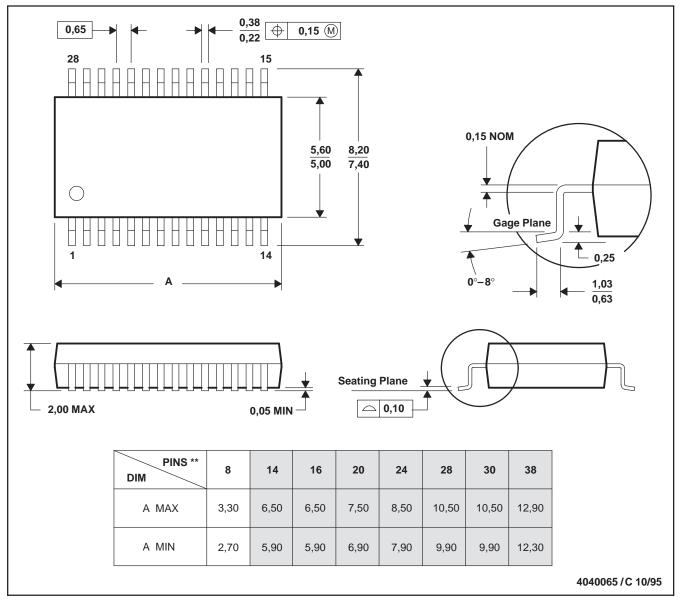
NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

28 PIN SHOWN



NOTES: A. All linear dimensions are in millimeters.

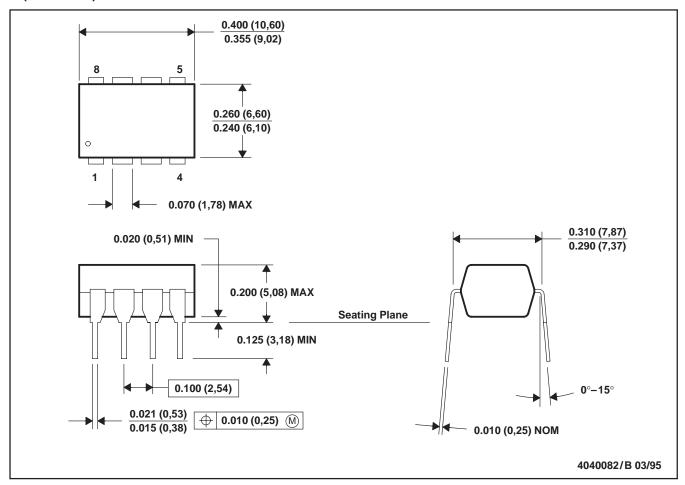
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

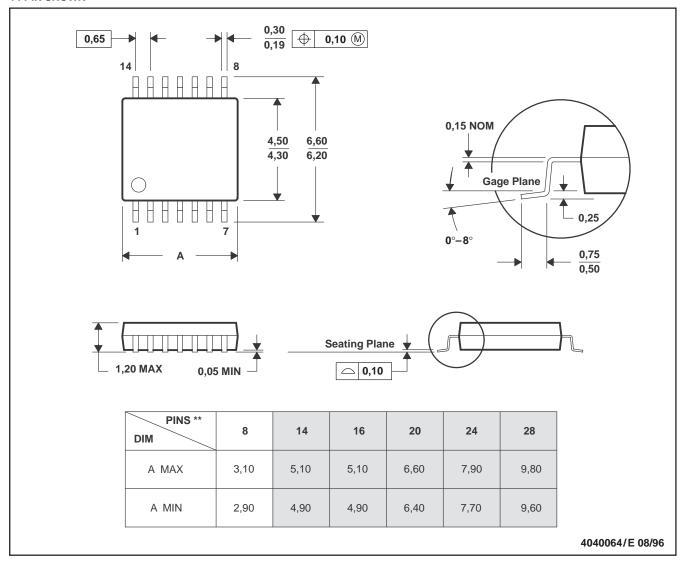
B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153





.com 16-Dec-2006

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TLC551CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC551CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC551CP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC551CPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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