



# FT3001

## Reset Timer with Configurable Delay

### Features

- Delay Times: 3.0, 3.75, 4.5, 6.0 Seconds
- $\leq 1\mu\text{A}$   $I_{CC}$  Current Consumption in Standby
- Primary and Secondary Input Reset Pins
- Push-Pull and Open-Drain Output Pins
- 1.65V to 5.0V Operation at  $T_A = 0^\circ\text{C}$  to  $+85^\circ\text{C}$
- 1.7V to 5.0V Operation at  $T_A = 0^\circ\text{C}$  to  $+85^\circ\text{C}$
- 1.8V to 5.0V Operation at  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$
- Available in 8-Lead MLP and 10-Lead UMLP Packages
- ESD Protection Exceeds:
  - 4kV HBM (per JESD22-A114 & Mil Std 883e 3015.7)
  - 2kV CDM (per ESD STM 5.3)

### Description

The FT3001 is a timer for resetting a mobile device where long reset times are needed. The long delay helps avoid unintended resets caused by accidental key presses. Four timer values can be selected by configuring the DSR0 and DSR1 pins.

The FT3001 has two inputs for single- or dual-button resetting capability. The device has two outputs: a push-pull output with 0.5mA drive and an open-drain output with 0.5mA pull-down drive.

The FT3001 draws minimal supply current when inactive and functions over a power supply range of 1.65V to 5.0V.

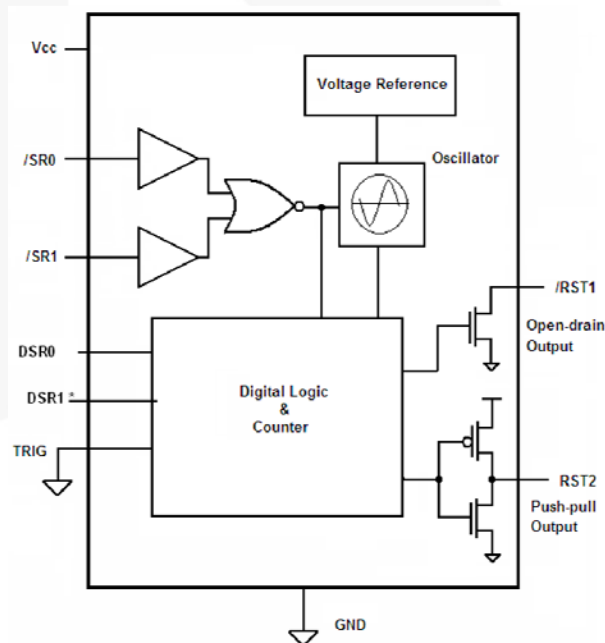


Figure 1. Block Diagram

### Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FT3001UMX	-40°C to +85°C	10-Lead Ultrathin MLP, 1.4 x 1.8 x 0.55mm Package, 0.40mm Pitch	5000 Units Tape and Reel
FT3001MPX	-40°C to +85°C	8-Lead Molded Leadless Package (MLP), Dual JEDEC, MO-229 2.0 x 2.0mm	3000 Units Tape and Reel

## Pin Configurations

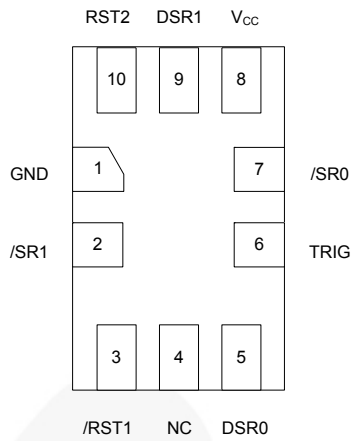


Figure 2. UMLP (Top Through View)

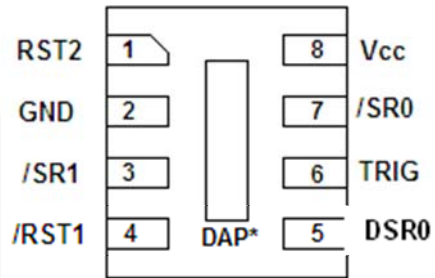


Figure 3. MLP (Top Through View)

## Pin Definitions

UMLP Pin#	MLP Pin#	Name	Description
1	2	GND	Ground
2	3	/SR1	Secondary Reset Input, Active LOW
3	4	/RST1	Open-Drain Output, Active LOW
4		NC	No Connect
5	5	DSR0	Delay Selection Input
6	6	TRIG	Test Pin; tied to ground in normal use
7	7	/SR0	Primary Reset Input, Active LOW
8	8	V <sub>CC</sub>	Power Supply
9		DSR1	Delay Selection Input
10	1	RST2	Push-Pull Output, Active HIGH

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Condition	Min.	Max.	Unit
$V_{CC}$	Supply Voltage		-0.5	7.0	V
$V_{IN}$	DC Input Voltage	/SR0, /SR1, TRIG, DSR0	-0.5	7.0	V
$V_{OUT}$	Output Voltage <sup>(1)</sup>	/RST1, RST2 HIGH or LOW	-0.5	$V_{CC}+0.5$	V
		/RST1, RST2, $V_{CC}=0$	-0.5	7.0	
$I_{IK}$	DC Input Diode Current	$V_{IN} < 0V$		-50	mA
$I_{OK}$	DC Output Diode Current	$V_{OUT} < 0V$		-50	mA
		$V_{OUT} > V_{CC}$		+50	
$I_{OH}/I_{OL}$	DC Output Source/Sink Current		-50	+50	mA
$I_{CC}$	DC $V_{CC}$ or Ground Current per Supply Pin			$\pm 100$	mA
$T_{STG}$	Storage Temperature Range		-65	+150	°C
$V_{CC}$	Junction Temperature Under Bias			+150	°C
$V_{IN}$	Junction Lead Temperature, Soldering 10 Seconds			+260	°C
$P_D$	Power Dissipation			5	mW
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		4	kV
		Charged Device Model, JESD22-C101		2	

### Note:

- $I_O$  absolute maximum rating must be observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	T <sub>A</sub> = 0°C to +85°C	1.65	5.00	V
		T <sub>A</sub> = -25°C to +85°C	1.7	5.0	
		T <sub>A</sub> = -40°C to +85°C	1.8	5.0	
t <sub>VCC_REC</sub>	V <sub>CC</sub> Recovery Time After Power Down	V <sub>CC</sub> = 0V after power down, then rising to 0.5V	5		ms
V <sub>IN</sub>	Input Voltage <sup>(2)</sup>	/SR0, /SR1	0	5.0	V
V <sub>OUT</sub>	Output Voltage	/RST1, RST2 High or Low	0	V <sub>CC</sub>	V
		/RST1, RST2, V <sub>CC</sub> = 0	0	5.0	
I <sub>OH</sub>	DC Output Source Current	RST2, 1.8V ≤ V <sub>CC</sub> ≤ 3.0V	-100	---	μA
		RST2, 3.0V ≤ V <sub>CC</sub> ≤ 5.0V	-500	---	
I <sub>OL</sub>	DC Output Sink Current	/RST1, RST2, V <sub>CC</sub> = 1.8V to 5.0V	+500	---	
T <sub>A</sub>	Free Air Operating Temperature		-40	+85	°C
θ <sub>JA</sub>	Thermal Resistance	MLP-8		245	°C/W
		UMLP-10		200	

### Notes:

2. All unused inputs must be held at V<sub>CC</sub> or GND.

## DC Electrical Characteristics

Unless otherwise specified, conditions of T<sub>A</sub>=-40 to 80C with V<sub>CC</sub>=1.8 - 5.0V OR T<sub>A</sub>=-25 to 85C with V<sub>CC</sub>=1.7 - 5V OR T<sub>A</sub>=0 to 85C with V<sub>CC</sub>=1.65 - 5V produce the performance characteristics below.

Symbol	Parameter	Condition	Min.	Max.	Unit
V <sub>IH</sub>	Input High Voltage <sup>(3)</sup>	/SR0, /SR1	0.8 x V <sub>CC</sub>		V
V <sub>IL</sub>	Input Low Voltage	/SR0, /SR1		0.2 x V <sub>CC</sub>	V
V <sub>IH</sub>	Input High Voltage	DSR0, DSR1	0.8 x V <sub>CC</sub>		V
V <sub>IL</sub>	Input Low Voltage	DSR0, DSR1		0.2 x V <sub>CC</sub>	V
V <sub>OH</sub>	High Level Output Voltage	RST2, I <sub>OH</sub> =-100μA	0.8 x V <sub>CC</sub>		V
		RST2, I <sub>OH</sub> =-500μA V <sub>CC</sub> =3.0 to 5.0V	0.8 x V <sub>CC</sub>		
V <sub>OL</sub>	Low Level Output Voltage	RST2, I <sub>OL</sub> =500μA		0.3	V
		/RST1, I <sub>OL</sub> =500μA		0.3	
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> =0.0V or 5.0V		±1	μA
I <sub>CC</sub>	Quiescent Supply Current (Timer Inactive)	/SR0 or /SR1=V <sub>CC</sub>		1	μA
I <sub>CC</sub>	Dynamic Supply Current (Timer Active)	/SR0 and /SR1=0V		100	μA

### Note:

3. /SR0 and /SR1 HIGH levels should be referenced to the same V<sub>CC</sub> rail supplying the FT3001.

## AC Electrical Characteristics

Unless otherwise specified, conditions of  $T_A = -40$  to  $80^\circ\text{C}$  with  $V_{CC} = 1.8 - 5.0\text{V}$  OR  $T_A = -25$  to  $85^\circ\text{C}$  with  $V_{CC} = 1.7 - 5\text{V}$  OR  $T_A = 0$  to  $85^\circ\text{C}$  with  $V_{CC} = 1.65 - 5\text{V}$  produce the performance characteristics below.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{PHL1}$ , $t_{PLH1}$	Timer Delay, /SRn to /RST1 (DSR0=0, DSR1=0)	$C_L = 5\text{pF}$ , $R_L = 5\text{K}\Omega$ , Figure 9, Figure 4, Figure 5	2.40	3.00	3.60	s
	Timer Delay, /SRn to /RST1 (DSR0=0, DSR1=1)	$C_L = 5\text{pF}$ , $R_L = 5\text{K}\Omega$ , Figure 9, Figure 4, Figure 5	3.00	3.75	4.50	
	Timer Delay, /SRn to RST2 (DSR0=1, DSR1=0)	$C_L = 5\text{pF}$ , $R_L = 10\text{K}\Omega$ , Figure 6, Figure 7	3.60	4.50	5.40	
	Timer Delay, /SRn to RST2 (DSR0=1, DSR1=1),	$C_L = 5\text{pF}$ , $R_L = 10\text{K}\Omega$ , Figure 6, Figure 7	4.80	6.00	7.20	
$t_{REC}$	Reset Timeout Delay, /RST1 and RST2	Figure 4, Figure 5, Figure 6, Figure 7		400		ms

## Capacitance Specifications

$T_A = +25^\circ\text{C}$ .

Symbol	Parameter	Condition	Typical	Unit
$C_{IN}$	Input Capacitance	$V_{CC} = \text{GND}$	4.0	pF
$C_{OUT}$	Output capacitance	$V_{CC} = 5.0\text{V}$	5.0	pF

AC Test Circuits and Waveforms

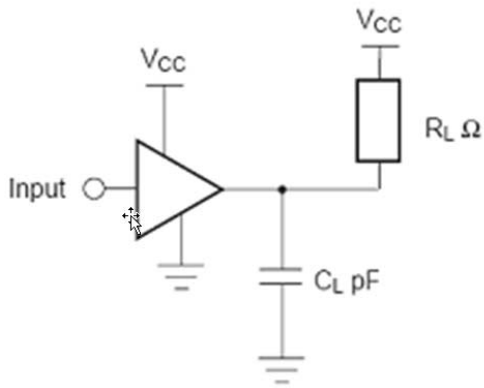


Figure 4. AC Test Circuit, RST1 Output

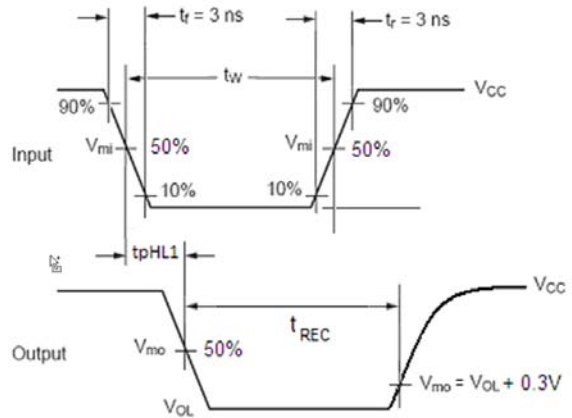


Figure 5. RST1 Output Waveform

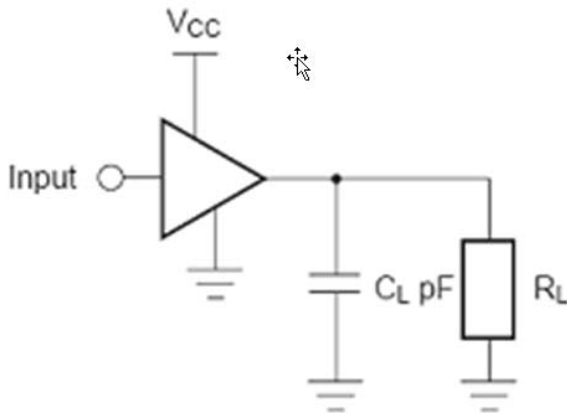


Figure 6. AC Test Circuit, RST2 Output

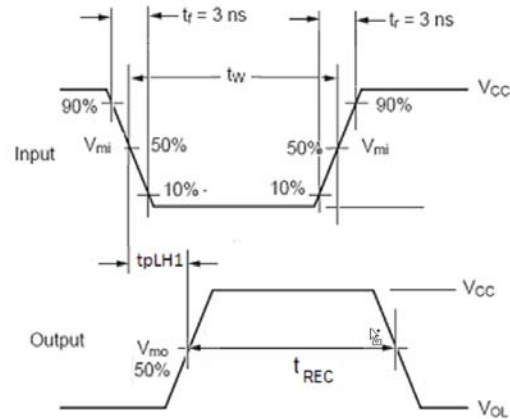


Figure 7. RST2 Output Waveform

## Functional Description

The reset timer uses an internal oscillator and a two-stage 21-bit counter to determine when the output pins switch. The time,  $n$ , is set by the hard-wired logic level of the DSR0 and DSR1 pins. See Table 1 & 2.

**Table 1. FT3001UMX Truth Table**


DSR0	DSR1	Reset Time ( $\pm 20\%$ ) in Seconds
0	0	3.00
0	1	3.75
1	0	4.50
1	1	6.00

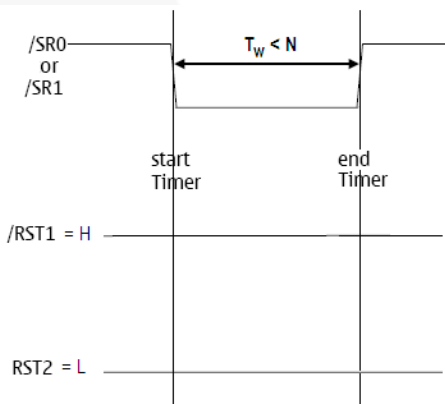
**Table 2. FT3001MPX Truth Table**

DSR0	Reset Time ( $\pm 20\%$ ) in Seconds
0	3.0
1	4.5

The two CMOS input pins, /SR0 and /SR1, control the reset function. A low input signal on both /SR0 and /SR1 starts the oscillator. Both /SR0 and /SR1 pins must be held LOW for time  $n$  before the /RST1 and RST2 outputs are activated. The TRIG pin should be tied LOW during normal operation. The TRIG pin is used for SCAN testing.

**Table 3. Short Duration**

/SR0	/SR1	/RST1	RST2	Description
	L	H	L	The timer starts counting when both inputs go LOW. The timer stops counting and resets when either input goes high. No changes occur on the outputs. Both /SR0 and /SR1 need to be LOW to activate (start) the timer.



**Figure 8. Short Duration**

## Application Information

**IMPORTANT:** The DSR0 and DSR1 pins must be tied to  $V_{CC}$  or GND to provide a HIGH or LOW voltage level. The voltage level on these pins determines the length of the configurable delay. The voltage level on the DSR0 pins must not change during normal operation.

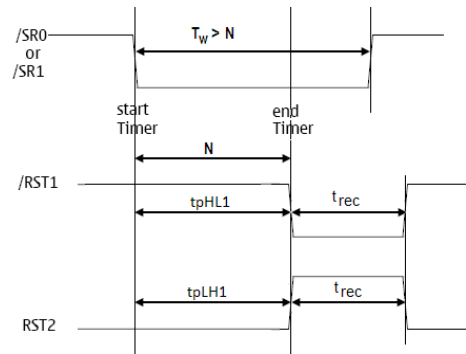
### Short Duration (Button Press Time $< n$ )

In this case, both input /SR0 and /SR1 are LOW for a duration ( $t_w$ ) that is shorter than time  $n$ . When an input goes LOW, the internal timer starts counting. If the input goes HIGH before time  $n$ , the timer stops counting and resets and no changes occur on the outputs.

### Long Duration ( $t_w > n$ )







In this case, both input /SR0 and /SR1 are LOW for a duration ( $t_w$ ) that is longer than time  $n$ . When an input goes LOW, the internal timer starts counting.

After time  $n$ , the outputs switch and the timer stops counting. After time  $t_{REC}$ , the outputs return to their original states.

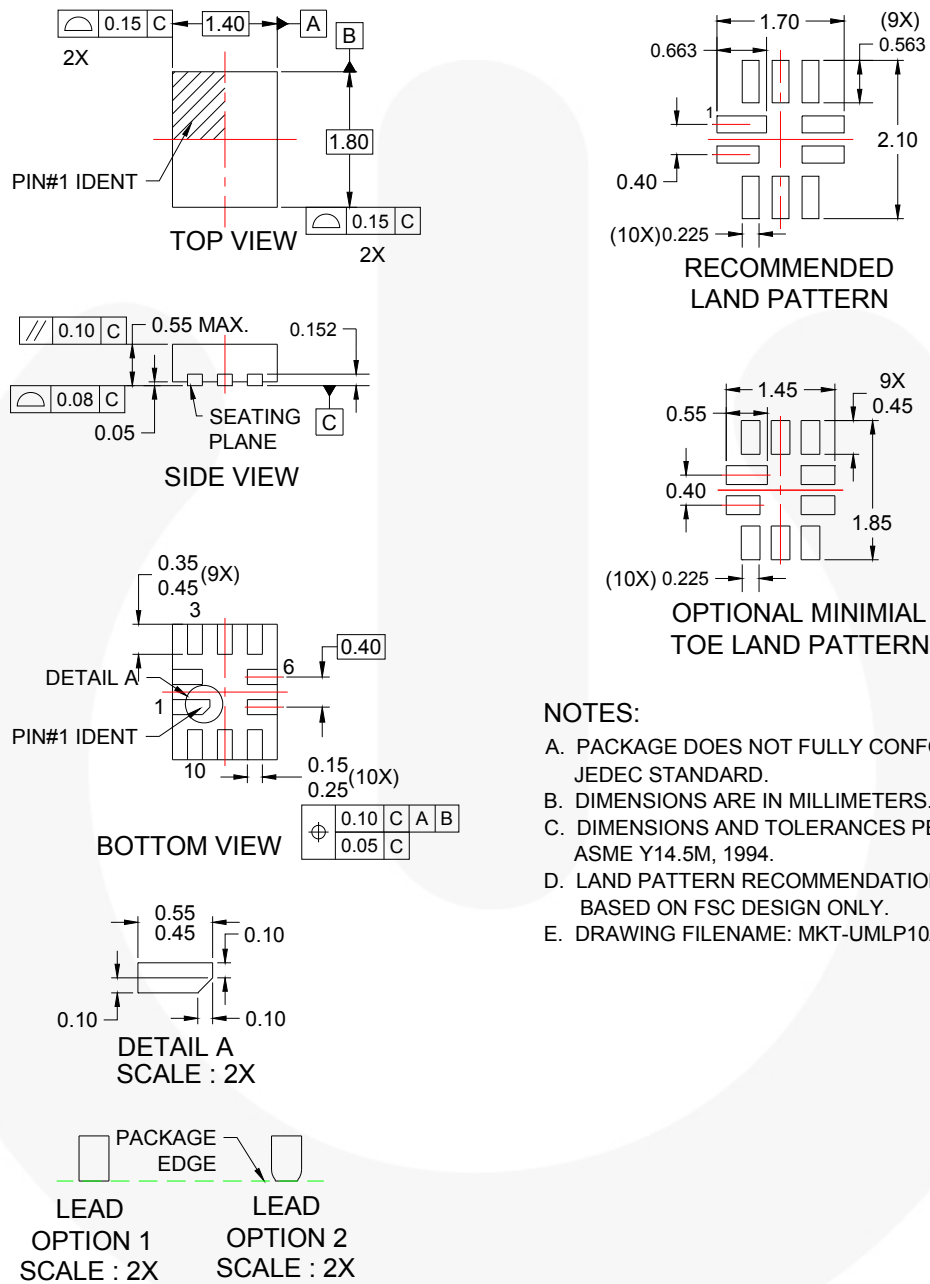


**Figure 9. Long Duration**

**Table 4. Long Duration**

/SR0	/SR1	/RST1	RST2	Description
	L			The timer starts counting when both inputs go LOW. After time $n$ , the outputs switch. After time $t_{REC}$ , the outputs return to their original states. Both /SR0 and /SR1 need to be LOW to activate (start) the timer.
L				

## Physical Dimensions



### NOTES:

- PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.
- DRAWING FILENAME: MKT-UMLP10Arev3.

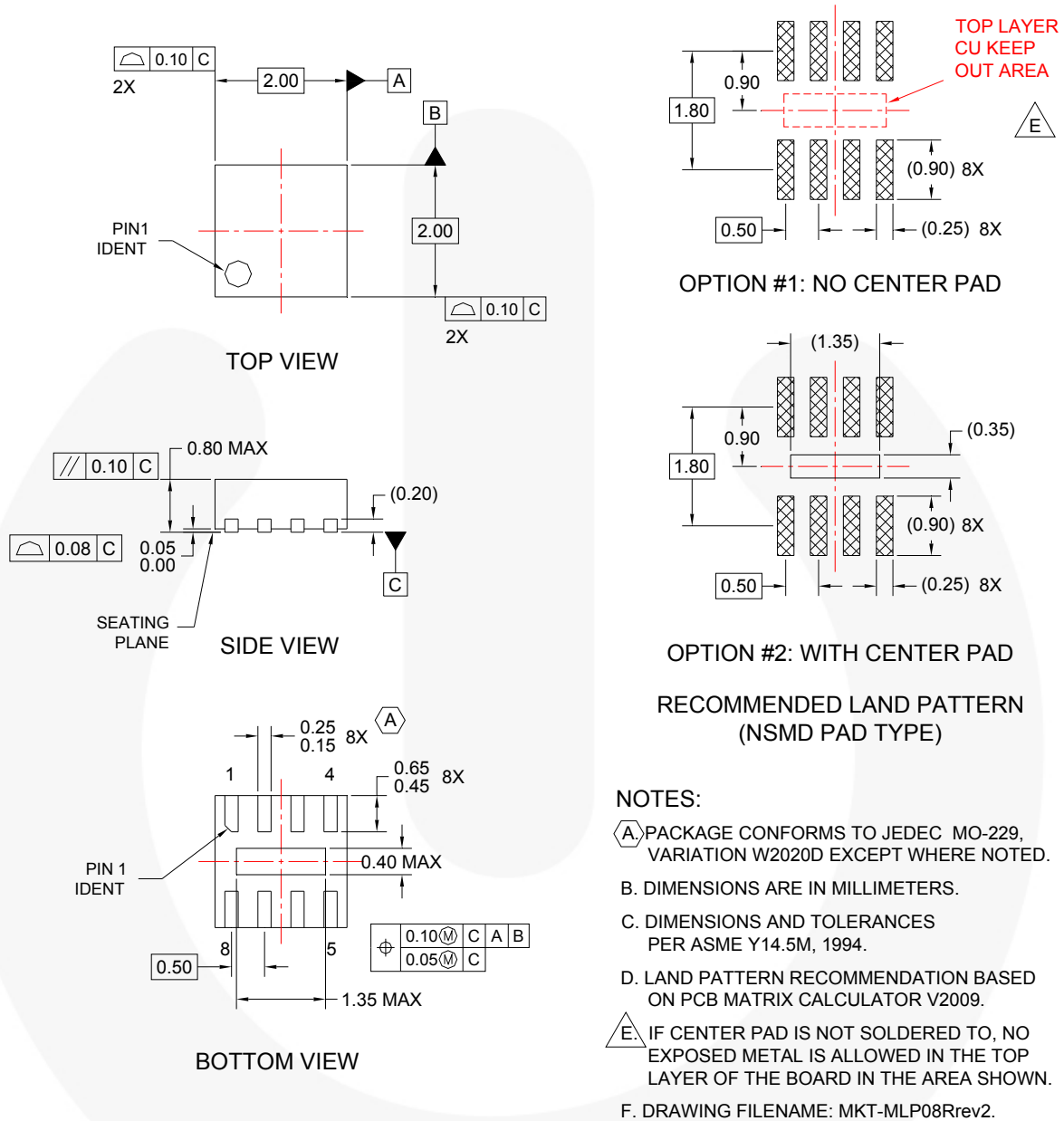
**Figure 10. 10-Lead Ultrathin MLP, 1.4 x 1.8 x 0.55mm Package, 0.40mm Pitch**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:  
<http://www.fairchildsemi.com/packaging/>



**Physical Dimensions (Continued)**



**Figure 11. 8-Lead Molded Leadless Package (MLP), Dual JEDEC, MO-229 2.0 x 2.0mm**





Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:  
<http://www.fairchildsemi.com/packaging/>



**TRADEMARKS**

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- |  |  |  |   |
|--|--|--|---|
| 2Cool™   | F-PFS™   | PowerTrench®   | The Power Franchise®  |
| AccuPower™   | FRFET®   | PowerXS™   | the power franchise   |
| AX-CAP™*   | Global Power Resource™                         | Programmable Active Droop™   | TinyBoost™  |
| BitSiC™  | GreenBridge™                                   | QFET®  | TinyBuck™   |
| Build it Now™  | Green FPS™                                     | QS™  | TinyCalc™   |
| CorePLUS™  | Green FPS™ e-Series™                           | Quiet Series™  | TinyLogic®  |
| CorePOWER™   | Gmax™  | RapidConfigure™  | TINYOPTO™   |
| CROSSVOLT™   | GTO™   |  ™                | TinyPower™  |
| CTL™   | IntelliMAX™                                    | Saving our world, 1mW/W/kW at a time™  | TinyPWM™  |
| Current Transfer Logic™  | ISOPLANAR™                                     | SignalWise™  | TinyWire™   |
| DEUXPEED®  | Making Small Speakers Sound Louder and Better™ | SmartMax™  | TranSiC™  |
| Dual Cool™   | MegaBuck™                                      | SMART START™   | TriFault Detect™  |
| EcoSPARK®  | MICROCOUPLER™                                  | Solutions for Your Success™  | TRUECURRENT®*   |
| EfficientMax™  | MicroFET™                                      | SPM®   | µSerDes™  |
| ESBC™  | MicroPak™                                      | STEALTH™   |  SerDes™ |
|  Fairchild® | MicroPak2™                                     | SuperFET®  | UHC®  |
| Fairchild Semiconductor®   | MillerDrive™                                   | SuperSOT™-3  | Ultra FRFET™  |
| FACT Quiet Series™   | MotionMax™                                     | SuperSOT™-6  | UniFET™   |
| FACT®  | Motion-SPM™                                    | SuperSOT™-8  | VCX™  |
| FAST®  | mWSaver™                                       | SupreMOS®  | VisualMax™  |
| FastvCore™   | OptoHit™                                       | SyncFET™   | VoltagePlus™  |
| FETBench™  | OPTOLOGIC®                                     | Sync-Lock™   | XS™   |
| FlashWriter®*  | OPTOPLANAR®                                    |  SYSTEM GENERAL®* |   |
| FPS™   |  |  |   |

\* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**ANTI-COUNTERFEITING POLICY**

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, [www.fairchildsemi.com](http://www.fairchildsemi.com), under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I61