SCAN90CP02

SCAN90CP02 1.5 Gbps 2x2 LVDS Crosspoint Switch with Pre-Emphasis and IEEE 1149.6



Literature Number: SNLS168L



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General Description

The SCAN90CP02 is a 1.5 Gbps 2 x 2 LVDS crosspoint switch. High speed data paths and flow-through pinout minimize internal device jitter, while configurable 0/25/50/100% pre-emphasis overcomes external ISI jitter effects of lossy backplanes and cables. The differential inputs interface to LVDS and Bus LVDS signals such as those on National's 10-, 16-, and 18- bit Bus LVDS SerDes, as well as CML and LVPECL. The SCAN90CP02 can also be used with ASICs and FPGAs. The non-blocking crosspoint architecture is pinconfigurable as a 1:2 clock or data splitter, 2:1 redundancy mux, crossover function, or dual buffer for signal booster and stub hider applications.

Integrated IEEE 1149.1 (JTAG) and 1149.6 circuitry supports testability of both single-ended LVTTL/CMOS and differential LVDS PCB interconnect. The 3.3V supply, CMOS process, and LVDS I/O ensure high performance at low power over the entire industrial -40 to +85°C temperature range.

Features

- 1.5 Gbps per channel
- Low power: 70 mA in dual repeater mode @1.5 Gbps
- Low output iitter
- Configurable 0/25/50/100% pre-emphasis drives lossy backplanes and cables
- Non-blocking architecture allows 1:2 splitter, 2:1 mux, crossover, and dual buffer configurations
- Flow-through pinout
- LVDS/BLVDS/CML/LVPECL inputs. LVDS Outputs
- IEEE 1149.1 and 1149.6 compliant
- Single 3.3V supply
- Separate control of inputs and outputs allows for power savings
- Industrial -40 to +85°C temperature range
- 28-lead LLP package, or 32-lead LQFP package

Block Diagram

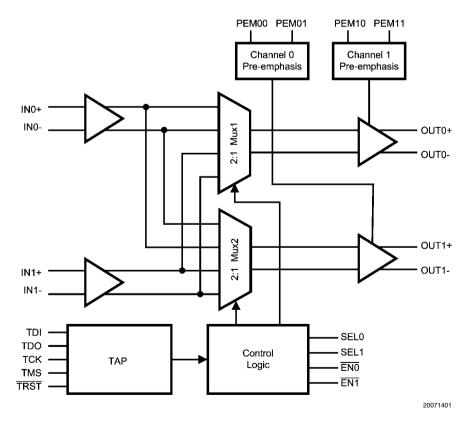


FIGURE 1. SCAN90CP02 Block Diagram

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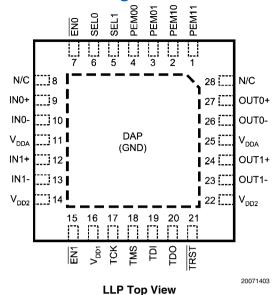
Pin Descriptions

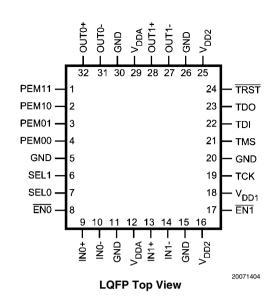
Pin Name	LLP Pin Number	LQFP Pin Number	I/O, Type	Description	
DIFFEREN	TIAL INPU	TS COMM	ON TO ALL MUX	(ES	
IN0+	9	9	I, LVDS	Inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL	
IN0-	10	10		compatible.	
IN1+ IN1-	12 13	13 14	I, LVDS	Inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.	
		NTIAL OUT	TPUTS	Companion.	
OUT0+	27	32	O, LVDS	Inverting and non-inverting differential outputs. OUT0± can be connected to any	
OUT0-	26	31	0, 2, 20	one pair IN0±, or IN1±. LVDS compatible (Note 2).	
OUT1+	24	28	O, LVDS	Inverting and non-inverting differential outputs. OUT1± can be connected to any	
OUT1-	23	27		one pair IN0±, or IN1±. LVDS compatible (Note 2).	
DIGITAL C	ONTROL I	NTERFACE			
SEL0,	6	7	I, LVTTL	Select Control Inputs	
SEL1	5	6			
ENO, EN1	7	8	I, LVTTL	Output Enable Inputs	
	15	17			
PEM00,	4	4	I, LVTTL	Channel 0 Output Pre-emphasis Control Inputs	
PEM01	3	3			
PEM10,	2	2	I, LVTTL	Channel 1 Output Pre-emphasis Control Inputs	
PEM11	10	1	LIVITI	Test Data languists accepted IEEE 1140 1 feetures	
TDI	19	22	I, LVTTL	Test Data Input to support IEEE 1149.1 features	
TDO	20	23	O, LVTTL	Test Data Output to support IEEE 1149.1 features	
TMS TCK	18	21	I, LVTTL	Test Mode Select to support IEEE 1149.1 features	
	17	19	I, LVTTL	Test Clock to support IEEE 1149.1 features	
TRST	21	24	I, LVTTL	Test Reset to support IEEE 1149.1 features	
N/C POWER	8, 28			Not Connected	
		10.10		N	
V_{DD}	11, 14, 16, 22, 25	12, 16, 18, 25, 29	I, Power	V_{DD} = 3.3V ±0.3V. At least 4 low ESR 0.01 µF bypass capacitors should be connected from V_{DD} to GND plane.	
GND	(Note 1)	5, 11, 15,		Ground reference to LVDS and CMOS circuitry.	
		20, 26, 30		For the LLP package, the DAP is used as the primary GND connection to the	
				device. The DAP is the exposed metal contact at the bottom of the LLP-28	
				package. It should be connected to the ground plane with at least 4 vias for optimal AC and thermal performance.	

Note 1: Note that for the LLP package GND is not an actual pin on the package, the GND is connected thru the DAP on the back side of the LLP package.

Note 2: The LVDS outputs do not support a multidrop (BLVDS) environment. The LVDS output characteristics of the SCAN90CP02 device have been optimized for point-to-point backplane and cable applications.

Connection Diagrams





Configuration Select Truth Table

DAP = GND

SEL0	SEL1	EN0	EN1	OUT0	OUT1	Mode
0	0	0	0	IN0	IN0	1:2 Splitter (IN1 powered down)
0	1	0	0	IN0	IN1	Dual Channel Repeater
1	0	0	0	IN1	IN0	Dual Channel Switch
1	1	0	0	IN1	IN1	1:2 Splitter (IN0 powered down)
0	1	0	1	IN0	PD	Single Channel Repeater (Channel 1 powered down)
1	1	0	1	IN1	PD	Single Channel Switch (IN0 and OUT1 powered down)
0	0	1	0	PD	IN0	Single Channel Switch (IN1 and OUT0 powered down)
0	1	1	0	PD	IN1	Single Channel Repeater (Channel 0 powered down)
Х	Х	1	1	PD	PD	Both Channels in Power Down Mode
0	0	0	1			Invalid State*
1	0	0	1			Invalid State*
1	0	1	0			Invalid State*
1	1	1	0			Invalid State*

PD = Power Down mode to minimize power consumption

Pre-Emphasis

The pre-emphasis is used to compensate for long or lossy transmission media. Separate pins are provided for each output to minimize power consumption. Pre-emphasis is programmable to be off or to preset values per the Pre-emphasis Control Selection Table.

Output Characteristics

The output characteristics of the SCAN90CP02 device have been optimized for point-to-point backplane and cable applications.

Pre-emphasis Control Selection Table

Chan	nel 0	Char	nel 1	Pre-emphasis
PEM01 PEM00		PEM11	PEM10	
0	0	0	0	0%
0	1	0	1	25%
1	0	1	0	50%
1	1	1	1	100%

X = Don't Care

^{*} Entering these states is not forbidden, however device operation is not defined in these states.

Applications Information

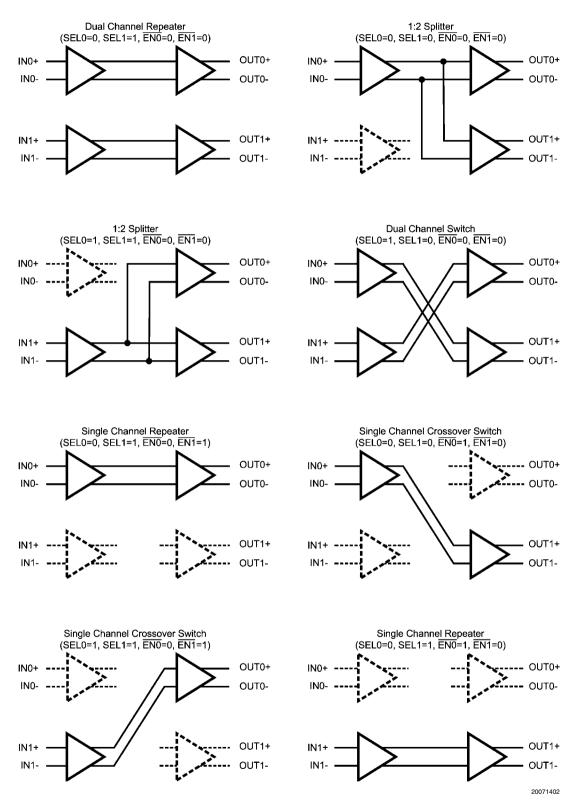


FIGURE 2. SCAN90CP02 Configuration Select Decode

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD}) -0.3V to +4.0V **CMOS Input Voltage** -0.3V to $(V_{DD} + 0.3V)$ LVDS Receiver Input Voltage -0.3V to +3.6V LVDS Driver Output Voltage -0.3V to +3.6VLVDS Output Short Circuit Current 40mA +150°C Junction Temperature Storage Temperature -65°C to +150°C Lead Temperature +260°C (Soldering, 4sec.) Maximum Package Power Dissipation at 25°C LLP-28 4.31 W LQFP-32 1.47 W Derating above 25°C

LQFP-32	11.8 mW/°C
Thermal Resistance, θ_{JA}	
LLP-28	29°C/W
LQFP-32	85°C/W
ESD Rating	
HBM, 1.5 kΩ, 100 pF	6.5 kV
EIAJ, 0Ω , 200 pF	>250V

Recommended Operating Conditions

	Min	Тур	Max	Unit
Supply Voltage (V _{DD} - GND)	3.0	3.3	3.6	V
Receiver Input Voltage	0		3.6	V
Operating Free Air				
Temperature	-40	25	85	°C
Junction Temperature			150	°C

Electrical Characteristics

LLP-28

Over recommended operating supply and temperature ranges unless other specified.

34.5 mW/°C

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
LVTTL DO	C SPECIFICATIONS (SEL0, SEL1, E	1, TDI, TCK	, TMS, TRS	ST)		
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I _{IH}	High Level Input Current	$V_{IN} = V_{DD} = V_{DDMAX}$	-10		+10	μA
I _{IL}	Low Level Input Current	$V_{IN} = V_{SS}, V_{DD} = V_{DDMAX}$	-10		+10	μA
I _{ILR}	Low Level Input Current	TDI, TMS, TRST	-40		-200	μA
C _{IN1}	Input Capacitance	Any Digital Input Pin to V _{SS}		3.5		pF
C _{OUT1}	Output Capacitance	Any Digital Output Pin to V _{SS}		5.5		pF
V _{CL}	Input Clamp Voltage	I _{CL} = -18 mA	-1.5	-0.8		V
V _{OH}	High Level Output Voltage	$I_{OH} = -12 \text{ mA}, V_{DD} = 3.0 \text{ V}$	2.4			V
	(TDO)	$I_{OH} = -100 \ \mu A, \ V_{DD} = 3.0 \ V$	V _{DD} -0.2			V
$\overline{V_{OL}}$	Low Level Output Voltage	I _{OL} = 12 mA, V _{DD} = 3.0 V			0.5	V
	(TDO)	$I_{OL} = 100 \mu A, V_{DD} = 3.0 V$			0.2	V
I _{os}	Output Short Circuit Current	TDO	-15		-125	mA
LVDS INF	PUT DC SPECIFICATIONS (IN0±, IN	11±)				
V _{TH}	Differential Input High Threshold (Note 5)	$V_{CM} = 0.8V \text{ or } 1.2V \text{ or } 3.55V, V_{DD} = 3.6V$		0	100	mV
V _{TL}	Differential Input Low Threshold	$V_{CM} = 0.8V \text{ or } 1.2V \text{ or } 3.55V, V_{DD} = 3.6V$	-100	0		mV
V _{ID}	Differential Input Voltage	V _{CM} = 0.8V to 3.55V, V _{DD} = 3.6V	100			mV
V _{CMR}	Common Mode Voltage Range	V _{ID} = 150 mV, V _{DD} = 3.6V	0.05		3.55	V
C _{IN2}	Input Capacitance	IN+ or IN- to V _{SS}		3.5		pF
I _{IN}	Input Current	$V_{IN} = 3.6V$, $V_{DD} = V_{DDMAX}$ or $0V$	-10		+10	μA
		$V_{IN} = 0V$, $V_{DD} = V_{DDMAX}$ or $0V$	-10		+10	μA

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
LVDS OU	ITPUT DC SPECIFICATIONS (OUTO	±, OUT1±)					
V _{OD}	Differential Output Voltage, 0% Pre-emphasis (Note 5)	R_L = 100Ω between OUT+ and	250	400	575	mV	
ΔV_{OD}	Change in V _{OD} between Complementary States		-35		35	mV	
V _{os}	Offset Voltage (Note 6)		Ī	1.09	1.25	1.475	V
ΔV _{OS}	Change in V _{OS} between Complementary States		-	-35		35	mV
I _{OS}	Output Short Circuit Current, One Complementary Output	OUT+ or OUT- Short to GND			-60	-90	mA
C _{OUT2}	Output Capacitance	OUT+ or OUT- to GND when T STATE®	RI-		5.5		pF
SUPPLY	CURRENT (Static)	<u> </u>					
I _{CC0}	Supply Current	All inputs and outputs enabled a active, terminated with differentian 100Ω between OUT+ and OUT-	al load of		42	60	mA
I _{CC1}	Supply Current - one channel powered down	Single channel crossover switch channel repeater modes (1 char active, one channel in power down	or single nnel		22	30	mA
I _{CC2}	Supply Current - one input powered down	Splitter mode (One input powere both outputs active)	ed down,		30	40	mA
I _{CCZ}	TRI-STATE Supply Current	Both input/output Channels in P Down Mode	ower		1.4	2.5	mA
SWITCHI	NG CHARACTERISTICS—LVDS OU	JTPUTS (Figures 3, 4)	<u>.</u>				
t _{LHT}	Differential Low to High Transition Time	Use an alternating 1 and 0 patte Mb/s, measure between 20% an		70	150	215	ps
t _{HLT}	Differential High to Low Transition Time	V _{OD} .	50	135	180	ps	
t _{PLHD}	Differential Low to High Propagation Delay	Use an alternating 1 and 0 patte Mb/s, measure at 50% V _{OD} betw		0.5	2.4	3.5	ns
t _{PHLD}	Differential High to Low Propagation Delay	input to output.		0.5	2.4	3.5	ns
t _{SKD1}	Pulse Skew	It _{PLHD} -t _{PHLD} I			55	120	ps
t _{SKCC}	Output Channel to Channel Skew	Difference in propagation delay (t _{PLHD} or t _{PHLD}) among all output channels in Splitter mode (any one input to all outputs).		0	130	315	ps
t _{JIT}	Jitter (0% Pre-emphasis)	RJ - Alternating 1/0 @ 750 MHz	(Note 8)		1.4	2.5	psrms
	(Note 7)	DJ - K28.5 Pattern	LQFP		110	140	psp-p
		1.5 Gbps (Note 9)	LLP		42	75	psp-p
		TJ - PRBS 223-1 Pattern	LQFP		113	148	psp-p
		1.5 Gbps (Note 10)	LLP		93	126	psp-p
t _{ON}	LVDS Output Enable Time	Time from ENx to OUT± change from TRI-STATE to active.		50	110	150	ns
t _{OFF}	LVDS Output Disable Time	Time from ENx to OUT± change from active to TRI-STATE.			5	12	ns
t _{SW}	LVDS Switching Time SELx to OUT±	Time from configuration select (SELx) to new switch configuration effective for OUT±.			110	150	ns

SCAN Circuitry Timing Requirements

Symbol	Parameter	Conditions	Min	Тур	Max	Units
f _{MAX}	Maximum TCK Clock Frequency	$R_L = 500\Omega$,	25.0			MHz
t _S	TDI to TCK, H or L	$C_L = 35 pF$	1.0			ns
t _H	TDI to TCK, H or L		2.0			ns
t _S	TMS to TCK, H or L		2.0			ns
t _H	TMS to TCK, H or L		1.5			ns
t _W	TCK Pulse Width, H or L		10.0			ns
t _W	TRST Pulse Width, L		2.5			ns
t _{REC}	Recovery Time, TRST to TCK		2.0			ns

Note 3: "Absolute Maximum Ratings" are the ratings beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

Note 4: Typical parameters are measured at $V_{DD} = 3.3V$, $T_A = 25$ °C. They are for reference purposes, and are not production-tested.

Note 5: Differential output voltage V_{OD} is defined as ABS(OUT+-OUT-). Differential input voltage V_{ID} is defined as ABS(IN+-IN-).

Note 6: Output offset voltage V_{OS} is defined as the average of the LVDS single-ended output voltages at logic high and logic low states.

Note 7: Jitter is not production tested, but guaranteed through characterization on a sample basis.

Note 8: Random Jitter, or RJ, is measured RMS with a histogram including 1500 histogram window hits. The input voltage = V_{ID} = 500mV, 50% duty cycle at 750MHz, $t_r = t_f$ = 50ps (20% to 80%).

Note 9: Deterministic Jitter, or DJ, is measured to a histogram mean with a sample size of 350 hits. The input voltage = $V_{ID} = 500$ mV, K28.5 pattern at 1.5 Gbps, $t_r = t_f = 50$ ps (20% to 80%). The K28.5 pattern is repeating bit streams of (0011111010 110000101).

Note 10: Total Jitter, or TJ, is measured peak to peak with a histogram including 3500 window hits. Stimulus and fixture jitter has been subtracted. The input voltage = V_{ID} = 500mV, 223-1 PRBS pattern at 1.5 Gbps, $t_r = t_i$ = 50ps (20% to 80%).

Timing Diagrams

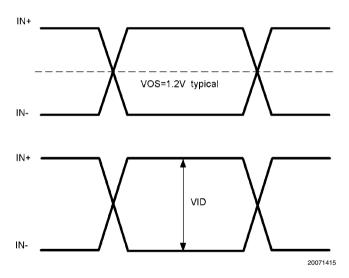


FIGURE 3. LVDS Signals

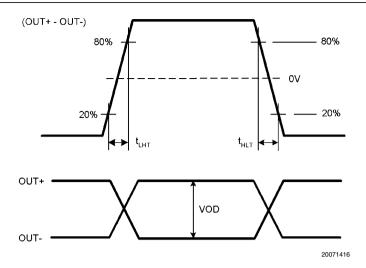


FIGURE 4. LVDS Output Transition Time

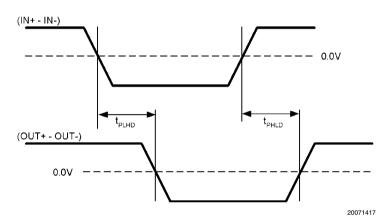


FIGURE 5. LVDS Output Propagation Delay

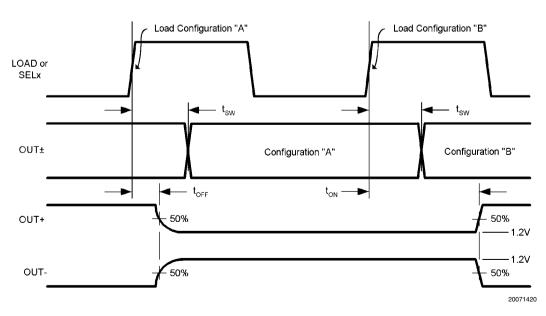
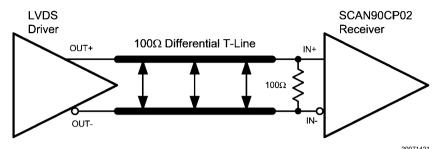


FIGURE 6. Configuration and Output Enable/Disable Timing

Input Interfacing

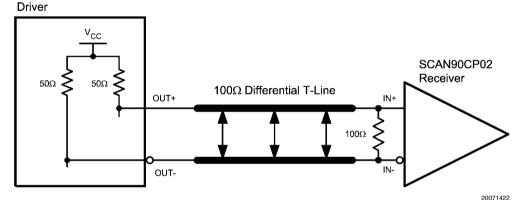
The SCAN90CP02 accepts differential signals and allow simple AC or DC coupling. With a wide common mode range, the

SCAN90CP02 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers.

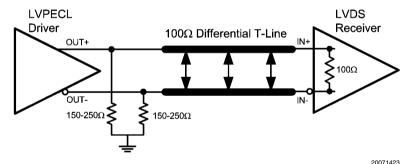


Typical LVDS Driver DC-Coupled Interface to SCAN90CP02 Input

CML3.3V or CML2.5V



Typical CML Driver DC-Coupled Interface to SCAN90CP02 Input



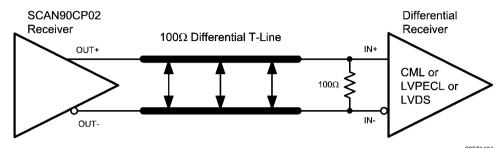
Typical LVPECL Driver DC-Coupled Interface to SCAN90CP02 Input

9

Output Interfacing

The SCAN90CP02 outputs signals that are compliant to the LVDS standard. Their outputs can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers

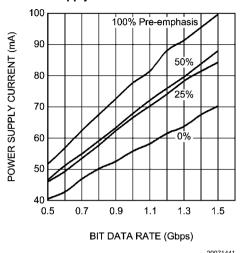
and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accomodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.



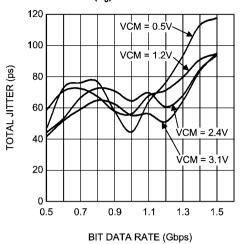
Typical SCAN90CP02 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

Typical Performance Characteristics for LLP Package

Power Supply Current vs. Bit Data Rate



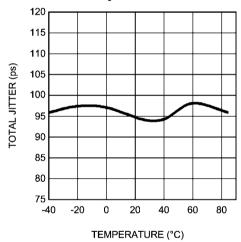
Total Jitter (T_.) vs. Bit Data Rate



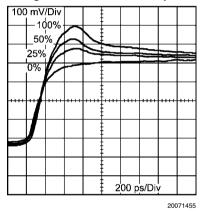
20071442

Dynamic power supply current was measured while running a PRBS 2²³-1 patternTotal Jitter measured at 0V differential while running a PRBS 2²³-1 pattern in in dual channel repeater mode. V_{CC} = 3.3V, T_A = +25°C, V_{ID} = 0.5V, V_{CM} = 1.2Vsingle channel repeater mode. V_{CC} = 3.3V, T_A = +25°C, V_{ID} = 0.5V, 0% Pre-

Total Jitter (T_.) vs. Temperature



Positive Edge Transition vs. Pre-emphasis Level



20071443

Total Jitter measured at 0V differential while running a PRBS 2²³-1 pattern in dual channel repeater mode. $V_{CC}=3.3V,\ V_{ID}=0.5V,\ V_{CM}=1.2V,\ 1.5$ Gbps data rate, 0% Pre-emphasis

FIGURE 7. Typical Performance Characteristics

Design-For-Test (DfT) Features

IEEE 1149.1 SUPPORT

The SCAN90CP02 supports a fully compliant IEEE 1149.1 interface. The Test Access Port (TAP) provides access to boundary scan cells at each LVTTL I/O on the device for interconnect testing. Differential pins are included in the same boundary scan chain but instead contain IEEE1149.6 cells. IEEE1149.6 is the improved IEEE standard for testing high-speed differential signals.

Refer to the BSDL file located on National's website for the details of the SCAN90CP02 IEEE 1149.1 implementation.

IEEE 1149.6 SUPPORT

AC-coupled differential interconnections on very high speed (1+ Gbps) data paths are not testable using traditional IEEE 1149.1 techniques. The IEEE 1149.1 structures and methods are intended to test static (DC-coupled), single ended networks. IEEE1149.6 is specifically designed for testing high-speed differential, including AC coupled networks.

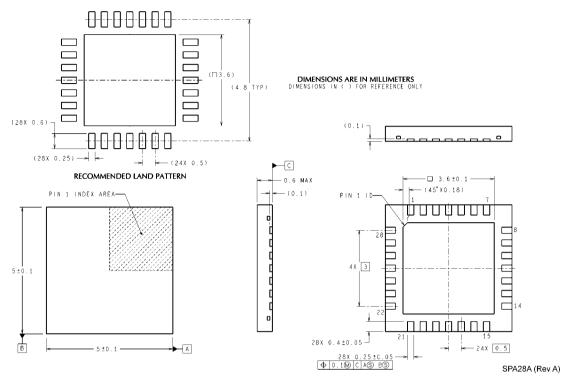
The SCAN90CP02 is intended for high-speed signalling up to 1.5 Gbps and includes IEEE1149.6 on all differential inputs and outputs.

FAULT INSERTION

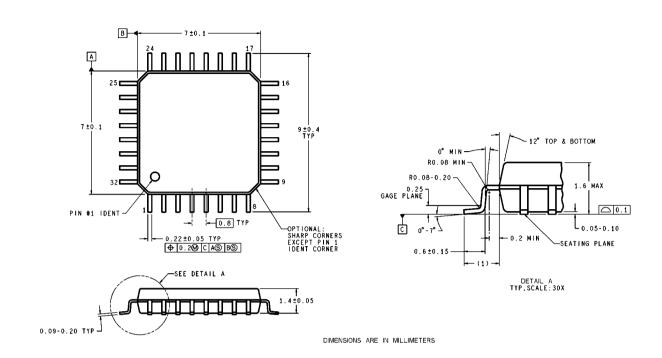
Fault Insertion is a technique used to assist in the verification and debug of diagnostic software. During system testing faults are "injected" to simulate hardware failure and thus help verify the monitoring software can detect and diagnose these faults. In the SCAN90004 an IEEE1149.1 "stuck-at" instruction can create a stuck-at condition, either high or low, on any pin or combination of pins.

A more detailed description of the stuck-at feature can be found in NSC Applications note AN-1313.

Physical Dimensions inches (millimeters) unless otherwise noted



LLP, Plastic, QUAD,
Order Number SCAN90CP02SP (1000 piece Tape and Reel),
SCAN90CP02SPX (4500 piece Tape and Reel)
NS Package Number SPA28A



VBE32A (Rev E)

LQFP, Plastic, Quad Order Number SCAN90CP02VY (250 piece Tray) SCAN90CP02VYX (1000 piece Tape and Reel) NS Package Number VBE32A

Notes

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Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns	
Data Converters	www.national.com/adc	Samples	www.national.com/samples	
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards	
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging	
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green	
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts	
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality	
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback	
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy	
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions	
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero	
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic	
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