DS90CP02

DS90CP02 1.5 Gbps 2x2 LVDS Crosspoint Switch

Literature Number: SNLS267

National Semiconductor

November 20, 2008

DS90CP02
1.5 Gbps 2x2 LVDS Crosspoint Switch

General Description

The DS90CP02 is a 1.5 Gbps 2 x 2 LVDS crosspoint switch optimized for high-speed signal routing and switching over lossy FR-4 printed circuit board backplanes and balanced cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity. The non-blocking architecture allows connections of any input to any output or outputs.

Wide input common mode range allows the switch to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires a minimal space on the board while the flow-through pinout allows easy board layout. The 3.3V supply, CMOS process, and LVDS I/O ensure high performance at low power over the entire industrial -40 to +85°C temperature range.

Features

- 1.5 Gbps per channel
- Low power: 70 mA in dual repeater mode @1.5 Gbps
- Low output jitter
- Non-blocking architecture allows 1:2 splitter, 2:1 mux, crossover, and dual buffer configurations
- Flow-through pinout
- LVDS/BLVDS/CML/LVPECL inputs, LVDS Outputs
- Single 3.3V supply
- Separate control of inputs and outputs allows for power savings
- Industrial -40 to +85°C temperature range
- 28-lead LLP-28 space saving package

Block Diagram

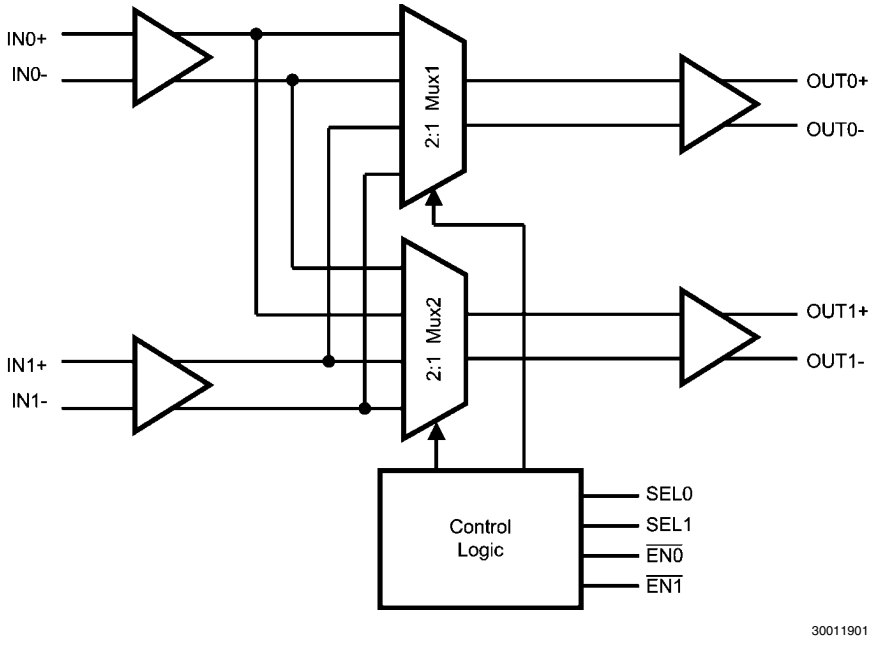
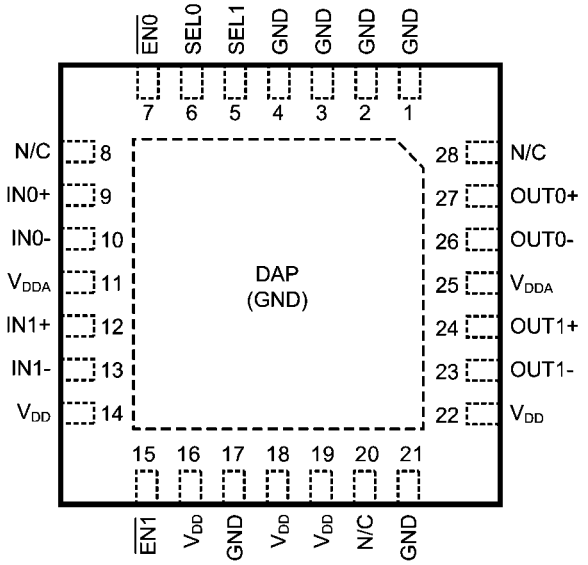


FIGURE 1. DS90CP02 Block Diagram

Pin Descriptions

Pin Name	Pin Number	I/O, Type	Description
DIFFERENTIAL INPUTS COMMON TO ALL MUXES			
IN0+ IN0–	9 10	I, LVDS	Inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
IN1+ IN1–	12 13	I, LVDS	Inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
SWITCHED DIFFERENTIAL OUTPUTS			
OUT0+ OUT0–	27 26	O, LVDS	Inverting and non-inverting differential outputs. OUT0± can be connected to any one pair IN0±, or IN1±. LVDS compatible .
OUT1+ OUT1–	24 23	O, LVDS	Inverting and non-inverting differential outputs. OUT1± can be connected to any one pair IN0±, or IN1±. LVDS compatible .
DIGITAL CONTROL INTERFACE			
SEL0, SEL1	6 5	I, LVTTL	Select Control Inputs
$\overline{EN0}$, $\overline{EN1}$	7 15	I, LVTTL	Output Enable Inputs
N/C	8, 20, 28		Not Connected
POWER			
V_{DD}	11, 14, 16, 18, 19, 22, 25	I, Power	V_{DD} = 3.3V ±0.3V. At least 4 low ESR 0.01 µF bypass capacitors should be connected from V_{DD} to GND plane.
GND	DAP, 1, 2, 3, 4, 17, 21	I, Power	Ground reference to LVDS and CMOS circuitry. For the LLP package, the DAP is used as the primary GND connection to the device. The DAP is the exposed metal contact at the bottom of the LLP-28 package. It should be connected to the ground plane with at least 4 vias for optimal AC and thermal performance.

Connection Diagram



LLP Top View
DAP = GND

Configuration Select Truth Table

SEL0	SEL1	$\overline{EN0}$	$\overline{EN1}$	OUT0	OUT1	Mode
0	0	0	0	IN0	IN0	1:2 Splitter (IN1 powered down)
0	1	0	0	IN0	IN1	Dual Channel Repeater
1	0	0	0	IN1	IN0	Dual Channel Switch
1	1	0	0	IN1	IN1	1:2 Splitter (IN0 powered down)
0	1	0	1	IN0	PD	Single Channel Repeater (Channel 1 powered down)
1	1	0	1	IN1	PD	Single Channel Switch (IN0 and OUT1 powered down)
0	0	1	0	PD	IN0	Single Channel Switch (IN1 and OUT0 powered down)
0	1	1	0	PD	IN1	Single Channel Repeater (Channel 0 powered down)
X	X	1	1	PD	PD	Both Channels in Power Down Mode
0	0	0	1			Invalid State*
1	0	0	1			Invalid State*
1	0	1	0			Invalid State*
1	1	1	0			Invalid State*

PD = Power Down mode to minimize power consumption
X = Don't Care
* Entering these states is not forbidden, however device operation is not defined in these states.

Application Information

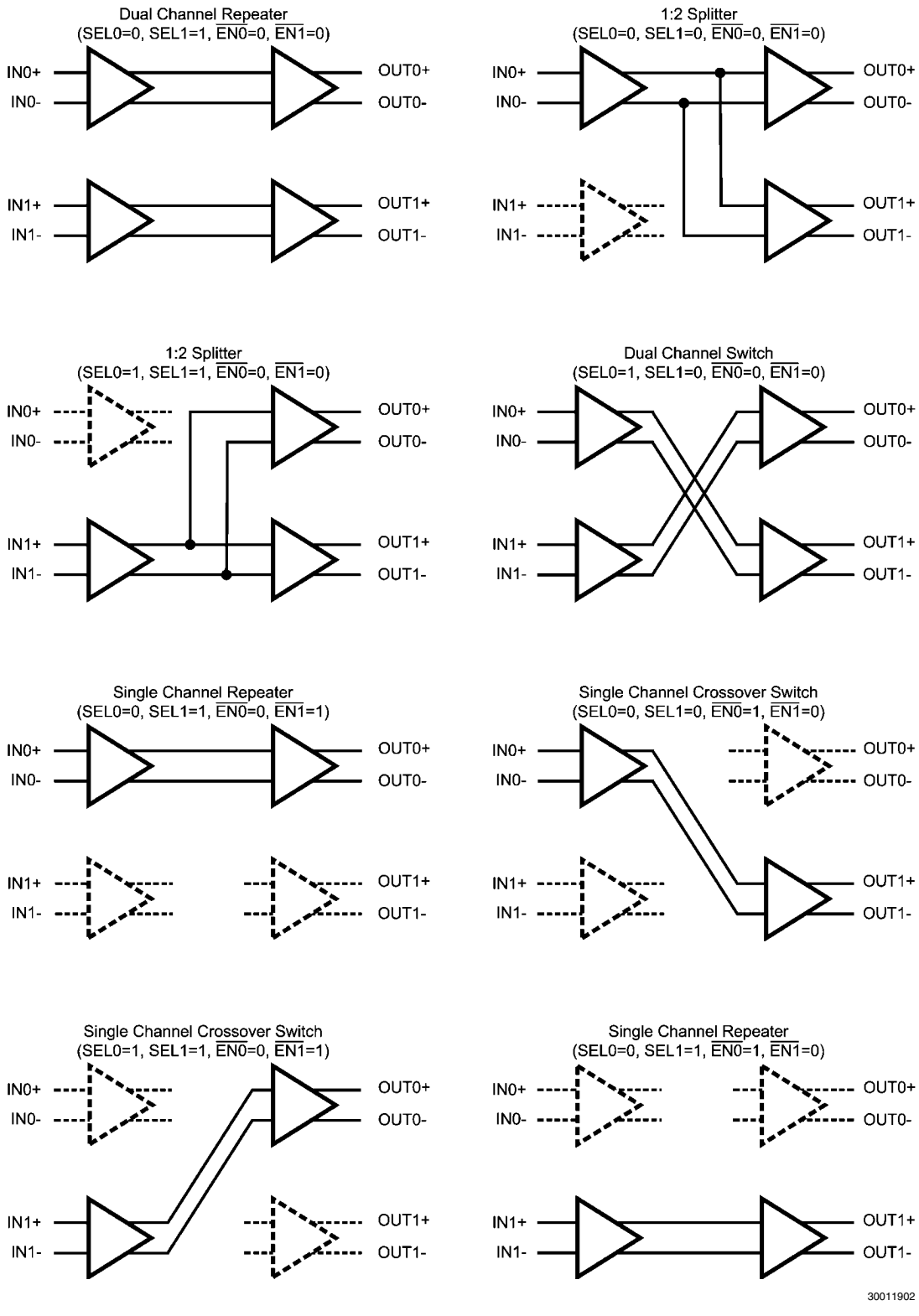


FIGURE 2. DS90CP02 Configuration Select Decode

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.3V to +4.0V
CMOS Input Voltage	−0.3V to (V_{DD} +0.3V)
LVDS Receiver Input Voltage	−0.3V to +3.6V
LVDS Driver Output Voltage	−0.3V to +3.6V
LVDS Output Short Circuit Current	40mA
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
LLP-28	4.31 W
Derating above 25°C	
LLP-28	34.5 mW/°C
Thermal Resistance, θ_{JA}	
LLP-28	29°C/W
ESD Rating	
HBM, 1.5 kΩ, 100 pF	6.5 kV
EIAJ, 0Ω, 200 pF	>250V

Recommended Operating Conditions

	Min	Typ	Max	Unit
Supply Voltage (V_{DD}– GND)	3.0	3.3	3.6	V
Receiver Input Voltage	0		3.6	V
Operating Free Air Temperature	−40	25	85	°C
Junction Temperature			150	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
LVTTL DC SPECIFICATIONS (SEL0, SEL1, $\overline{EN1}$, $\overline{EN2}$)						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{DD} = V_{DDMAX}$	−10		+10	µA
I_{IL}	Low Level Input Current	$V_{IN} = V_{SS}$, $V_{DD} = V_{DDMAX}$	−10		+10	µA
C_{IN1}	Input Capacitance	Any Digital Input Pin to V_{SS}		3.5		pF
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA	−1.5	−0.8		V
LVDS INPUT DC SPECIFICATIONS (IN0±, IN1±)						
V_{TH}	Differential Input High Threshold (Note 3)	V_{CM} = 0.8V or 1.2V or 3.55V, V_{DD} = 3.6V		0	100	mV
V_{TL}	Differential Input Low Threshold	V_{CM} = 0.8V or 1.2V or 3.55V, V_{DD} = 3.6V	−100	0		mV
V_{ID}	Differential Input Voltage	V_{CM} = 0.8V to 3.55V, V_{DD} = 3.6V	100			mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 150 mV, V_{DD} = 3.6V	0.05		3.55	V
C_{IN2}	Input Capacitance	IN+ or IN– to V_{SS}		3.5		pF
I_{IN}	Input Current	V_{IN} = 3.6V, $V_{DD} = V_{DDMAX}$ or 0V	−10		+10	µA
		V_{IN} = 0V, $V_{DD} = V_{DDMAX}$ or 0V	−10		+10	µA
LVDS OUTPUT DC SPECIFICATIONS (OUT0±, OUT1±)						
V_{OD}	Differential Output Voltage, 0% Pre-emphasis (Note 3)	R_L = 100Ω between OUT+ and OUT–	250	400	575	mV
ΔV_{OD}	Change in V_{OD} between Complementary States		−35		35	mV
V_{OS}	Offset Voltage (Note 4)		1.09	1.25	1.475	V
ΔV_{OS}	Change in V_{OS} between Complementary States		−35		35	mV
I_{OS}	Output Short Circuit Current, One Complementary Output	OUT+ or OUT– Short to GND		−60	-90	mA
C_{OUT}	Output Capacitance	OUT+ or OUT– to GND when TRI-STATE		5.5		pF

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
SUPPLY CURRENT (Static)						
I_{CC0}	Supply Current	All inputs and outputs enabled and active, terminated with differential load of 100Ω between OUT+ and OUT-.		42	60	mA
I_{CC1}	Supply Current - one channel powered down	Single channel crossover switch or single channel repeater modes (1 channel active, one channel in power down mode)		22	30	mA
I_{CC2}	Supply Current - one input powered down	Splitter mode (One input powered down, both outputs active)		30	40	mA
I_{CCZ}	TRI-STATE Supply Current	Both input/output Channels in Power Down Mode		1.4	2.5	mA
SWITCHING CHARACTERISTICS—LVDS OUTPUTS (*Figures 3*, *4*)						
t_{LHT}	Differential Low to High Transition Time	Use an alternating 1 and 0 pattern at 200 Mb/s, measure between 20% and 80% of V_{OD}.	70	150	215	ps
t_{HLT}	Differential High to Low Transition Time		50	135	180	ps
t_{PLHD}	Differential Low to High Propagation Delay	Use an alternating 1 and 0 pattern at 200 Mb/s, measure at 50% V_{OD} between input to output.	0.5	2.4	3.5	ns
t_{PHLD}	Differential High to Low Propagation Delay		0.5	2.4	3.5	ns
t_{SKD1}	Pulse Skew	$\lvert t_{PLHD} - t_{PHLD} \rvert$		55	120	ps
t_{SKCC}	Output Channel to Channel Skew	Difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels in Splitter mode (any one input to all outputs).	0	130	315	ps
t_{JIT}	Jitter (Note 5)	RJ - Clock Pattern 750 MHz (Note 6)		1.4	2.5	psrms
		DJ - K28.5 Pattern 1.5 Gbps (Note 7)		42	75	psp-p
		TJ - PRBS 2^{23}-1 Pattern 1.5 Gbps (Note 8)		93	126	psp-p
t_{ON}	LVDS Output Enable Time	Time from $\overline{ENx}$ to OUT± change from TRI-STATE to active.	50	110	150	ns
t_{OFF}	LVDS Output Disable Time	Time from $\overline{ENx}$ to OUT± change from active to TRI-STATE.		5	12	ns
t_{SW}	LVDS Switching Time SELx to OUT±	Time from configuration select (SELx) to new switch configuration effective for OUT±.		110	150	ns

Note 1: "Absolute Maximum Ratings" are the ratings beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

Note 2: Typical parameters are measured at V_{DD} = 3.3V, T_A = 25°C. They are for reference purposes, and are not production-tested.

Note 3: Differential output voltage V_{OD} is defined as ABS(OUT+–OUT–). Differential input voltage V_{ID} is defined as ABS(IN+–IN–).

Note 4: Output offset voltage V_{OS} is defined as the average of the LVDS single-ended output voltages at logic high and logic low states.

Note 5: Jitter is not production tested, but guaranteed through characterization on a sample basis.

Note 6: Random Jitter, or RJ, is measured RMS with a histogram including 1500 histogram window hits. The input voltage = V_{ID} = 500mV, 50% duty cycle at 750MHz, $t_r = t_f$ = 50ps (20% to 80%).

Note 7: Deterministic Jitter, or DJ, is measured to a histogram mean with a sample size of 350 hits. The input voltage = V_{ID} = 500mV, K28.5 pattern at 1.5 Gbps, $t_r = t_f$ = 50ps (20% to 80%). The K28.5 pattern is repeating bit streams of (0011111010 1100000101).

Note 8: Total Jitter, or TJ, is measured peak to peak with a histogram including 3500 window hits. Stimulus and fixture jitter has been subtracted. The input voltage = V_{ID} = 500mV, 2^{23}-1 PRBS pattern at 1.5 Gbps, $t_r = t_f$ = 50ps (20% to 80%).

Timing Diagrams

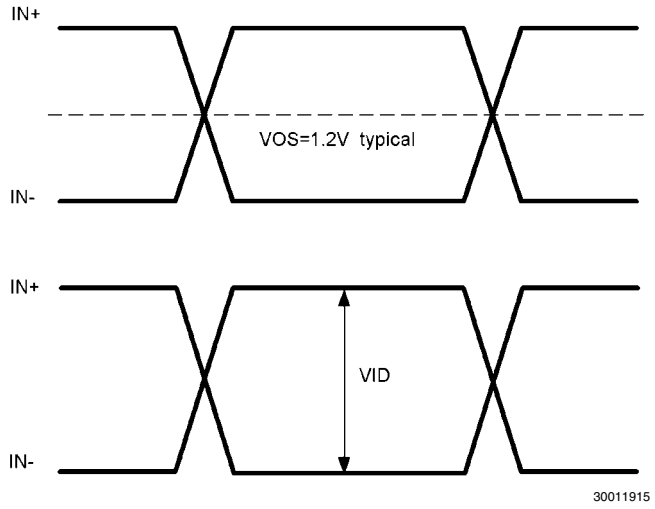


FIGURE 3. LVDS Signals

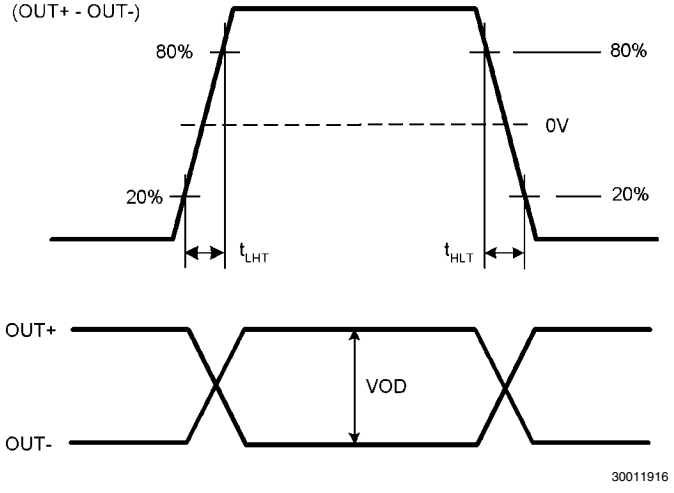


FIGURE 4. LVDS Output Transition Time

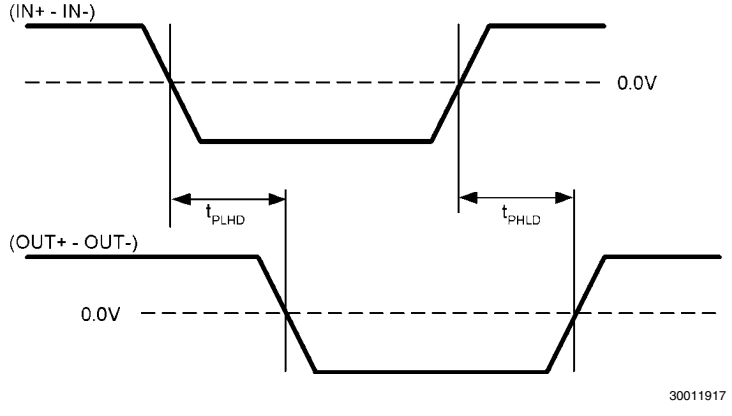


FIGURE 5. LVDS Output Propagation Delay

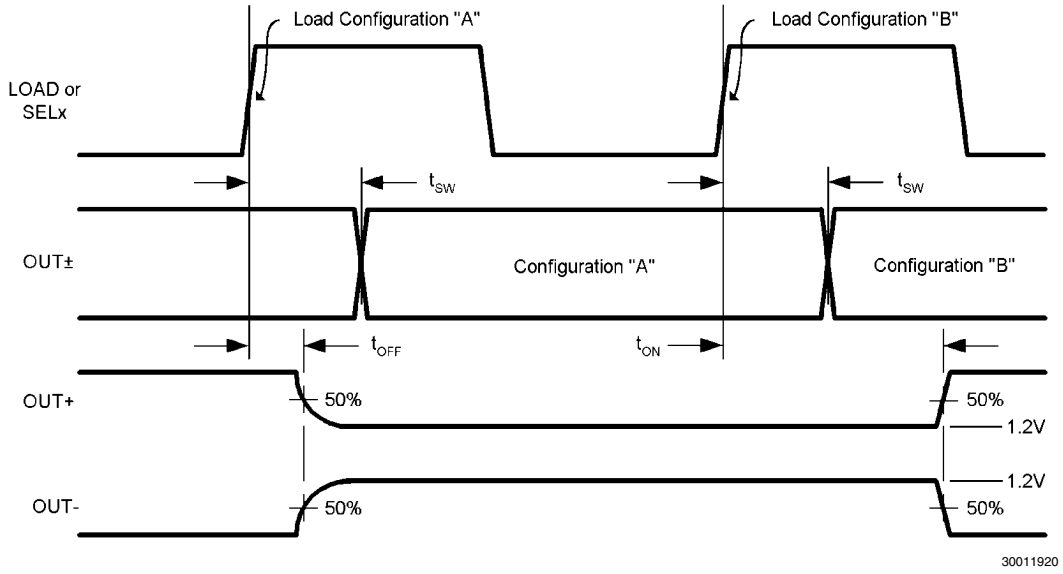
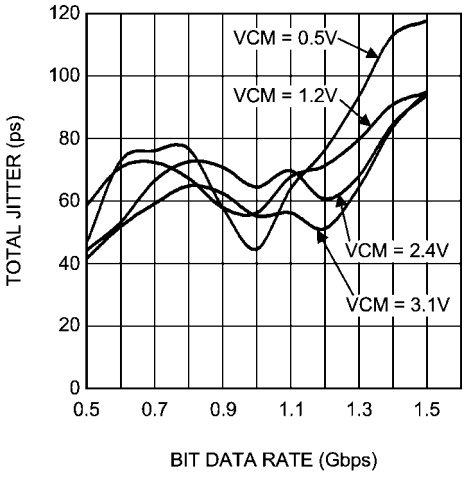


FIGURE 6. Configuration and Output Enable/Disable Timing

Typical Performance

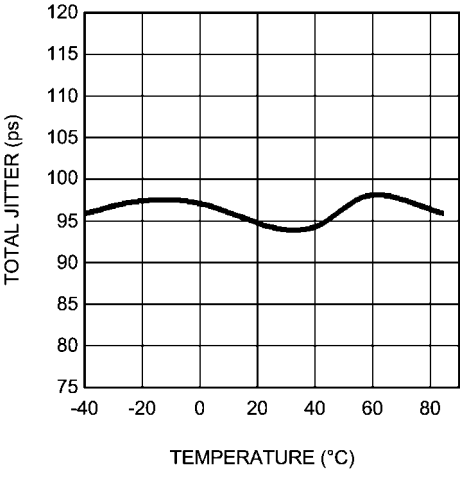
Total Jitter (T_J) vs. Bit Data Rate



30011942

Total Jitter measured at 0V differential while running a PRBS 2^{23}-1 pattern in single channel repeater mode. V_{CC} = 3.3V, T_A = +25°C, V_{ID} = 0.5V

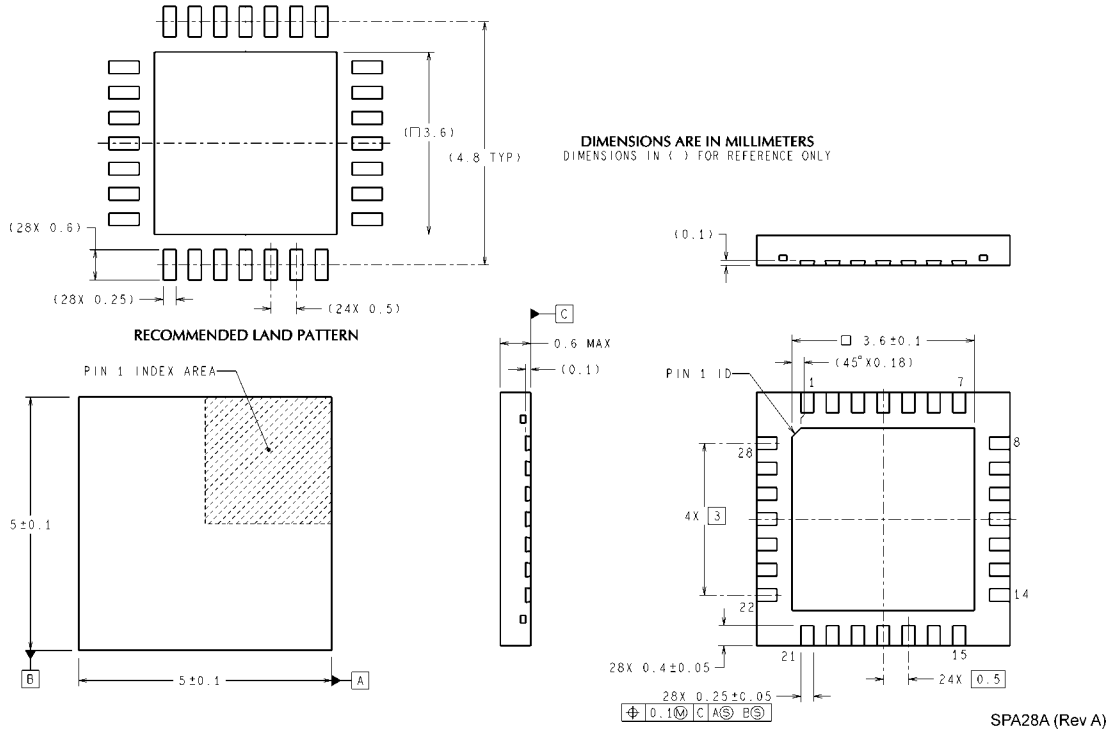
Total Jitter (T_J) vs. Temperature



30011943

Total Jitter measured at 0V differential while running a PRBS 2^{23}-1 pattern in dual channel repeater mode. V_{CC} = 3.3V, V_{ID} = 0.5V, V_{CM} = 1.2V, 1.5 Gbps data rate

Physical Dimensions inches (millimeters) unless otherwise noted



LLP, Plastic, QUAD,
Order Number DS90CP02SP (1000 piece Tape and Reel),
DS90CP02SPX (4500 piece Tape and Reel)
NS Package Number SPA28A

Notes

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench
Audio	www.national.com/audio	App Notes	www.national.com/appnotes
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	Solar Magic®	www.national.com/solarmagic
Wireless (PLL/VCO)	www.national.com/wireless	Analog University®	www.national.com/AU

National Semiconductor Americas Technical Support Center
Email: support@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Technical Support Center
Email: europe.support@nsc.com
German Tel: +49 (0) 180 5010 771
English Tel: +44 (0) 870 850 4288

National Semiconductor Asia Pacific Technical Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Technical Support Center
Email: jpn.feedback@nsc.com

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265