

SLLS699A-JUNE 2007-REVISED JANUARY 2009

Gigabit 2x2 CROSSPOINT SWITCH

FEATURES

- Up to 4.25 Gbps Operation
- Non-blocking Architecture Allows Each Output to be Connected to Any Input
- 30 ps of Deterministic Jitter
- Selectable Transmit Pre-Emphasis Per Lane
- Receive Equalization
- Available Packaging 24 Pin QFN
- Propagation Delay Times: 500 ps Typical
- Inputs Electrically Compatible With CML Signal Levels
- Operates From a Single 3.3-V Supply
- Ability to 3-STATE Outputs
- Low Power: 290 mW (typ)
- Integrated Termination Resistors

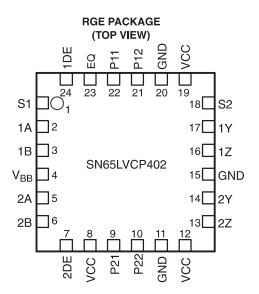
APPLICATIONS

- Clock Buffering/Clock MUXing
- Wireless Base Stations
- High-Speed Network Routing
- Telecom/Datacom
- XAUI 802.3ae Protocol Backplane Redundancy

DESCRIPTION

The SN65LVCP402 is a 2x2 non-blocking crosspoint switch in a flow-through pin-out allowing for ease in PCB layout. VML signaling is used to achieve a high-speed data throughput while using low power. Each of the output drivers includes a 2:1 multiplexer to allow any input to be routed to any output. Internal signal paths are fully differential to achieve the high signaling speeds while maintaining low signal skews. The SN65LVCP402 incorporates $100-\Omega$ termination resistors for those applications where board space is a premium. Built-in transmit pre-emphasis and receive equalization for superior signal integrity performance.

The SN65LVCP402 is characterized for operation from -40°C to 85° C.





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN65LVCP402

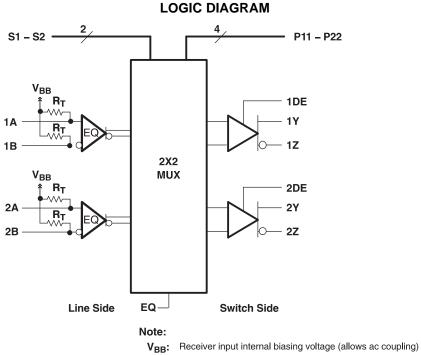


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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



EQ: Input Equalizer (compensates for frequency dependent

- transmission line loss of backplanes)
- RT: Internal 50–Ohm receiver termination (100–Ohm differential)

Preemphasis: Output precompensation for transmission line losses

TERMINAL FUNCTIONS

TERMINAL		ТҮРЕ	DESCRIPTION
NAME	NO.		DESCRIPTION
High Speed I/C)		
xA xB	2, 5 3, 6	Differential Inputs (with 50- Ω termination to V _{BB}) xA=P; xB=N	Line Side Differential Inputs CML compatible
xY xZ	17, 14 16, 13	Differential Output xY=P; xZ=N	Switch Side Differential Outputs. VML
Control Signal	S	-	
xDE	24, 7	Input	Data Enable; Active Low; LVTTL; When not enabled the output is in 3-STATE mode for power savings
S1, S2	1, 18	Input; S1 = Channel 1	Switching Selection; LVTTL
P11-P22	22, 21, 9, 10	Input; P11- Channel 1 bit one	Output Preemphasis Control; LVTTL
EQ	23	Input: Selection for Receive Equalization Setting	EQ=1 (default) is for the 5 dB setting; EQ=0 is for the 12 dB setting
Power Supply			
VCC	8, 12, 19	Power	Power Supply 3.3 V ±5%
GND	11, 15, 20		
Thermal Pad	Thermal Pad		The ground center pad of the package must be connected to GND plane with thermal vias.
V _{BB}	4	Input	Receiver input biasing voltage. For ac coupling, V_{BB} should be left floating for optimal bias value. For dc coupling, V_{BB} can driven to change the common mode. V_{BB} should not be tied to ground.



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EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

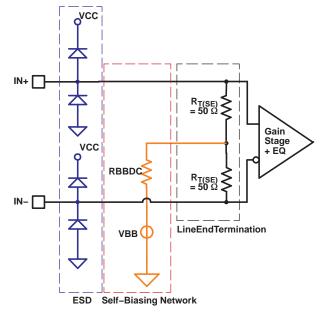


Figure 1. Equivalent Input Circuit Design

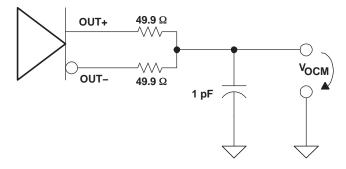




Table 1. CROSSPOINT LOGIC TABLES

OUTPUT CHAI	NNEL 1 (1Y/1Z)	OUTPUT CHANNEL 2 (2Y/2Z)		
CONTROL PINS			INPUT SELECTED	
S1		S2		
0	1A/1B	0	1A/1B	
1	2A/2B	1	2A/2B	

AVAILABLE OPTIONS

Ŧ	DESCRIPTION	PACKAGED DEVICE ⁽¹⁾⁽²⁾	
'A	DESCRIPTION	RGE (24 pin)	
-40°C to 85°C	Serial multiplexer	SN65LVCP402	

(1) The package is available taped and reeled. Add an R suffix to device types (e.g., SN65LVCP402RGER).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



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DISSIPATION RATINGS

PACKAGE THERMAL CHARACTERISTICS ⁽¹⁾		
Parameter	Conditions	NOM
θ_{JA} (junction-to-ambient) #1	4-layer JEDEC Board (JESD51-7), Airflow = 0 ft/min	106.6 C/W
θ_{JA} (junction-to-ambient) #2	4-layer JEDEC Board (JESD51-7) using 4 Thermal-vias of 22-mil diameter each, Airflow = 0 ft/min	55.4 C/W

(1) See application note SPRA953 for a detailed explanation of thermal parameters (http://www-s.ti.com/sc/psheets/spra953/spra953.pdf).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

				UNIT
V _{CC}	Supply voltage r	ange ⁽²⁾	–0.5 V to 6 V	
V	Voltogo rongo		Control inputs, all outputs	-0.5 V to (V _{CC} + 0.5 V)
VI	Voltage range		Receiver inputs	–0.5 V to 4 V
	F0D	Human Body Model ⁽³⁾	All pins	4 kV
	ESD	Charged-Device Model ⁽⁴⁾	All pins	500 V
TJ	Maximum junction	on temperature		See Package Thermal Characteristics Table
	Moisture sensitivity level			2
	Reflow temperature package soldering, 4 seconds			260°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

All voltage values, except differential I/O bus voltages, are with respect to network ground terminal. Tested in accordance with JEDEC Standard 22, Test Method A114-A. (2)

(3)

Tested in accordance with JEDEC Standard 22, Test Method C101. (4)



RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
dR	Operating data rate				4.25	Gbps
V _{CC}	Supply voltage		3.135	3.3	3.465	V
V _{CC(N)}	Supply voltage noise amplitude	10 Hz to 2 GHz			20	mV
TJ	Junction temperature				125	°C
T _A	Operating free-air temperature ⁽¹⁾		-40		85	°C
DIFFER	ENTIAL INPUTS					
		dR _(in) ≤ 1.25 Gbps	100		1750	mV _{PP}
V _{ID}	Receiver peak-to-peak differential input voltage ⁽²⁾	1.25 Gbps < dR _(in) ≤ 3.125 Gbps	100		1560	mV _{PP}
	Voltage	dR _(in) > 3.125 Gbps	100		1000	$\mathrm{mV}_{\mathrm{PP}}$
V _{ICM}	Receiver common-mode input voltage	Note: for best jitter performance ac coupling is recommended.	1.5	1.6 ^V cc	$=\frac{ V_{ID} }{2}$	V
CONTR	OL INPUTS					
VIH	High-level input voltage		2	Vo	_C + 0.3	V
V _{IL}	Low-level input voltage		-0.3		0.8	V
DIFFER	ENTIAL OUTPUTS					
RL	Differential load resistance		80	100	120	Ω

(1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

(2) Differential input voltage V_{ID} is defined as | IN+ - IN- |.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
DIFFERE	NTIAL INPUTS					
V _{IT+}	Positive going differential input high threshold				50	mV
V _{IT-}	Negative going differential input low threshold		-50			mV
A _(EQ)	Equalizer gain	at 1.875 GHz (EQ=0)		12		dB
R _{T(D)}	Termination resistance, differential		80	100	120	Ω
V_{BB}	Open-circuit Input voltage (input self-bias voltage)	AC-coupled inputs		1.6		V
R _(BBDC)	Biasing network dc impedance			30		kΩ
Ċ	Biasing network ac	375 MHz		42		Ω
R _(BBAC)	impedance	1.875 GHz		8.4		Ω
DIFFERE	NTIAL OUTPUTS					
V _{ODH}	High-level output voltage	$R_{L} = 100 \ \Omega \pm 1\%,$		650		mV _{PP}
V _{ODL}	Low-level output voltage	PRES_1 = PRES_0=0; PREL_1 = PREL_0=0; 4 Gbps alternating		-650		mV_{PP}
V _{ODB(PP)}	Output differential voltage without preemphasis ⁽²⁾	1010-pattern; Figure 3	1000	1300	1500	mV _{PP}
V _{OCM}	Output common mode voltage			1.65		V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See Figure 2		1		mV

- (1) All typical values are at $T_A = 25^{\circ}C$ and $V_{CC} = 3.3 \text{ V}$ supply unless otherwise noted. They are for reference purposes and are not production tested.
- (2) Differential output voltage $V_{(ODB)}$ is defined as | OUT+ OUT– |.



ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TES	T CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
	Output preemphasis voltage		Px_2:Px_1 = 00		0		
	ratio,	$R_{L} = 100 \ \Omega \pm 1\%;$	Px_2:Px_1 = 01		3		
V _(PE)		x = Channel 1 or 2; See Figure 3	Px_2:Px_1 = 10		6		dB
	VODPE(PP)	See Figure 5	Px_2:Px_1= 11		9		
t _(PRE)	Preemphasis duration measurement	Output preemphasis is set to 9 dB during test PREx_x = 1; Measured with a 100-MHz clock signal; $R_{\perp} = 100 \Omega \pm 1\%$, See Figure 4			175		ps
r _o	Output resistance	Differential on-chip termination between OUT+ and OUT-			100		Ω
CONTR	OL INPUTS						
IIH	High-level Input current	VIN = VCC				5	μA
IIL	Low-level Input current	VIN = GND		-125	-90		μA
R _(PU)	Pullup resistance				35		kΩ
	CONSUMPTION						
PD	Device power dissipation	All outputs terminate	ed 100 Ω		290	414	mW
Pz	Device power dissipation in 3-state	All outputs in 3-state				331	mW
I _{CC}	Device current consumption	All outputs terminated 100 Ω	PRBS 2 ⁷⁻¹ pattern at 4 Gbps			115	mA

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
MULTI	PLEXER					
t _(SM)	Multiplexer switch time	Multiplexer to valid output		3	6	ns
DIFFE	RENTIAL OUTPUTS					
t _{PLH}	Low-to-high propagation delay	Propagation delay input to output		0.5	0.7	ns
t _{PHL}	High-to-low propagation delay	See Figure 6		0.5	0.7	ns
t _r	Rise time	20% to 80% of V _{O(DB)} ; Test Pattern: 100-MHz clock signal;		80		ps
t _f	Fall time	See Figure 5 and Figure 8		80		ps
t _{sk(p)}	Pulse skew, t _{PHL} – t _{PLH} ⁽²⁾				20	ps
t _{sk(o)}	Output skew ⁽³⁾	All outputs terminated with 100 Ω		25	100	ps
t _{sk(pp)}	Part-to-part skew ⁽⁴⁾				300	ps
t _{zd}	3-State switch time to disable	Assumes 50 Ω to Vcm and 150 pF load on each output			20	ns
t _{ze}	3-State switch time to enable	Assumes 50 Ω to Vcm and 150 pF load on each output			10	ns
RJ	Device random jitter, rms	See Figure 8 for test circuit. BERT setting 10 ⁻¹⁵ Alternating 10-pattern.		0.8	2	ps-rms

(1)

All typical values are at 25°C and with 3.3 V supply unless otherwise noted. $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any output of a single device. (2)

(3)

 $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any two outputs of a single device. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices (4) operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.



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SWITCHING CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	AMETER TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT	
	Intrinsic deterministic device jitter ⁽⁵⁾⁽⁶⁾ , peak-to-peak	0 dB preemphasis (PREx_x = 0); See Figure 8 for the test circuit.	PRBS 2 ⁷⁻¹ pattern	4 Gbps			30	ps
DJ	Absolute deterministic output jitter ⁽⁷⁾ , peak-to-peak			1.25 Gbps Over 20-inch FR4 trace		7		
			PRBS 2 ⁷⁻¹ pattern	4 Gbps Over FR4 trace 2-inch to 20 inches long		20		ps

(5) Intrinsic deterministic device jitter is a measurement of the deterministic jitter contribution from the device. It is derived by the equation (DJ_(OUT) – DJ_(IN)), where DJ_(OUT) is the total peak-to-peak deterministic jitter measured at the output of the device in PSPP. DJ_(IN) is the peak-to-peak deterministic jitter of the pattern generator driving the device.

(6) The SN65LVCP402 built-in passive input equalizer compensates for ISI. For a 20-inch FR4 transmission line with 8-mil trace width, the LVCP402 typically reduces jitter by 60 ps from the device input to the device output.

(7) Absolute deterministic output jitter reflects the deterministic jitter measured at the SN65LVCP402 output. The value is a real measured value with a Bit error tester as described in Figure 8. The absolute DJ reflects the sum of all deterministic jitter components accumulated over the link: DJ_(absolute) = DJ_(Signal generator) + DJ_(transmission line) + DJ_{(intrinsic(LVCP402))}.

Table 2. Preemphasis Controls Settings

– – (1)	- (1)	OUTPUT	OUTPUT LEVEL IN mV _{PP}		TYPICAL FR4
Px_2 ⁽¹⁾	Px_1 ⁽¹⁾	PREEMPHASIS LEVEL IN dB	DE-EMPHASIZED	PRE-EMPHASIZED	TRACE LENGTH
0	0	0 dB	1200	1200	10 inches of FR4 trace
0	1	3 dB	850	1200	20 inches of FR4 trace
1	0	6 dB	600	1200	30 inches of FR4 trace
1	1	9 dB	425	1200	40 inches of FR4 trace

(1) x = 1 or 2

Table 2. Receive Equalization Settings

EQ	Equalization	Typical Line Trace
1	5 dB	25 inches of FR4
0	12 dB	43 inches of FR4



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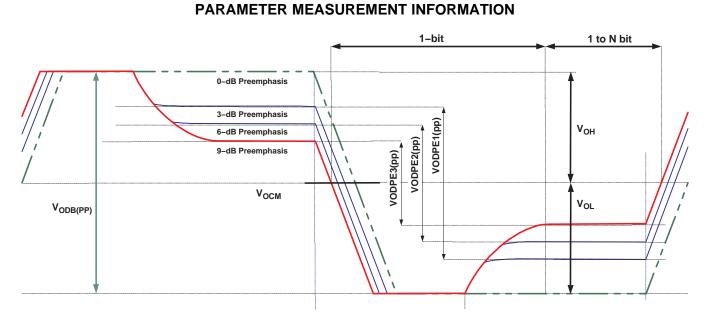


Figure 3. Preemphasis and Output Voltage Waveforms and Definitions

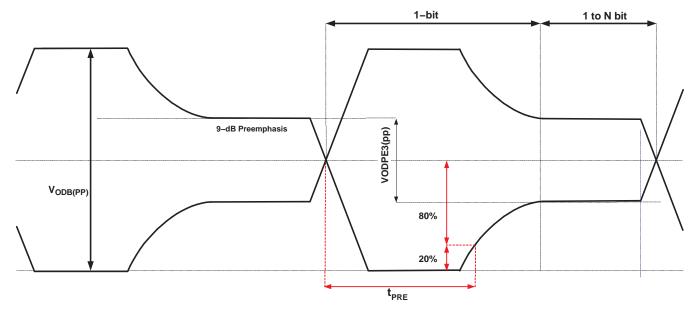


Figure 4. t_{(PRE}) Preemphasis Duration Measurement

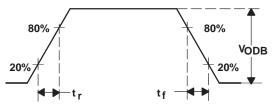


Figure 5. Driver Output Transition Time



PARAMETER MEASUREMENT INFORMATION (continued)

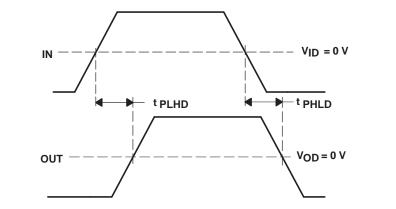
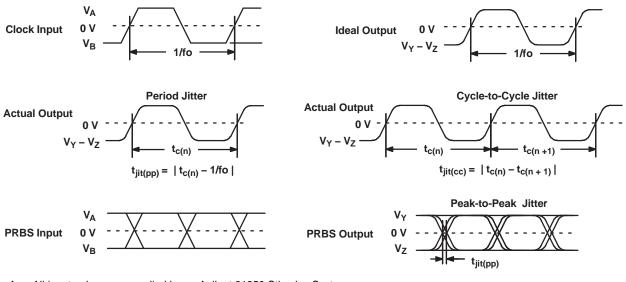


Figure 6. Propagation Delay Input to Output



- A. All input pulses are supplied by an Agilent 81250 Stimulus System.
- B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software.

Figure 7. Driver Jitter Measurement Waveforms

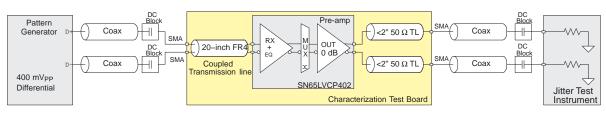


Figure 8. AC Test Circuit — Jitter and Output Rise Time Test Circuit

The SN65LVCP402 input equalizer provides 5-dB frequency gain to compensate for frequency loss of a shorter backplane transmission line. For characterization purposes, a 24-inch FR-4 coupled transmission line is used in place of the backplane trace. The 24-inch trace provides roughly 5 dB of attenuation between 375 MHz and 1.875 GHz, representing closely the characteristics of a short backplane trace. The loss tangent of the FR4 in the test board is 0.018 with an effective $\epsilon(r)$ of 3.1.

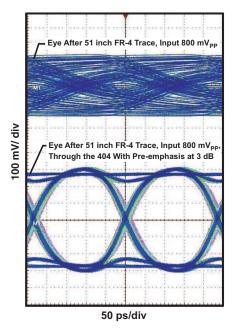
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SN65LVCP402

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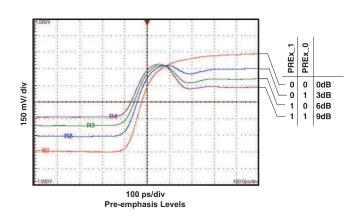
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TYPICAL DEVICE BEHAVIOR



NOTE: 51 Inch (128.54 cm) Input Trace, dR = 4.25 Gbps; 2⁷⁻¹ PRBS **Figure 9. Data Input and Output Pattern**







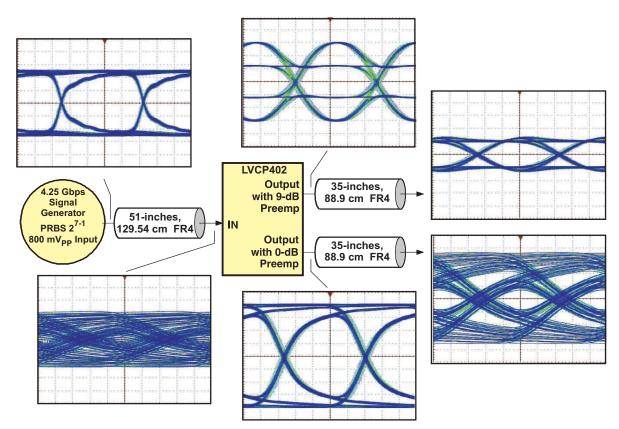


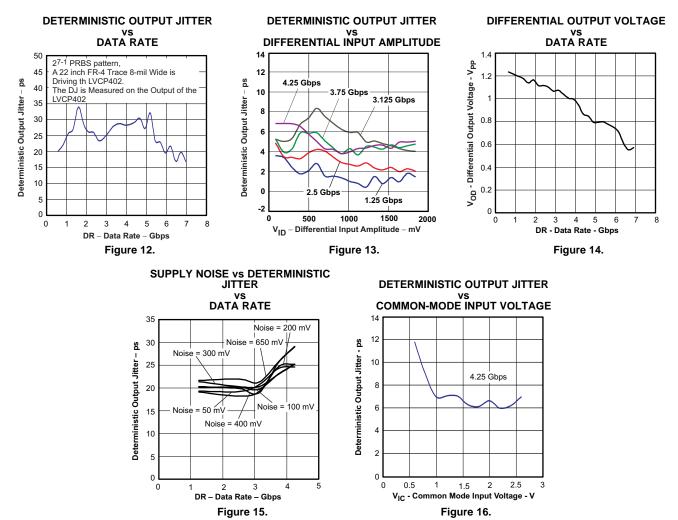
Figure 11. Data Output Pattern

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INSTRUMENTS

TYPICAL CHARACTERISTICS





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APPLICATION INFORMATION

BANDWIDTH REQUIREMENTS

Error free transmission of data over a transmission line has specific bandwidth demands. It is helpful to analyze the frequency spectrum of the transmit data first. For an 8B10B coded data stream at 3.75 Gbps of random data, the highest bit transition density occurs with a 1010 pattern (1.875 GHz). The least transition density in 8B10B allows for five consecutive ones or zeros. Hence, the lowest frequency of interest is 1.875 GHz/5 = 375 MHz. Real data signals consist of higher frequency components than sine waves due to the fast rise time. The faster the rise time, the more bandwidth becomes required. For 80-ps rise time, the highest important frequency component is at least $0.6/(\pi \times 80 \text{ ps}) = 2.4 \text{ GHz}$. Figure 17shows the Fourier transformation of the 375-MHz and 1.875-GHz trapezoidal signal.

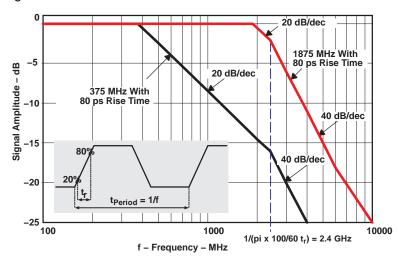


Figure 17. Approximate Frequency Spectrum of the Transmit Output Signal With 80 ps Rise Time

The spectrum analysis of the data signal suggests building a backplane with little frequency attenuation up to 2 GHz. Practically, this is achievable only with expensive, specialized PCB material. To support material like FR4, a compensation technique is necessary to compensate for backplane imperfections.

EXPLANATION OF EQUALIZATION

Backplane designs differ widely in size, layer stack-up, and connector placement. In addition, the performance is impacted by trace architecture (trace width, coupling method) and isolation from adjacent signals. Common to most commercial backplanes is the use of FR4 as board material and its related high-frequency signal attenuation. Within a backplane, the shortest to longest trace lengths differ substantially – often ranging from 8 inches up to 40 inches. Increased loss is associated with longer signal traces. In addition, the backplane connector often contributes a good amount of signal attenuation. As a result, the frequency signal attenuation for a 300-MHz signal might range from 1 dB to 4 dB while the corresponding attenuation for a 2-GHz signal might span 6 dB to 24 dB. This frequency dependent loss causes distortion jitter on the transmitted signal. Each LVCP402 receiver input incorporates an equalizer and compensates for such frequency loss. The SN65LVCP402 equalizer provides 5/12 dB of frequency gain between 375 MHz and 1.875 GHz, compensating roughly for 20 inches of FR4 material with 8-mil trace width. Distortion jitter improvement is substantial, often providing more than 30-ps jitter reduction. The 5-dB compensation is sufficient for most short backplane traces. For longer trace lengths, it is recommended to enable transmit preemphasis in addition.



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SETTING THE PREEMPHASIS LEVEL

The receive equalization compensates for ISI. This reduces jitter and opens the data eye. In order to find the best preemphasis setting for each link, calibration of every link is recommended. Assuming each link consists of a transmitter (with adjustable pre-emphasis such as LVCP402) and the LVCP402 receiver, the following steps are necessary:

- 1. Set the transmitter and receiver to 0-dB preemphasis; record the data eye on the LVCP402 receiver output.
- 2. Increase the transmitter preemphasis until the data eye on the LVCP402 receiver output looks the cleanest.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65LVCP402RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
SN65LVCP402RGERG4	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
SN65LVCP402RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
SN65LVCP402RGETG4	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

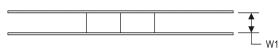
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TEXAS INSTRUMENTS





TAPE AND REEL INFORMATION

TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

1	All dimensions are nominal												
	Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	SN65LVCP402RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
	SN65LVCP402RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

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PACKAGE MATERIALS INFORMATION

6-Jan-2012



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVCP402RGER	VQFN	RGE	24	3000	346.0	346.0	29.0
SN65LVCP402RGET	VQFN	RGE	24	250	210.0	185.0	35.0

MECHANICAL DATA



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No-Leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions. F. Falls within JEDEC MO-220.
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RGE (S-PVQFN-N24)

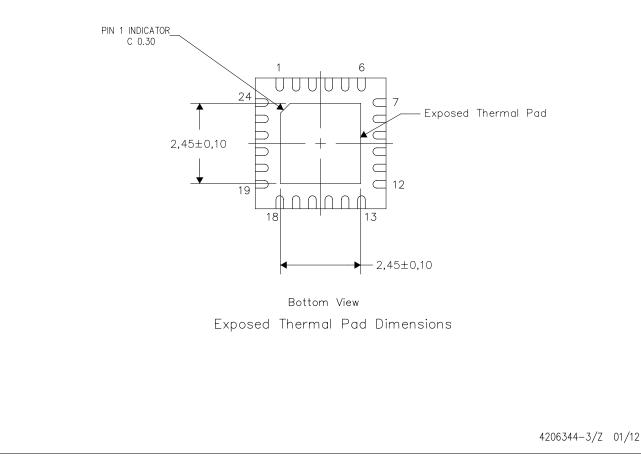
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

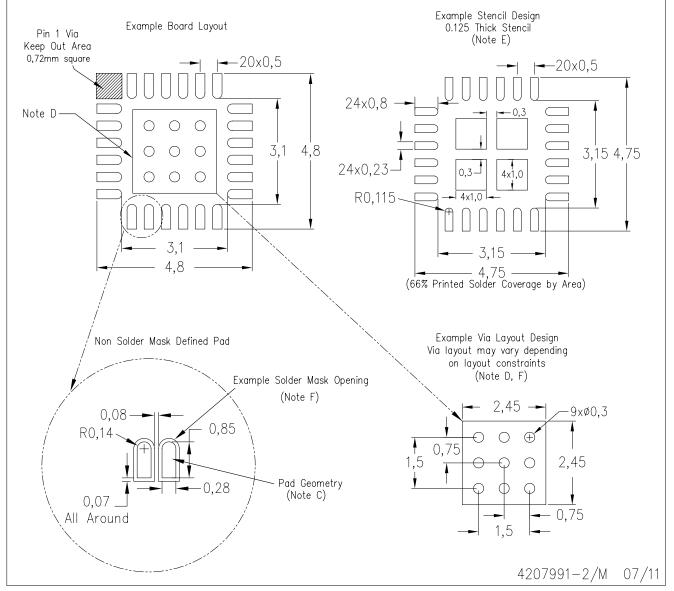


NOTES: A. All linear dimensions are in millimeters



RGE (S-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- : A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.



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