ENC28J60

ENC28J60 Rev. B1 Silicon Errata

The ENC28J60 (Rev. B1) parts you have received conform functionally to the Device Data Sheet (DS39662**B**), except for the anomalies described below. Any data sheet clarification issues related to this device will be reported in a separate data sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to ENC28J60 devices with the following revision identifier:

Part Number	Device Revision (EREVID)
ENC28J60	0000 0010

EREVID is located at address 0312h in the device's memory register space.

1. Module: MAC Interface

When the SPI clock from the host microcontroller is run at frequencies of less than 8 MHz, reading or writing to the MAC registers may be unreliable.

Work around 1

Run the SPI at frequencies of at least 8 MHz.

Work around 2

Generate an SPI clock of 25/2 (12.5 MHz), 25/3 (8.333 MHz), 25/4 (6.25 MHz), 25/5 (5 MHz), etc., and synchronize with the 25 MHz clock entering OSC1 on the ENC28J60. This could potentially be accomplished by feeding the same 25 MHz clock into the ENC28J60 and host controller. Alternatively, the host controller could potentially be clocked off of the CLKOUT output of the ENC28J60.

2. Module: Reset

After sending an SPI Reset command, the PHY clock is stopped but the ESTAT.CLKRDY bit is not cleared. Therefore, polling the CLKRDY bit will not work to detect if the PHY is ready.

Additionally, the hardware start-up time of 300 μs may expire before the device is ready to operate.

Work around

After issuing the Reset command, wait for at least 1 ms in firmware for the device to be ready.

3. Module: Core (Operating Specifications)

The device data sheet specifies that industrial operating temperature range (-40°C to +85°C) is supported. However, this silicon revision only supports the commercial temperature range (0°C to +70°C).

Work around

None at this time.

4. Module: Oscillator (CLKOUT Pin)

No output is available on CLKOUT during Power Save mode (ECON2.PWRSV = 0).

Work around

If the host controller uses the CLKOUT signal as the system clock, do not enable Power Save mode.

5. Module: Memory (Ethernet Buffer)

The receive hardware maintains an internal Write Pointer which defines the area in the receive buffer where bytes arriving over the Ethernet are written. This internal Write Pointer should be updated with the value stored in ERXST whenever the Receive Buffer Start Pointer, ERXST, or the Receive Buffer End Pointer, ERXND, is written to by the host microcontroller. Sometimes, when ERXST or ERXND is written to, the exact value, 0000h, is stored in the internal receive Write Pointer instead of the ERXST address.

Work around

Use the lower segment of the buffer memory for the receive buffer, starting at address 0000h. For example, use the range (0000h to n) for the receive buffer and ((n + 1) – 8191) for the transmit buffer.

6. Module: Interrupts

The Receive Packet Pending Interrupt Flag (EIR.PKTIF) does not reliably/accurately report the status of pending packets.

Work around

In the Interrupt Service Routine, if it is unknown if a packet is pending and the source of the interrupt, switch to Bank 1 and check the value in EPKTCNT.

If polling to see if a packet is pending, check the value in EPKTCNT.

Note: This errata applies only to the interrupt flag. If the receive packet pending interrupt is enabled, the $\overline{\text{INT}}$ pin will continue to reliably become asserted when a packet arrives. The receive packet pending interrupt is cleared in the same manner described in the data sheet.

7. Module: PHY

The automatic polarity detection and correction features of the PHY layer do not work as described. This may cause poor receive network performance, or no receive activity, with some link partners.

Work around

When designing the application, always verify that the TPIN+ and TPIN- pins are connected correctly.

8. Module: PHY

The external resistor value recommended for RBIAS in the current data sheet does not apply to this revision of silicon.

Work around

Rev. B1 silicon requires that a 2.7 kΩ, 1% external resistor be attached from the RBIAS pin to ground.

Note: ENC28J60 Rev. B1 and Rev. B4 silicon require a 2.70 kΩ RBIAS resistor. Rev. B5 requires a 2.32 kΩ RBIAS resistor. Using an incorrect resistor value will cause the Ethernet transmit waveform to violate IEEE 802.3 specification requirements.

9. Module: PHY

The PHY Half-Duplex Loopback mode, enabled when PHCON1.PDPXMD = 0, PHCON2.HDLDIS = 0, PHCON2.FRCLNK = 1 or a link partner is connected, does not loop packets back to itself reliably.

Work around

Perform loopback diagnostics in full duplex using an external loopback connector/cable. To avoid looping occasional packets back to one self, PHCON2.HDLDIS should be set by the host controller. PHCON2.HDLDIS is clear by default.

10. Module: PHY

The PHY Full-Duplex Loopback mode, enabled when PHCON1.PDPXMD = 1 and PHCON1.PLOOPBK = 1, does not loop packets back to itself reliably.

Work around

Perform loopback diagnostics in full duplex using an external loopback connector/cable.

11. Module: PHY LEDs

When the PHLCON register is programmed to output the duplex status and collision activity on the same LED (1110b), only the duplex status will be displayed (i.e., the LED will be illuminated when in Full-Duplex mode and extinguished when in Half-Duplex mode, regardless of collision activity).

Work around

When Half-Duplex mode is being used, program the PHLCON register's LxCFG bits with '0011b' to display the collision status. When Full-Duplex mode is being used, program the PHLCON register's LxCFG bits with '0101b' to display the duplex status.

12. Module: Transmit Logic

In Half-Duplex mode, a hardware transmission abort caused by excessive collisions, a late collision or excessive deferrals, may stall the internal transmit logic. The next packet transmit initiated by the host controller may never succeed (ECON1.TXRTS will remain set indefinitely).

Work around

Before attempting to transmit a packet (setting ECON1.TXRTS), reset the internal transmit logic by setting ECON1.TXRST and then clearing ECON1.TXRST. The host controller may wish to issue this Reset before any packet is transmitted (for simplicity), or it may wish to conditionally reset the internal transmit logic based on the Transmit Error Interrupt Flag (EIR.TXERIF), which will become set whenever a transmit abort occurs. Clearing ECON1.TXRST may cause a new transmit error interrupt event (EIR.TXERIF will become set). Therefore, the interrupt flag should be cleared after the Reset is completed.

13. Module: Memory (Ethernet Buffer)

The receive hardware may corrupt the circular receive buffer (including the Next Packet Pointer and receive status vector fields) when an even value is programmed into the ERXRDPTH:ERXRDPTL registers.

Work around

Ensure that only odd addresses are written to the ERXRDPT registers. Assuming that ERXND contains an odd value, many applications can derive a suitable value to write to ERXRDPT by subtracting one from the Next Packet Pointer (a value always ensured to be even because of hardware padding) and then compensating for a potential ERXST to ERXND wraparound. Assuming that the receive buffer area does not span the 1FFFh to 0000h memory boundary, the logic in Example 1 will ensure that ERXRDPT is programmed with an odd value:

EXAMPLE 1:

```
if (Next Packet Pointer – 1 < ERXST) or
(Next Packet Pointer – 1 > ERXND)
    then:
ERXRDPT = ERXND
    else:
ERXRDPT = Next Packet Pointer – 1
```

14. Module: Transmit Logic

If a collision occurs after 64 bytes have been transmitted, the transmit logic may not set the Late Collision Error bit (ESTAT.LATECOL).

Work around

Whenever a late collision has potentially occurred (both EIR.TXERIF and ESTAT.TXABRT bits will be set), read the transmit status vector and check the transmit late collision bit (bit 29).

15. Module: PHY

With some LEDs, the LED auto-polarity detection circuit misdetects the connected polarity of the LED upon Reset. As a result, the LED output pin will sink current when it should be sourcing current and vice versa. The LED will visually appear inverted. For example, an LED configured to display the link status will be illuminated when no link is present and extinguished when a link has been established. The likelihood of a misdetection will vary over temperature. If LEDB is misdetected, the PHCON1.PDPXMD bit will also reset to the incorrect state.

Work around

Place a resistor in parallel with the LED. The resistor value needed is not critical. Resistors between 1 kΩ and 100 kΩ are recommended.

16. Module: DMA

If the DMA module is operated in Checksum mode (ECON1.CSUMEN, DMAST = 1) at any time while a packet is currently being received from the Ethernet (ESTAT.RXBUSY = 1), the packet being received will be aborted. The packet abort will cause the Receive Error Interrupt Flag (EIR.RXERIF) to be set, the interrupt will occur, if enabled, and the Buffer Error status bit (ESTAT.BUFER) will also become set. The packet will be permanently lost.

Work around

Do not use the DMA module to perform checksum calculations; perform checksums in software. This problem does not affect the DMA copy operation (ECON1.CSUMEN = 0).

Ethernet Conformance Issues

In testing the ENC28J60 device (Revision B1 silicon) for compliance with IEEE Standard 802.3, the following conformance issues have been noted. All of these will be addressed in future revisions of the ENC28J60 silicon.

1. Issue: TP_IDL Pattern

The observed TP_IDL pattern transmitted by ENC28J60 was observed to not stay within the standard defined template when using the TPM (Twisted Pair Model) and TP Test Load 2.

Reference: IEEE Std 802.3, §14.3.1.2.1, Figures 14-10 and 14-11

Potential Application Impact

The TP_IDL test requires a total of six separate sub tests, using three different test loads with and without TPM. The fact that the device consistently passed five of the six sub tests, while narrowly missing the sixth, leads to the conclusion that this is a minor issue. No failures have been observed due to this issue.

Work around

None.

2. Issue: Exiting Link Test Fail State

The ENC28J60 was observed to improperly accept a frame with no preceding LTPs (Link Test Pulse). When a device is in the Link Test Fail state, it should exit this state when a valid packet is received, however, the first packet should not be accepted. The second and subsequent packets should be accepted while the device is in the Link Test Pass state.

Reference: IEEE Std 802.3, Figure 14-6

Potential Application Impact

Link Test Pulse is an integral part of every 10Base-T system. It is used to notify a link partner of the presence of a 10Base-T device. An absence of LTPs signifies that the Ethernet cable is not connected or a link partner is missing. Even when a cable is not connected, a 10Base-T device would continuously send out LTPs. This fact makes it unlikely that there will ever be a situation in which a device would be receiving valid Ethernet frames without already being in the Link Test Pass state.

In the unlikely event that this situation does occur, higher layer protocols would protect the system from accepting unwanted data. It is unlikely that this failure will have significant impact on a networked application. No failures have been observed due to this issue.

Work around

None.

3. Issue: Collision Handling

The delay from the collision event to collision enforcement with the jam pattern is approximately 50 BT (Bit Times), which is greater than the specified limit of 36 BT.

Reference: IEEE Std 802.3, Annex B, § B.1.2

Potential Application Impact

A collision in a half-duplex 10Base-T is not an unexpected event. It exists as a normal part of the network operation. The purpose of the jam pattern is to ensure that the duration of the collision is sufficient to be noticed by the other transmitting station(s) involved in the collision. A longer delay between the collision event and the start of jam pattern would cause the duration of the collision to be longer.

After each collision, both transmitting stations would back off and wait a random amount of time before attempting to transmit again. The minimum Idle time between each Ethernet frame is 9.6 μs. The longer collision duration of 14 BT, or 1.4 μs, can be considered as a small fraction of time wasted for each collision. It is unlikely that this issue will have significant impact on networked applications. No failures have been observed due to this issue.

Work around

None.

REVISION HISTORY

Rev A Document (12/2005)

Original revision. Silicon errata issues 1 (MAC Interface), 2 (Reset), 3 (Core), 4 (Oscillator), 5 (Memory) and 6 (Interrupts), and Ethernet Conformance issues 1 (TP_IDL Pattern), 2 (Exiting Link Test Fail State) and 3 (Collision Handling).

Rev B Document (2/2006)

Added silicon errata issues 7-10 (PHY), 11 (PHY LEDs), 12 (Transmit Logic) 13 (Memory – Ethernet Buffer) and 14 (MAC).

Rev C Document (8/2006)

Updated Silicon errata issues 1 (MAC Interface), 5 (Memory – Ethernet Buffer), 6 (Interrupts), 8 (PHY) and 12 (Transmit Logic). Removed Silicon issue 14 (MAC) and added new silicon issue, now 14 (Transmit Logic).

Rev D Document (9/2006)

Added silicon issue 15 (PHY).

Rev E Document (10/2006)

Added silicon issue 16 (DMA).

NOTES:

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