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HIGH-SPEED CMOS LOGIC HEX INVERTER

Check for Samples: CD74HCU04-Q1

FEATURES PW PACKAGE Qualified for Automotive Applications (TOP VIEW) **Wide Operating Temperature Range:** 1A □□ $\square V_{cc}$ -40°C to 125°C 1Y 📖 2 **□** 6A **Balanced Propagation Delay and Transition** 2A 🖂 3 **Ⅲ** 6Y **Times Ⅲ** 5A **Significant Power Reduction Compared to** 3A ____ 5 LSTTL Logic ICs 3Y 🖂 **Ⅲ** 4A HCU Types GND □□ ☐ 4Y

DESCRIPTION

- 2-V to 6-V Operation

CMOS Input Compatibility: I₁ ≤ 1µA at V_{OL}, V_{OH}

The CD74HCU04 unbuffered hex inverter utilizes silicon-gate CMOS technology to achieve operation speeds similar to LSTTL gates, with the low power consumption of standard CMOS integrated circuits. These devices especially are useful in crystal oscillator and analog applications.

ORDERING INFORMATION

| T _A | PACI | KAGE | ORDERABLE PART NUMBER | TOP-SIDE MARKING | |
|----------------|------------|--------------|-----------------------|------------------|--|
| -40°C to 125°C | TSSOP - PW | Reel of 2000 | CD74HCU04QPWRQ1 | HJU04Q | |

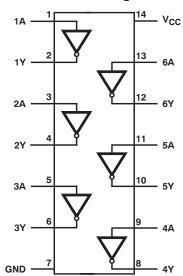


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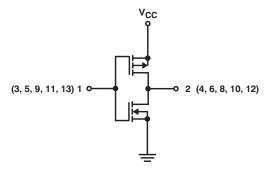
Functional Diagram



Logic Symbol



Schematic Diagram





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ABSOLUTE MAXIMUM RATINGS(1)(2)

| V_{CC} | DC supply voltage | -0.5V to +7V |
|------------------|---|----------------|
| I_{IK} | DC input diode current, $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ | ±20mA |
| I _{OK} | DC output diode current, $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ | ±20mA |
| Io | DC drain current per output, $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ | ±25mA |
| I _{CC} | DC VCC or ground current | ±50mA |
| θ_{JA} | Thermal impedance, junction to free air (3) | 112.6°C/W |
| T_{J} | Maximum junction temperature | 150°C |
| T _{Stg} | Storage temperature range | -65°C to 150°C |

⁽¹⁾ Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

| | | MIN | MAX | UNIT |
|----------------|--------------------------------|-----|----------|------|
| V_{CC} | Supply voltage | 2 | 6 | V |
| V_{I} | Input voltage | 0 | V_{CC} | V |
| Vo | Output voltage | 0 | V_{CC} | V |
| T _A | Operating free-air temperature | -40 | 125 | °C |

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| | PARAMETER | TEST COM | V _{cc} | T _A = 25°C | | T _A = -40 to 125°C | | UNIT | | | | | |
|-----------------------|---------------------------------------|------------------------------------|--|-----------------------|------|----------------------------------|-----|------|-----|---|-----|--|-----|
| | | V ₁ (V) | V _I (V) I _O (mA) | | MIN | MAX | MIN | MAX | | | | | |
| | | | | 2 | 1.7 | | 1.7 | | | | | | |
| V_{IH} | High level input voltage | _ | _ | 4.5 | 3.6 | | 3.6 | | V | | | | |
| | | | | 6 | 4.8 | | 4.8 | | | | | | |
| | | | | 2 | | 0.3 | | 0.3 | | | | | |
| V_{IL} | Low level input voltage | _ | _ | 4.5 | | 0.8 | | 0.8 | V | | | | |
| | | | | 6 | | 1.1 | | 1.1 | | | | | |
| | High level output voltage, CMOS loads | V _{IH} or V _{IL} | | 2 | 1.8 | | 1.8 | | V | | | | |
| V _{OH(CMOS)} | | | -0.02 | 4.5 | 4 | | 4 | | | | | | |
| | | | | | | | | | | 6 | 5.5 | | 5.5 |
| \ / | High level output voltage, TTL loads | V OND | -4 | 4.5 | 3.98 | | 3.7 | | | | | | |
| $V_{OH(TTL)}$ | | V _{CC} or GND | -5.2 | 6 | 5.48 | | 5.2 | | V | | | | |
| | | | | 2 | | 0.2 | | 0.2 | | | | | |
| V _{OL(CMOS)} | Low level output voltage, CMOS loads | V _{IH} or V _{IL} | 0.02 | 4.5 | | 0.5 | | 0.5 | V | | | | |
| , , | loads | | | | 6 | | 0.5 | | 0.5 | | | | |
| V _{OL(TTL)} | Low level output voltage, TTL |)/ OND | 4 | 4.5 | | 0.26 | | 0.4 | | | | | |
| | loads | V _{CC} or GND | 5.2 | 6 | | 0.26 | | 0.4 | V | | | | |
| I _I | Input leakage current | V _{CC} or GND | _ | 6 | | ±0.1 | | ±1 | μΑ | | | | |
| I _{CC} | Quiescent device current | V _{CC} or GND | 0 | 6 | | 2 | | 40 | μΑ | | | | |

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⁽²⁾ All voltages are referenced to ground.

⁽³⁾ The package thermal impedance is calculated in accordance with JESD 51-7.



SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| | PARAMETER | TEST | V | T, | _A = 25°C | T _A = -40 to 125°C | UNIT |
|-------------------------------------|---|-----------------------|-----------------|-----|---------------------|-------------------------------|------|
| | PARAMETER | CONDITIONS | V _{CC} | MIN | TYP MAX | MIN MAX | UNII |
| | Propagation delay, input to output Y (see Figure 1) | C _L = 50pF | 2 | | 70 | 105 | ns |
| t _{PLH} , t _{PHL} | | $C_L = 50pF$ | 4.5 | | 14 | 21 | |
| | | $C_L = 50pF$ | 6 | | 12 | 18 | |
| | Transition times (see Figure 1) | C _L = 50pF | 2 | | 75 | 110 | |
| t _{TLH} , t _{THL} | | | 4.5 | | 15 | 22 | ns |
| | | | 6 | | 13 | 19 | |
| C _I | Input capacitance | _ | _ | | See Figure | 3 | |
| C _{PD} | Power dissipation capacitance (1)(2) | _ | 5 | | 14 | | pF |

TEST WAVEFORMS

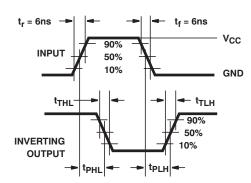


Figure 1. HC and HCU Transition Times and Propagation Delay Times, Combination Logic

ISTRUMENTS

⁽¹⁾ C_{PD} is used to determine the dynamic power consumption, per inverter. (2) $P_D = V_{CC2} \times f_i (C_{PD} + C_L)$, where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage



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TYPICAL PERFORMANCE CURVES

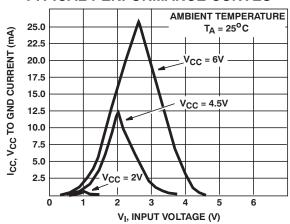


Figure 2. Typical Inverter Supply Current as a Function of Input Voltage

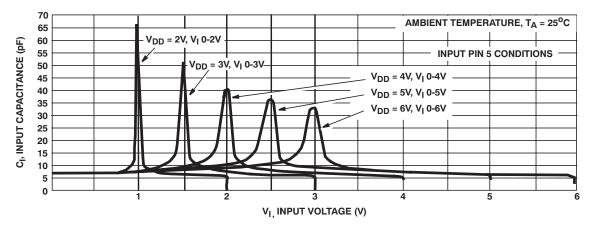


Figure 3. Input Capacitance as a Function of Input Voltage

15-Jul-2010

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|------------|--------------|--------------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| CD74HCU04QPWRQ1 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF CD74HCU04-Q1:

Catalog: CD74HCU04

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





| A0 | Dimension designed to accommodate the component width |
|----|---|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|-----------------|--------------------|----|------|--------------------------|--------------------------|------------|------------|------------|------------|-----------|------------------|
| CD74HCU04QPWRQ1 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HCU04QPWRQ1 | TSSOP | PW | 14 | 2000 | 346.0 | 346.0 | 29.0 |

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
 - Sody length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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