



#### **General Description**

The MAX14500-MAX14503 USB-to-SD™ card readers provide a means for portable devices that support fullspeed USB communication (12Mbps) with one or two SD card slots, upgrading the USB SD card reader function to USB Hi-Speed (480Mbps) operation. The MAX14500-MAX14503 have two modes of operation: Pass Thru and Card Reader. In pass thru, the SD and USB signals pass through the MAX14500-MAX14503 without modification, appearing like the device is not present. The host microprocessor firmware does not need modification, as there is no change from the host microprocessor's perspective. In Card Reader mode, the MAX14500-MAX14503 implement a Hi-Speed USB card reader that operates independently of the host microprocessor. All the capabilities of the full-speed USB port and SD card slot are preserved with the additional feature that allows a faster way for a PC to read or write to the SD card. The MAX14500-MAX14503 support SD high capacity SDHC cards. The 40-pin TQFN version supports one SD card, while the 56-bump WLP version supports two SD cards.

The MAX14500-MAX14503 feature advanced powersaving modes to reduce power consumption in portable applications. The low-power Sleep modes allow the ability to disable internal circuit blocks, providing power-saving operating modes. The default clock input for each part number is specified in the ordering information. The MAX14500-MAX14503 feature the option to change the default values using the I<sup>2</sup>C interface.

The MAX14500-MAX14503 are available in 5mm x 5mm, 40-pin TQFN, and 3.23mm x 3.5mm, 56-bump WLP packages. These devices operate over a wide supply voltage range and are specified over the -40°C to +85°C extended temperature range.

#### Applications

Cell Phones **PDAs** MP3 Players Digital Still Cameras **GPS** 

#### **Features**

- ♦ USB 2.0 Hi-Speed and Full-Speed Compliant
- **♦ SDHC Card Support**
- ♦ Internal Hi-Speed USB SD Card Reader Eases Host µP Overhead
- ♦ On-Chip Termination and Pullup Resistors
- ♦ Internal SD Switches Allow For Multiplexing Two SD Cards on a Single-Microprocessor SD Port
- **♦** Accommodates Clock Input Frequencies 26MHz, 19.2MHz, 13MHz, and 12MHz
- ♦ Internal Clock Squarer for Low-Amplitude TCXO **Signals**
- ♦ No Power-Supply Sequencing Required
- ♦ Compatible with +1.8V to +3.3V I/O Host Microprocessor
- ♦ Simple Control Mode Requires Only a Single **GPIO**
- ♦ I<sup>2</sup>C Control Provides Multiple Configuration **Options**
- ♦ I<sup>2</sup>C Control Required for Two SD Cards
- ♦ On-Chip Power-On Reset/Brown-Out Reset

### Ordering Information/ **Selector Guide**

PART	INPUT FREQUENCY (MHz)	SD CARDS	PIN- PACKAGE
MAX14500ETL+*	12	1	40 TQFN-EP**
MAX14500AEWN+*	12	2	56 WLP
MAX14501ETL+*	13	1	40 TQFN-EP**
MAX14501AEWN+*	13	2	56 WLP
MAX14502AETL+	19.2	1	40 TQFN-EP**
MAX14502AEWN+*	19.2	2	56 WLP
MAX14503ETL+*	26	1	40 TQFN-EP**
MAX14503AEWN+*	26	2	56 WLP

Note: All devices are specified over the -40°C to +85°C operating temperature range.

SD is a trademark of the SD Card Association.

<sup>+</sup>Denotes a lead(Pb)-free/RoHS-compliant package.

<sup>\*</sup>Future product—contact factory for availability.

<sup>\*\*</sup>EP = Exposed pad.

#### **ABSOLUTE MAXIMUM RATINGS**

(All voltages referenced to GND.)
V <sub>C</sub> C0.3V to +4V
V <sub>SD</sub> 0.3V to +4V
V <sub>IO</sub> 0.3V to +4V
V <sub>TM</sub> 0.3V to +4V
KVBUS0.3V to +4V
CLDO0.3V to +2V
CDAT1_[3:0], HDAT1_[3:0], CCMD1, HCMD1, CCLK1, HCLK1,
CCRD_PRST, HCRD_PRST, CDAT2_[3:0], HDAT2_[3:0],
CCMD2, HCMD2, CCLK2, HCLK20.3V to (V <sub>SD</sub> + 0.3V)
BUSY, BERR/INT, MODE, SCL, SDA, I2C_SEL,
ADD, RST0.3V to (V <sub>IO</sub> + 0.3V)

CD+, CD-, HD+, HD-, RREF, FREF0.3V to $(V_{TM} + 0.3V)$
Continuous Power Dissipation ( $T_A = +70^{\circ}C$ )
40-Pin TQFN (derate 35.7mW/°C above +70°C)2857mW
Junction-to-Case Thermal Resistance (θ <sub>JC</sub> ) (Note 1)
40-Pin TQFN1.7°C/W
Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> ) (Note 1)
40-Pin TQFN28°C/W
Operating Temperature Range40°C to +85°C
Junction Temperature+150°C
Storage Temperature Range65°C to +160°C
Lead Temperature (soldering, 10s)+300°C

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to <a href="https://www.maxim-ic.com/thermal-tutorial">www.maxim-ic.com/thermal-tutorial</a>.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### **ELECTRICAL CHARACTERISTICS**

 $(V_{CC} = +2.4 V \ to \ +3.6 V, \ V_{SD} = +2.4 V \ to \ +3.6 V, \ V_{IO} = +1.5 V \ to \ +3.6 V, \ V_{TM} = +2.91 V \ to \ +3.4 V, \ T_A = -40 ^{\circ} C \ to \ +85 ^{\circ} C, \ unless \ otherwise \ noted. Typical values are at V_{CC} = +3.3 V, V_{IO} = +2.5 V, V_{SD} = +2.5 V, V_{TM} = +3.3 V, T_A = +25 ^{\circ} C.) \ (Note 2)$ 

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
		Pass thru	2.1		3.6	
V <sub>CC</sub> Supply Voltage	V <sub>CC</sub>	Card reader active, f <sub>CCLK</sub> ≤ 26MHz	2.1		3.6	V
		Card reader active, f <sub>CCLK</sub> > 26MHz	2.4		3.6	
		Pass thru	2.0		3.6	
V <sub>SD</sub> Supply Voltage	V <sub>SD</sub>	Card reader active, f <sub>CCLK</sub> ≤ 26MHz	2.0		3.6	V
		Card reader active, f <sub>CCLK</sub> > 26MHz	2.4		3.6	
Logic Interface Supply Voltage	V <sub>IO</sub>		1.5		3.6	V
USB Supply Voltage	V <sub>TM</sub>		2.91		3.4	V
Digital Core LDO Regulator Output Voltage	V <sub>CLDO</sub>	C <sub>CLDO</sub> = 1.0µF		1.8		V
V 0 10 1	1	Pass thru		5	15	μΑ
V <sub>CC</sub> Supply Current	Icc	Card reader active		35	50	mA
Van Supply Current	la-	Pass thru		17	40	μΑ
V <sub>SD</sub> Supply Current	ISD	Card reader active		3		mA
V <sub>IO</sub> Supply Current	lio	Pass thru		2	10	μΑ
VIO Supply Current	110	Card reader active		0.2		mA
V <sub>TM</sub> Supply Current	I <sub>TM</sub>	Pass thru		13	50	μΑ
VIM Supply Current	1	Card reader active		25		mA
V <sub>SD</sub> Comparator Threshold	VSDCT		1.0	1.5	1.9	V
V <sub>TM</sub> Comparator Threshold	V <sub>TMCT</sub>		2.0	2.5	2.9	V
MODE, I2C_SEL, ADD, RST Input-Voltage Low	V <sub>IL</sub>				0.4	V

### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{CC} = +2.4 \text{V to } +3.6 \text{V}, V_{SD} = +2.4 \text{V to } +3.6 \text{V}, V_{IO} = +1.5 \text{V to } +3.6 \text{V}, V_{TM} = +2.91 \text{V to } +3.4 \text{V}, T_{A} = -40 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C}, \text{ unless otherwise noted.}$  Typical values are at  $V_{CC} = +3.3 \text{V}, V_{IO} = +2.5 \text{V}, V_{SD} = +2.5 \text{V}, V_{TM} = +3.3 \text{V}, T_{A} = +25 ^{\circ}\text{C}.)$  (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MODE, I2C_SEL, ADD, RST Input-Voltage High	VIH		2/3 x V <sub>IO</sub>			V
BUSY, BERR/INT Output-Voltage Low	V <sub>OL</sub>	I <sub>LOAD</sub> = 1mA			0.4	V
BUSY, BERR/INT Output-Voltage High	VoH	I <sub>LOAD</sub> = -1mA	V <sub>IO</sub> - 0.4			V
I2C_SEL, ADD, RST Input Leakage Current	I <sub>IL</sub>		-1		+1	μΑ
MODE Input Resistance to GND	RMODE		150	300	500	kΩ
FREF Full-Swing Input-Voltage High	VIH		1.3			V
FREF Full-Swing Input-Voltage Low	VIL				0.4	V
FREF Low-Amplitude Input- Voltage Low	VIL		200			mV
FREF Input Leakage Current	lilF	Full-Swing mode	-10		+10	μΑ
FREF Input Resistance		Low-Amplitude input mode		1		ΜΩ
KVBUS Comparator Threshold	V <sub>TH</sub>		1.0	1.25	1.5	V
KVBUS Comparator Hysteresis	V <sub>HYS</sub>			20		mV
KVBUS Comparator Input Impedance	R <sub>IN</sub>		10			МΩ
SDA/SCL Input Low Voltage	V <sub>IL_I2C</sub>				0.3 x V <sub>IO</sub>	V
SDA/SCL Input High Voltage	V <sub>IH</sub> _I2C		0.7 x V <sub>IO</sub>			V
		V <sub>IO</sub> > +2V, 3mA sink current	0		0.4	
SDA Output Logic-Low	V <sub>OL_I2C</sub>	V <sub>IO</sub> ≤ +2V, 3mA sink current	0		0.2 x V <sub>IO</sub>	V
SDA/SCL Input Leakage Current	I <sub>IN_I2C</sub>		-10		+10	μΑ
SD CARD INTERFACE						
On-Resistance	Ron	V <sub>TEST</sub> = 0 or V <sub>SD</sub> , I <sub>TEST</sub> = 10mA (Note 3)		10		Ω
Off-Leakage Current	lilsd	V <sub>TEST</sub> = 0 or V <sub>SD</sub> (Note 3)	-1		+1	μΑ
Off-Capacitance	C <sub>SD_OFF</sub>	(Note 4)		5		рF
On-Capacitance	C <sub>SD_ON</sub>	(Note 5)		10		рF
Pullup Resistance	R <sub>PU</sub>	CCMD1, CCMD2, CDAT1_[3:0], CDAT2_[3:0]	50	75	100	kΩ
Output High Voltage	VoH	I <sub>OH</sub> = -100μA	0.75 x V <sub>SD</sub>			V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 100μA			0.125 x V <sub>SD</sub>	V

### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{CC} = +2.4 \text{V to } +3.6 \text{V}, V_{SD} = +2.4 \text{V to } +3.6 \text{V}, V_{IO} = +1.5 \text{V to } +3.6 \text{V}, V_{TM} = +2.91 \text{V to } +3.4 \text{V}, T_{A} = -40 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C}, \text{ unless otherwise noted.}$  Typical values are at  $V_{CC} = +3.3 \text{V}, V_{IO} = +2.5 \text{V}, V_{SD} = +2.5 \text{V}, V_{TM} = +3.3 \text{V}, T_{A} = +25 ^{\circ}\text{C}.)$  (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
	.,,	V <sub>SD</sub> < 2.4V	0.8 x V <sub>SD</sub>			
Input High Voltage	V <sub>IH</sub>	V <sub>SD</sub> ≥ 2.4V	0.625 x V <sub>SD</sub>			V
		V <sub>SD</sub> < 2.4V			0.2 x V <sub>SD</sub>	
Input Low Voltage	VIL	V <sub>SD</sub> ≥ 2.4V			0.25 x V <sub>SD</sub>	V
USB INTERFACE						
On-Resistance	Ron	V <sub>CD</sub> = 0 or V <sub>TM</sub> , switch closed		5		Ω
On-Resistance Flatness	RONFLAT	$V_{CD} = 0 \text{ to } 3.3V, V_{TM} = +3.3V$		2		Ω
On-Capacitance	C <sub>ON_USB</sub>	Switch closed, measured from CD+ and CD-		12		pF
Off-Capacitance	Coff_usb	Switch open, measured from CD+, CD-, HD+, HD-		6		pF
AC CHARACTERISTICS (Note 6)						
SD CARD CLOCK TIMING (CCL	(_), DEFAULT	SPEED (Figure 5a)				
Clock Low Time	tw∟	$C_L = 10pF$	19			ns
Clock High Time	twH	$C_L = 10pF$	19			ns
Clock Rise Time	tTLH	C <sub>L</sub> = 10pF			10	ns
Clock Fall Time	t <sub>THL</sub>	C <sub>L</sub> = 10pF			10	ns
SD CARD CLOCK TIMING (CCL	(_), HI-SPEEC	(Figure 5b)				
Clock Low Time	tw∟	$C_L = 40pF$	7			ns
Clock High Time	twH	$C_L = 40pF$	7			ns
Clock Rise Time	tTLH	$C_L = 40pF$			3	ns
Clock Fall Time	t <sub>THL</sub>	$C_L = 40pF$			3	ns
SD CARD COMMAND TIMING (C	CMD1, CCMD	2) (Figure 5b)	•			
Input Setup Time	tisu		5			ns
Input Hold Time	t <sub>IH</sub>		2			ns
Output Delay Time During Data Transfer Mode	todly				14	ns
Output Hold Time	toH		2.5			ns
I <sup>2</sup> C CHARACTERISTICS	•	•	•			
SCL Clock Frequency	fscl				400	kHz
SDA, SCL Capacitance	C <sub>IO_I2C</sub>			5		рF
SDA Output Fall Time	tOF_I2C				250	ns
Hold Time After Repeated START	thd,sta		0.6			μs

! \_\_\_\_\_\_\_/II/XI/M

### **ELECTRICAL CHARACTERISTICS (continued)**

 $(V_{CC} = +2.4 V \ to \ +3.6 V, \ V_{SD} = +2.4 V \ to \ +3.6 V, \ V_{IO} = +1.5 V \ to \ +3.6 V, \ V_{TM} = +2.91 V \ to \ +3.4 V, \ T_A = -40 ^{\circ}C \ to \ +85 ^{\circ}C, \ unless \ otherwise noted. Typical values are at V_{CC} = +3.3 V, V_{IO} = +2.5 V, V_{SD} = +2.5 V, V_{TM} = +3.3 V, T_A = +25 ^{\circ}C.) \ (Note \ 2)$ 

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Low Period	tLOW_I2C		1.3			μs
Clock High Period	thigh_i2C		0.6			μs
Setup Time for Repeated START	tsu,sta		0.6			μs
Hold Time for Data	thd,dat			0	0.9	μs
Setup Time for Data	tsu,dat		100			ns
SDA/SCL Input Fall Time	tF_I2C				300	ns
SDA/SCL Rise Time	tR_I2C				300	ns
Setup Time for STOP	tsu,sto		0.6			μs
Bus Free Time Between STOP and START	tBUF		1.3			μs

#### **USB HI-SPEED SOURCE ELECTRICAL CHARACTERISTICS**

 $(V_{CC} = +2.4V \text{ to } +3.6V, V_{SD} = +2.4V \text{ to } +3.6V, V_{IO} = +1.5V \text{ to } +3.6V, V_{TM} = +2.91V \text{ to } +3.4V, T_{A} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , unless otherwise noted. Typical values are at  $V_{CC} = +3.3V, V_{IO} = +2.5V, V_{SD} = +2.5V, V_{TM} = +3.3V, T_{A} = +25^{\circ}\text{C}$ .) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Hi-Speed Squelch Detection Threshold (Diff Signal Amplitude)	VHSSQ	(Note 6)	100		150	mV
Hi-Speed Differential Input Signaling Levels	VIL	Specified by Hi-Speed receive eye diagram				
Hi-Speed Data Signaling Common-Mode Voltage Range	SCM	(Note 6)	-50		+500	mV
Hi-Speed Idle Level	VHSOI		-10		+10	mV
Hi-Speed Data Signaling High	V <sub>HSOH</sub>		360		440	mV
Hi-Speed Data Signaling Low	VHSOL		-10		+10	mV
Chirp J Level (Differential Voltage)	VCHIRPJ		700		1100	mV
Chirp K Level (Differential Voltage)	VCHIRPK		-900		-500	mV
Termination Voltage (Hi-Speed)	VHSTERM		-10		+10	mV
AC CHARACTERISTICS						
Rise Time	tHSR	(Note 6)	500			ps
Fall Time	tHSF	(Note 6)	500			ps
Driver Waveform Requirements		Specified by Hi-Speed transmit eye diagram		Typical C		
Driver-Output Resistance	Z <sub>HSDRV</sub>		40.5		49.5	Ω
Source Jitter Total (Including Frequency Tolerance)		Specified by Hi-Speed transmit eye diagram	See the Typical Operating Characteristics section			

#### **USB FULL-SPEED SOURCE ELECTRICAL CHARACTERISTICS**

 $(V_{CC} = +2.4 \text{V to } +3.6 \text{V}, V_{SD} = +2.4 \text{V to } +3.6 \text{V}, V_{IO} = +1.5 \text{V to } +3.6 \text{V}, V_{TM} = +2.91 \text{V to } +3.4 \text{V}, T_{A} = -40 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C}, \text{ unless otherwise noted.}$  Typical values are at  $V_{CC} = +3.3 \text{V}, V_{IO} = +2.5 \text{V}, V_{SD} = +2.5 \text{V}, V_{TM} = +3.3 \text{V}, T_{A} = +25 ^{\circ}\text{C}.)$  (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS			•			
SE Receiver Input High	VIH		2.0			V
SE Receiver Input Low	VIL				0.8	V
Differential Common-Mode Voltage	V <sub>CM</sub>		0.8		2.0	V
Receiver Differential Input Sensitivity	V <sub>DI</sub>		0.2			V
Transmitter High	VoH	$R_L = 15k\Omega$ connected to GND	2.8		3.6	V
Transmitter Low	V <sub>OL</sub>	$R_L = 1.5 k\Omega$ connected to 3.3V	0		0.3	V
Transmitter Output Signal Crossover Voltage	VCRS	(Note 6)	1.3		2.0	V
Bus Pullup Resistor on Upstream Facing Port (Idle Bus)	R <sub>PUI</sub>		0.900	1.25	1.575	kΩ
Bus Pullup Resistor on Upstream Facing Port (Upstream Port Receiving)	R <sub>PUA</sub>		1.425	2.5	3.090	kΩ
Input Impedance	Z <sub>INP</sub>		300			kΩ
Termination Voltage for Upstream Facing Port Pullup (R <sub>PU</sub> )	VTERM			$V_{TM}$		V
AC CHARACTERISTICS			•			
Rise Time	t <sub>FR</sub>		4		20	ns
Fall Time	tFF		4		20	ns
Differential Rise and Fall Time Matching	tFRFM	(Note 6)	90		111.11	%
Full-Speed Data Rate	tfDRATHS		11.994		12.030	Mbps

- **Note 2:** All parameters are tested at  $T_A = +25^{\circ}C$ . Specifications over temperature are guaranteed by design.
- Note 3: On-resistance is measured by applying voltage and current on the SD card interface (CCLK1, CCMD1, CDAT1\_[3:0], CCLK2, CCMD2, CDAT2\_[3:0]).
- Note 4: Off-capacitance measured with SD switch open (CCLK1, HCLK1, CCMD1, HCMD1, CDAT1\_[3:0], HDAT1\_[3:0], CCLK2, HCLK2, CCMD2, HCMD2, CDAT2\_[3:0], HDAT2\_[3:0]).
- Note 5: On-capacitance measured on SD card side (CCLK1, CCMD1, CDAT1\_[3:0], CCLK2, CCMD2, CDAT2\_[3:0]).
- Note 6: Specifications guaranteed by design.

### **Typical Operating Characteristics**

 $(V_{CC} = +3.3V, V_{IO} = +2.5V, V_{SD} = +2.5V, V_{TM} = +3.3V, T_{A} = +25^{\circ}C, unless otherwise noted.)$ 

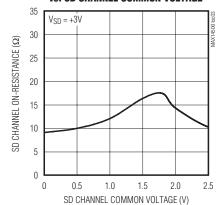
#### HI-SPEED EYE DIAGRAM FOR CARD READER MODE

MAX14500 too31

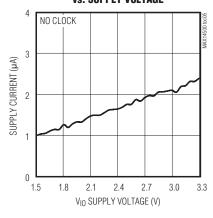
DIFFERENTIAL VOLTAGE

UNIT TIME INTERVAL

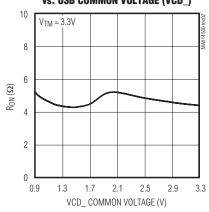
### SD CHANNEL ON-RESISTANCE vs. SD CHANNEL COMMON VOLTAGE



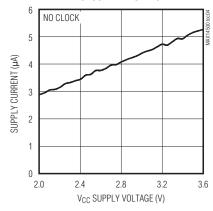
# PASS THRU V<sub>IO</sub> SUPPLY CURRENT vs. Supply Voltage



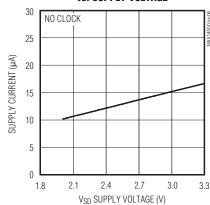
### USB ON-RESISTANCE vs. USB COMMON VOLTAGE (VCD\_)



# PASS THRU V<sub>CC</sub> SUPPLY CURRENT vs. SUPPLY VOLTAGE

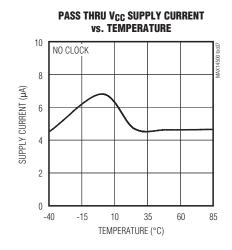


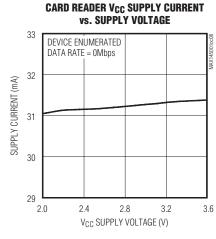
### PASS THRU V<sub>SD</sub> SUPPLY CURRENT vs. SUPPLY VOLTAGE

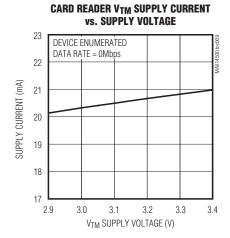


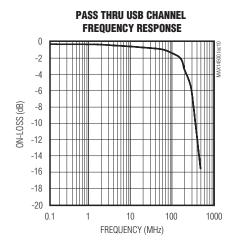
### Typical Operating Characteristics (continued)

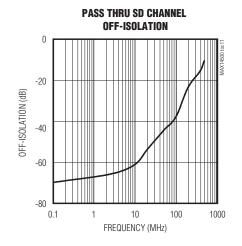
 $(V_{CC} = +3.3V, V_{IO} = +2.5V, V_{SD} = +2.5V, V_{TM} = +3.3V, T_{A} = +25^{\circ}C, unless otherwise noted.)$ 











### Pin Description

PIN			
TQFN	WLP	NAME	FUNCTION
INPUTS/OUT	PUTS	1	
1	C4	I2C_SEL	I <sup>2</sup> C Select Input. I <sup>2</sup> C_SEL must be connected to V <sub>IO</sub> or GND at power-up. Drive I <sup>2</sup> C_SEL low to disable I <sup>2</sup> C control and drive I <sup>2</sup> C_SEL high to enable I <sup>2</sup> C control.
2	A2	SCL	I <sup>2</sup> C Serial-Clock Input. SCL is $+3.6V$ tolerant and the high threshold is set by $V_{IO}$ . If the I <sup>2</sup> C interface is not used, connect SCL to GND.
3	B4	SDA	I2C Serial-Data I/O. SDA is $+3.6V$ tolerant and the high threshold is set by $V_{IO}$ . If the I2C interface is not used, connect SDA to GND.
4	А3	ADD	I <sup>2</sup> C Address Selection Input. Connect ADD to $V_{IO}$ or GND to select between two I <sup>2</sup> C slave addresses: (GND = 1110 000Xb and $V_{IO}$ = 1110 001Xb).
6	В6	BERR/INT	Card Reader Error/Interrupt Output. BERR/INT becomes BERR for simple control and INT for I2C control. BERR/INT goes low to indicate an error in Card Reader mode during simple control and asserts for enabled interrupts during I2C control.
7	A7	BUSY	Busy Output. BUSY asserts low to indicate device is in Card Reader mode.
8	C6	MODE	Card Reader/Pass Thru Mode Select Input. MODE is only active during simple control. Drive MODE low to enable Pass Thru mode and drive MODE high to enable Card Reader mode. For I <sup>2</sup> C control, MODE must be connected to GND.
9	B7	RST	Reset Input. Drive $\overline{RST}$ low to reset the internal registers to default values and put all outputs in high impedance. Connect $\overline{RST}$ to $V_{IO}$ for normal operation.
25	E6	FREF	Frequency Input. FREF is the clock input (12MHz/13MHz/19.2MHz/26MHz) for the internal logic and USB PHY. FREF can accept a square-wave or sine-wave clock. An internal clock squaring circuit can be enabled or disabled through I <sup>2</sup> C. In simple control, the internal clock squarer is enabled by default.
27	F5	RREF	Reference Resistor. Connect a Bias Resistor 6.19k $\Omega$ ±1% from RREF to GND.
USB INTERF	ACE	•	
22	G7	CD+	USB Analog Switch/Hi-Speed USB Transceiver. CD+ connects to D+ on the USB connector.
21	F7	CD-	USB Analog Switch/Hi-Speed USB Transceiver. CD- connects to D- on the USB connector.
20	G8	HD+	USB Analog Switch. HD+ connects to D+ on the host side.
19	F8	HD-	USB Analog Switch. HD- connects to D- on the host side.
28	E5	KVBUS	USB Bus Power-Supply Detection Input. Connect a resistor-divider between USB VBUS, KVBUS, and GND.
SD CARD IN	TERFACE		
13	C8	CDAT1_0	SD Card 1 Data Bus Analog Switch/Card Reader Interface. CDAT1_0 connects to DAT0 on the SD card.
12	B8	CDAT1_1	SD Data Card 1 Bus Analog Switch/Card Reader Interface. CDAT1_1 connects to DAT1 on the SD card.
11	C7	CDAT1_2	SD Data Card 1 Bus Analog Switch/Card Reader Interface. CDAT1_2 connects to DAT2 on the SD card.

### Pin Description (continued)

F	PIN		
TQFN	WLP	NAME	FUNCTION
10	A8	CDAT1_3	SD Card 1 Data Bus Analog Switch/Card Reader Interface. CDAT1_3 connects to DAT3 on the SD card.
34	E2	CCMD1	SD Card 1 Command Analog Switch/Card Reader Interface. CCMD1 connects to CMD on the SD card.
32	E3	CCLK1	SD Card 1 Clock Analog Switch/Card Reader Interface. CCLK1 connects to CLK on the SD card.
33	F1	CCRD_PRST	SD Card 1 Analog Switch for Card Present Detection. CCRD_PRST is the card detection line to the SD socket. When in Pass Thru mode, CCRD_PRST is connected to HCRD_PRST.
17	D7	HDAT1_0	SD Card 1 Data Bus Analog Switch. HDAT1_0 connects to DAT0 on the SD port of the host µP.
16	D8	HDAT1_1	SD Card 1 Data Bus Analog Switch. HDAT1_1 connects to DAT1 on the SD port of the host µP.
15	D6	HDAT1_2	SD Card 1 Data Bus Analog Switch. HDAT1_2 connects to DAT2 on the SD port of the host µP.
14	D5	HDAT1_3	SD Card 1 Data Bus Analog Switch. HDAT1_3 connects to DAT3 on the SD port of the host $\mu P$ .
31	G1	HCMD1	SD Card 1 Command Analog Switch. HCMD1 connects to CMD on the SD port of the host $\mu P$ .
29	G2	HCLK1	SD Card 1 Clock Analog Switch. HCLK1 connects to CLK on the SD port of the host µP.
30	F2	HCRD_PRST	SD Card 1 Analog Switch for Card Present Detection. HCRD_PRST is connected to CCRD_PRST in Pass Thru mode.
l	D2	CDAT2_0	SD Card 2 Data Bus Analog Switch/Card Reader Interface. CDAT2_0 connects to DAT0 on the SD card.
	D1	CDAT2_1	SD Card 2 Data Bus Analog Switch/Card Reader Interface. CDAT2_1 connects to DAT1 on the SD card.
_	B5	CDAT2_2	SD Card 2 Data Bus Analog Switch/Card Reader Interface. CDAT2_2 connects to DAT2 on the SD card.
_	A5	CDAT2_3	SD Card 2 Data Bus Analog Switch/Card Reader Interface. CDAT2_3 connects to DAT3 on the SD card.
_	F4	CCMD2	SD Card 2 Command Analog Switch/Card Reader Interface. CCMD2 connects to CMD on the SD card.
_	F3	CCLK2	SD Card 2 Clock Analog Switch/Card Reader Interface. CCLK2 connects to CLK on the SD card.
_	D3	HDAT2_0	SD Card 2 Data Bus Analog Switch. HDAT2_0 connects to DAT0 on the SD port of the host $\mu P$ .
_	E1	HDAT2_1	SD Card 2 Data Bus Analog Switch. HDAT2_1 connects to DAT1 on the SD port of the host µP.

### Pin Description (continued)

PIN NAME		FUNCTION		
WLP				
C5	HDAT2_2	SD Card 2 Data Bus Analog Switch. HDAT2_2 connects to DAT2 on the SD port of the host µP.		
A4	HDAT2_3	SD Card 2 Data Bus Analog Switch. HDAT2_3 connects to DAT3 on the SD port of the host µP.		
G4	HCMD2	SD Card 2 Command Analog Switch. HCMD2 connects to CMD on the SD port of the host $\mu P$ .		
G3	HCLK2	SD Card 2 Clock Analog Switch. HCLK2 connects to CLK on the SD port of the host µP.		
PLY				
A6	V <sub>IO</sub>	I/O Logic-Level Translator Voltage. Bypass V <sub>IO</sub> to GND with a 0.1µF ceramic capacitor. V <sub>IO</sub> powers the logic inputs/outputs and I <sup>2</sup> C block.		
F6	V <sub>TM</sub>	USB Analog Switch and Transceiver Power Supply. Bypass V <sub>TM</sub> to GND with a 0.1µF ceramic capacitor.		
B1, B2	CLDO	Bypass Capacitor for Internal +1.8V LDO. Connect a 1µF ceramic capacitor (X7R, X5R, or better) from CLDO to GND. CLDO must not be used to power external circuitry.		
B3, C3	Vcc	Digital Supply Voltage. Bypass $V_{CC}$ to GND with a 1 $\mu$ F ceramic capacitor (X7R, X5R, or better).		
A1	V <sub>SD</sub>	SD Card Voltage. Bypass $V_{SD}$ to GND with a 1 $\mu$ F ceramic capacitor (X7R, X5R, or better).		
C1, C2, E7, E8, G5, G6	GND	Ground		
ION				
D4, E4	N.C.	No Connection. Connect N.C. to GND.		
D				
_	EP	Exposed Pad. Connect EP to GND. Do not use EP as the sole GND connection.		
	MLP  C5  A4  G4  G3  LY  A6  F6  B1, B2  B3, C3  A1  C1, C2, E7, E8, G5, G6  ION  D4, E4	WLP         NAME           C5         HDAT2_2           A4         HDAT2_3           G4         HCMD2           G3         HCLK2           LY         VIO           F6         VTM           B1, B2         CLDO           B3, C3         VCC           A1         VSD           C1, C2, E7, E8, G5, G6         GND           ION         D4, E4         N.C.           D         N.C.		

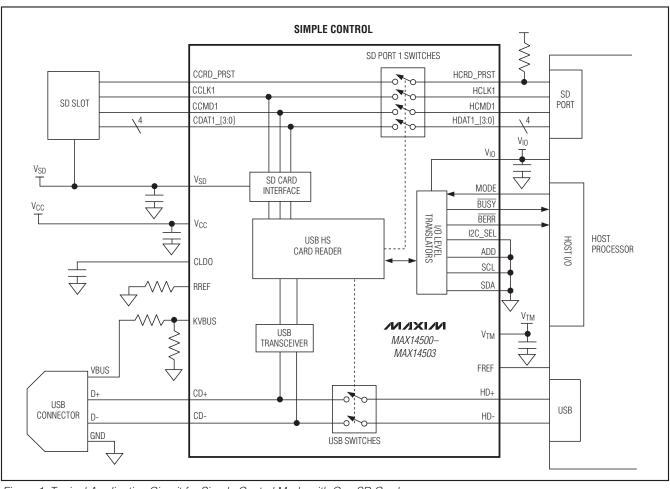


Figure 1. Typical Application Circuit for Simple Control Mode with One SD Card

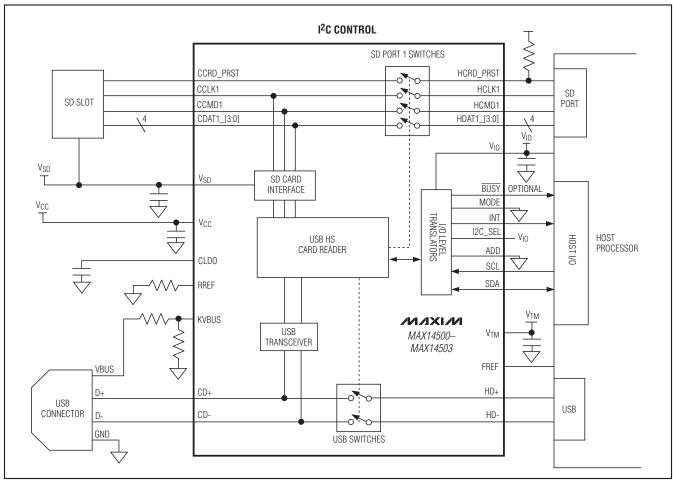


Figure 2. Typical Application Circuit for I<sup>2</sup>C Control Mode with One SD Card

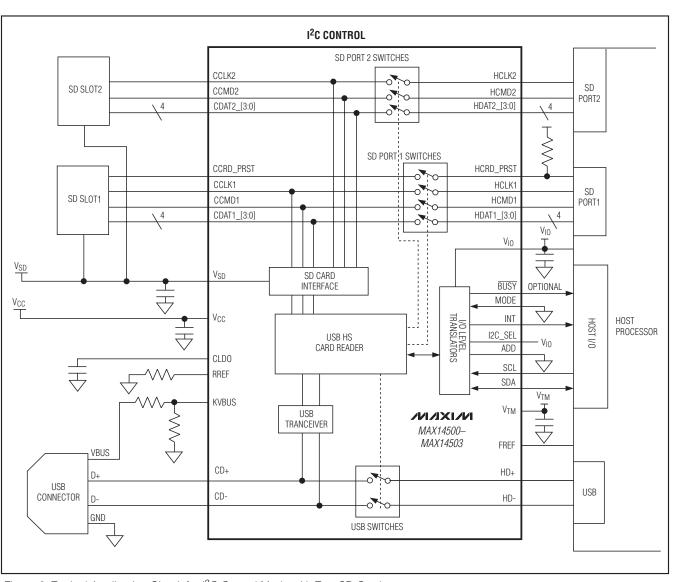


Figure 3. Typical Application Circuit for  $I^2C$  Control Mode with Two SD Cards

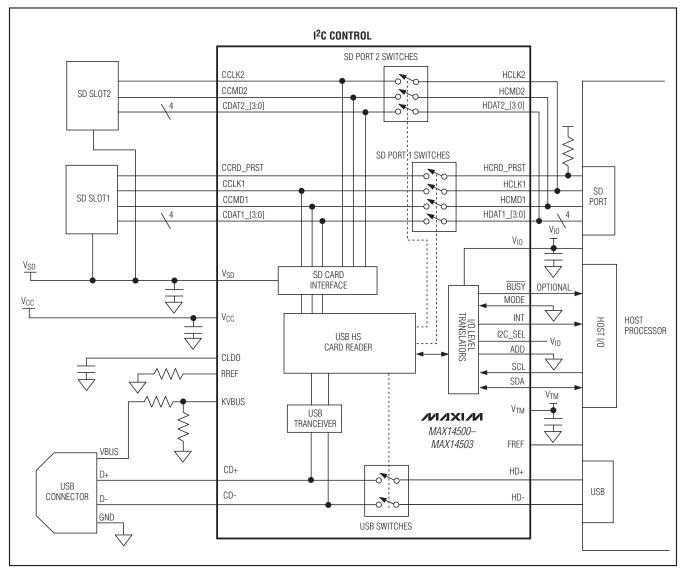


Figure 4. Typical Application Circuit for I<sup>2</sup>C Control Mode with One SD Port and Two SD Cards

# Timing Diagrams $t_{WL} \\$ $V_{\text{IH}}$ CLOCK $V_{\text{\scriptsize IL}}$ t<sub>TLH</sub> t<sub>THL</sub> t<sub>ISU</sub> $V_{\text{IH}} \\$ INPUT $V_{\mathsf{IL}}$ $V_{\text{OH}} \\$ OUTPUT todly (max) (min) SHADED AREAS ARE NOT VALID

Figure 5a. SD Card Default Timing Diagram

### Timing Diagrams (continued)

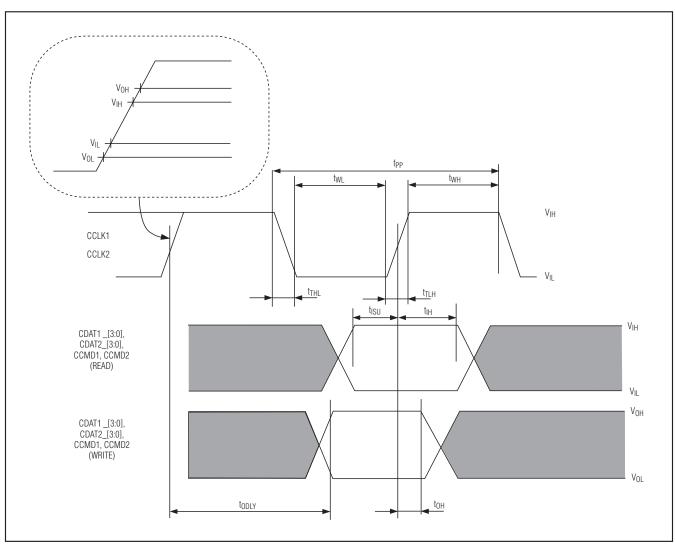


Figure 5b. SD Card Hi-Speed Timing Diagram

#### Timing Diagrams (continued)

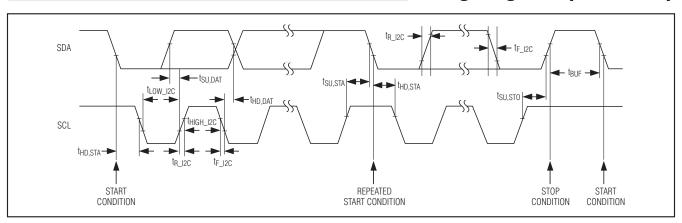


Figure 6. I<sup>2</sup>C Timing Diagram

### **Detailed Description**

The MAX14500-MAX14503 can be added to devices that have an SD card slot and a USB full-speed port (12Mbps) to provide a Hi-Speed USB path to an SD card bypassing the host microprocessor (µP), allowing for faster SD card transfers (Figures 1-4). Without the MAX14500-MAX14503, a host μP with a full-speed USB port moves data between an SD card and a host PC at 12Mbps when transferring data from an SD card through USB. The host µP has additional overhead because it has to accept data from the SD cards, process the data by putting it in USB format, and then transfer the data through the USB port. The MAX14500-MAX14503 create an alternate path from the SD card to USB, providing USB Hi-Speed capability. By bypassing the host µP using the MAX14500-MAX14503, SD card read and write operations are not limited by host uP overhead and USB full-speed data rates.

The MAX14500–MAX14503 operate in Pass Thru and Card Reader mode. In Pass Thru mode, the MAX14500–MAX14503 are transparent to the host  $\mu P.$  All read and write operations pass from the host  $\mu P$  SD port to the SD card without modification. All of the features of the original device are intact and there is no need to change firmware in the host  $\mu P.$  In Card Reader mode, the SD card is connected to the PC with the internal USB Hi-Speed card reader, bypassing the host  $\mu P.$ 

The MAX14500–MAX14503 can be controlled in two ways. The simple control method uses a single output from a  $\mu P$  or ASIC to select Pass Thru or Card Reader mode. Only one SD card can be used as a Hi-Speed USB card reader in simple control. I²C control allows more configuration options and provides status information along with error conditions and additional interrupts. Two SD cards can be connected and each set of SD port switches can be controlled independently (two SD port version under I²C control). The state of I2C\_SEL must not change after VIO is applied.

With I2C control, the I2C bus is used to read and write to internal registers for configuration, error checking, control, and status reporting. The control and configuration registers have various functions including wakeup, SD card selection, interrupt enable, and SD switch settings. The status registers give the status of errors, SD card detection, power supplies, and interrupts. Putting the MAX14500-MAX14503 to sleep puts the device into Pass Thru mode. The state of SD port switches for card 1 and card 2 can be changed while in Pass Thru. Some I<sup>2</sup>C commands are executed upon waking up or entering Card Reader mode. For register settings that involve Card Reader mode, (when in Sleep mode), programming the I<sup>2</sup>C registers changes the values, but the actions do not execute until the internal logic wakes up or Card Reader mode is entered. The register map indicates when register bit changes take effect.

Table 1. Power-Up Default Mini Register Map for Configuration Registers

REGISTER NAME	REGISTER ADDRESS (hex)	POWER-UP VALUE (hex)	POWER-UP DEFAULT SETTINGS
Control Register (CONTROL)	0x00	0x18	SD2SW = 1, SD switch 2 is closed SD1SW = 1, SD switch 1 is closed MODE[1:0] = 00, Card Reader mode is not active WAKEUP = 0, shutdown
Configuration Register 1 (CONFIG1)	0x01	0x00	SD2ONEBIT = 0, SD2 bus in 4-bit data mode SD1ONEBIT = 0, SD1 bus in 4-bit data mode INTPULSE = 0, INT stays asserted until status register is read INTACTHI = 0, INT asserts active low
Configuration Register 2 (CONFIG2)	0x02	0x00	CLKSOURCE = 00000, default clock input FORCEFS = 0, USB Hi-Speed
Configuration Register 3 (CONFIG3)	0x03	0x00	SD2MAXCLK = 0000, default clock (base SD clock) SD1MAXCLK = 0000, default clock (base SD clock)
Interrupt Enable Register 1 (IE1)	0x04	0x00	USBFS = 0, disable INT for full-speed status change USBSR = 0, disable INT for suspend/resume status change VTM = 0, disable INT for V <sub>TM</sub> status change VSD = 0, disable INT for V <sub>SD</sub> status change KVBUS = 0, disable INT for VBUS status change BSY = 0, disable INT for BUSY status change SDSTAT = 0, disable INT for SD card status change
Interrupt Enable Register 2 (IE2)	0x05	0x00	FWUPD = 0, disable INT for firmware update status change
USB Vendor ID High Byte (USBVIDH)	0x06	0x00	If VID = 0x0000, 0x06BA is used during USB enumeration, VID high byte = 0x06
USB Vendor ID Low Byte (USBVIDL)	0x07	0x00	If VID = 0x0000, 0x06BA is used during USB enumeration, VID low byte = 0xBA
USB Product ID High Byte (USBPIDH)	0x08	0x00	If PID = 0x0000, 0x38A4 is used during USB enumeration, PID high byte = 0x38
USB Product ID Low Byte (USBPIDL)	0x09	0x00	If PID = 0x0000, 0x38A4 is used during USB enumeration. PID low byte = 0xA4

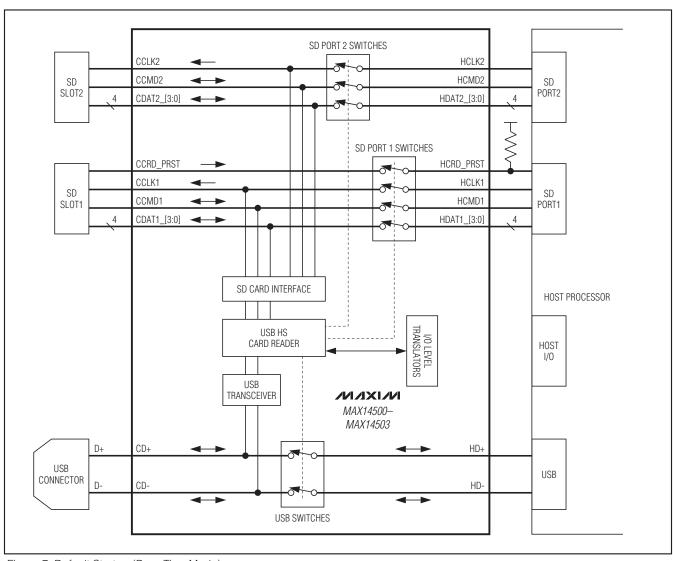


Figure 7. Default Startup (Pass Thru Mode)

#### **Default Power-Up (Pass Thru Mode)**

In the default Pass Thru mode, the MAX14500–MAX14503 are transparent and the existing host functions (access to SD cards and USB) are preserved (Figure 7). The host µP reads and writes data to the SD card from the SD port, and can communicate to a PC through its existing full-speed USB port. All of the features of the original chipset are intact. The MAX14500–MAX14503 sleep when in Pass Thru mode (WAKEUP = 0), when the MODE input is low, or when the MODE bits [2:1] in control register (0x00) are set to Card Reader mode, not active. In Sleep mode, the internal microcontroller is turned off and current consumption is mini-

mized. The settings for SD port switches for card 1 and card 2 are controlled by SD port switch bits [4:3] in the control register.

#### **Card Reader Mode**

In Card Reader mode, the PC communicates with the SD card through USB with an internal Hi-Speed SD card reader, bypassing the host  $\mu P.$  Figure 8 shows card reader mode with SD card 1 connected to the PC with the internal card reader. The 40-pin TQFN can connect to a single SD card in Card Reader mode. With the 56-bump WLP operating under  $I^2C$  control, either SD card can be selected for Card Reader mode.

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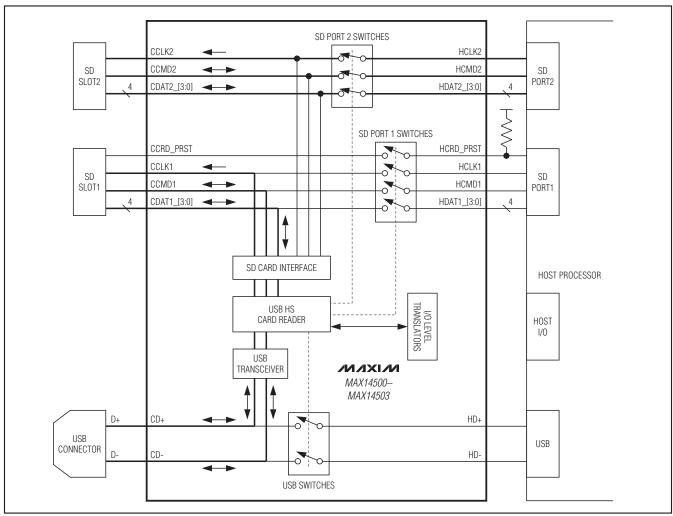


Figure 8. Card Reader Mode. The USB port is connected to SD card 1. In the 2 port version, a second SD card (SD slot 2) can be independently connected and disconnected to the host µP.

When the card reader is initiated in the control register, the internal USB switch disconnects from the host  $\mu P$  USB port and connects to the internal USB Hi-Speed SD card reader unit. When the MAX14500–MAX14503 disconnect from the host to implement a stand-alone high-speed card reader, it simulates a disconnect on the host USB and SD ports to maintain data coherence. The SD connections are restored to the host  $\mu P$  by closing the analog switch connecting CCRD\_PRST to HCRD\_PRST.

Certain registers execute actions when entering Card Reader mode. These actions are only valid for Card Reader mode. Writing to these registers in Sleep mode, or when awake, updates the registers, but the action is carried out when Card Reader mode is activated for one of the SD cards (see the *Register Map* section).

When Card Reader mode is initially entered, the internal microcontroller enumerates with the PC to establish a high-speed USB mass storage device. No actions by the host  $\mu P$  are required for enumeration other than entering Card Reader mode. Once the USB-SD card connection is established, PC to SD card data transfer begins and various interrupts monitor the status the of Card Reader mode if enabled. The BSY flag is represented externally by the  $\overline{BUSY}$  output and can be read serially through I²C. The  $\overline{BUSY}$  output is always active. If the host  $\mu P$  requests Sleep mode in the middle of the data transfer, the MAX14500–MAX14503 do not complete the transfer, exit Card Reader mode, reconnect USB switches, and

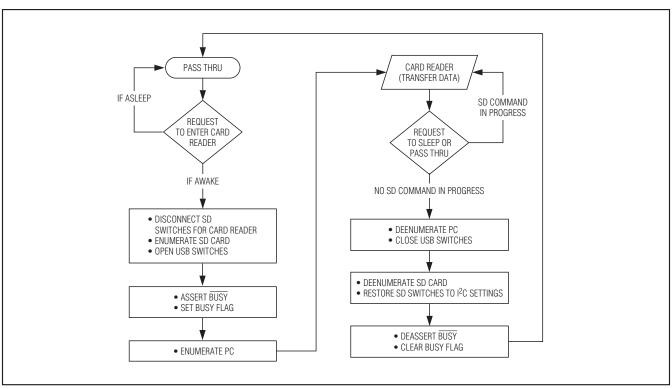


Figure 9. Card Reader Flow Chart

go to sleep. Because the  $\overline{BUSY}$  output (BSY bit in I²C) indicates Card Reader mode, the host  $\mu P$  may monitor this output after commanding a mode change to determine when the change takes place (Figure 9). If the host requests the other SD card to enter Card Reader mode, the busy flag deasserts and reasserts to let the host know that the change took place.

#### Simple Control (I2C\_SEL = Low)

The MAX14500–MAX14503 feature a very simple control scheme for entering Card Reader mode that requires a single logic (GPIO) from the host  $\mu P.$  The simple control may only be used with the single SD port versions. When I2C\_SEL is connected low at startup, the MODE input controls whether the device is in Pass Thru or Card Reader mode. Driving MODE low enables Pass Thru mode (Figure 10), and the host  $\mu P$  has a direct connection to the SD card and USB connector through internal analog switches. Driving MODE high enables Card Reader mode between SD card 1 and the PC through the USB connector (Figure 11).  $\overline{\rm BERR/INT}$  functions as the bridge error output  $\overline{\rm BERR}$  that asserts for card reader errors. Interrupts are not enabled, the clock source is set to the default as

defined by the part number, and the  $\overline{\text{BERR}}$  and  $\overline{\text{BUSY}}$  outputs are active. Upon MODE transitioning high, SD card 1 connects to the USB connector in Card Reader mode and  $\overline{\text{BUSY}}$  asserts low. The  $\overline{\text{BUSY}}$  output indicates that the device is in Card Reader mode.  $\overline{\text{BUSY}}$  may be important to the host  $\mu\text{P}$ , as the time to complete enumeration/de-enumeration may take a long time (> 100ms).

#### I<sup>2</sup>C Control (I2C\_SEL = High)

The MAX14500–MAX14503 feature I<sup>2</sup>C control that allows access to internal registers for complete control over configuration, SD port analog switches, interrupts, clock configuration, advanced power-on states, and error status. I<sup>2</sup>C control uses I<sup>2</sup>C to serially program the MAX14500–MAX14503 to be in Card Reader or Pass Thru mode, and allows either SD card to be connected in Card Reader mode. While a SD card is connected in Card Reader mode, the other SD port analog switches can be independently controlled serially through I<sup>2</sup>C. Using the I<sup>2</sup>C bus to put the device to sleep minimizes the supply current while maintaining control over the SD port switches.

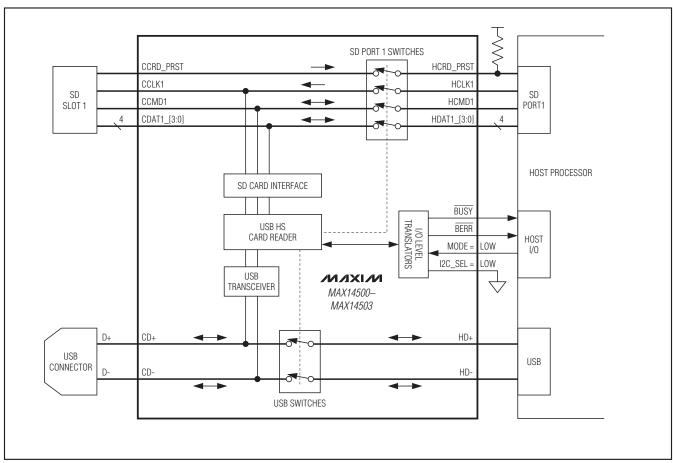


Figure 10. I2C\_SEL Connected Low to Enable Simple Control and MODE = 0 to Enable Pass Thru

#### **Control Register (0x00)**

The control register controls the settings of SD port analog switches, Card Reader mode, and sleep (Table 2.) The state of the SD port analog switches can be changed when the device is in Sleep mode or in Card Reader mode, and actions are executed immediately. If SD card 1 is connected to the PC through USB in Card Reader mode, the state of the SD port 1 switches are ignored, but the SD port 2 switches can still be controlled through the Control register. Likewise, if SD card 2 is connected to the USB connector in Card Reader mode, the state of the SD port 2 switches are ignored, but the SD port 1 switches can still be controlled through the Control register. Changing the card reader bits in Sleep mode does not cause the device to enter Card Reader mode. Under this condition, the MAX14500-MAX14503 enter Card Reader mode upon waking up.

#### **Configuration Registers**

The MAX14500–MAX14503 have three configuration registers (CONFIG1 = 0x01, CONFIG2 = 0x02, CONFIG3 = 0x03). The configuration registers control the SD bus bit data mode, interrupt polarity, interrupt clearance, clock configuration, SD clock, and USB speed for Card Reader mode. The default settings are shown in the *Register Map* section.

#### Interrupts (INT)

All interrupts are masked in the default reset state. There are two interrupt enable registers (IE1 = 0x04, IE2 = 0x05) and two interrupt request registers (IRQ1 = 0x10, IRQ2 = 0x11). The BERR/INT output functions as the bridge error output BERR in simple control and functions as an interrupt INT in I<sup>2</sup>C control. The polarity of INT and how INT is asserted can be programmed in CONFIG1. The INT output asserts for enabled interrupts and errors in Card Reader mode. The polarity of INT can be active-high or active-low, and INT can be pro-

Table 2. Control Register (0x00)

BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT
[7:5]	RESERVED	000	Set these bits to 0.	000
4	SD PORT 2 ANALOG SWITCHES SD Port 2 is a set of six analog switches connecting the SD port to the SD card. This set contains: clock (CCLK2), command (CCMD2), and	0	Analog switches are open, disconnecting the SD port from the SD card.	1
4	four data lines (CDAT2_[3:0]). The card-present line is not available for this port. This setting is ignored when Card Reader mode is enabled for this port.	1	Analog switches are closed, connecting the SD port to the SD card.	'
3	SD PORT 1 ANALOG SWITCHES  SD Port 1 is a set of seven analog switches connecting the SD port to the SD card. This set contains: card-present (CCRD_PRST), clock	0	Analog switches are open, disconnecting the SD port from the SD card.	1
3	(CCLK1), command (CCMD1), and four data lines (CDAT1_[3:0]). The difference between Port 1 and Port 2 is the card-present line. This setting is ignored when Card Reader mode is enabled for this port.	1	Analog switches are closed, connecting the SD port to the SD card.	'
	CARD READER MODE	00, 11	Card Reader mode not active.	
[2:1]	Changing these bits in Sleep mode does not execute the action until the host μP wakes up the MAX14500–MAX14503.	01	Card Reader mode active: Connects to SD card 1.	00
	the hoot pir warred up the him will hood with the hoot.	10	Card Reader mode active: Connects to SD card 2.	
0	WAKEUP In Sleep mode, the MAX14500–MAX14503 are in Pass Thru mode. SD port switches are controlled by their respective bits. Entering Sleep mode reduces the supply current by turning off the internal logic.	0	Request internal logic to shut down.	0
	Request to shut down may be delayed due to USB and de- enumeration.	1	Wake up internal logic.	

grammed to stay asserted until the status register is read, or stay asserted for 10ms. If INT is programmed to stay asserted, a read to the status register is required to clear INT. INT can be programmed to be active-high or active-low when I2C\_SEL is high (I²C control). INT is high impedance in Sleep mode (WAKEUP = 0), regardless of the INT polarity programmed in the I²C registers. Use a pullup or pulldown resistor for the desired inactive INT polarity state during Sleep mode.

#### Interrupt Masking

All interrupts are masked at power-up. While masked interrupts do not assert the INT output, they do register as changes in the interrupt request registers (IRQ1 and IRQ2). The status register (STATUS1 = 0x12) indicates the current state of the interrupt bits. If interrupts are masked, polling IRQ1 and IRQ2 indicate the fields with changes, and STATUS1 gives the current state. Reading the IRQ registers resets the interrupt request bits. If polling is used to read the device status, it is required to read both the status register and the interrupt request registers to check for state changes.

#### USB Interrupts

When enabled, the INT output asserts an interrupt for changes in the USB connection and if the operating system suspends the USB connection. VBUS is detected at the KVBUS input and changes in VBUS voltage can assert an interrupt when enabled.

#### Power-Supply Interrupts

The MAX14500–MAX14503 feature many advanced power-saving modes. V<sub>CC</sub>, V<sub>SD</sub>, and V<sub>TM</sub> do not need to be applied for I<sup>2</sup>C communication. Changes in V<sub>SD</sub> and V<sub>TM</sub> can assert an interrupt when enabled to indicate different power-saving modes (see the *Power-Supply Modes* section).

#### **Busy Interrupt**

When enabled, changes in the BSY bit can assert an interrupt (see the *Busy Indication (BSY)* section).

#### SD Status Interrupt

When enabled, the SDSTAT bit asserts an interrupt for card detection and removal upon entering Card Reader mode for the SD card socket configured as the card reader. The SDSTAT bit is not active during Pass Thru mode and does not change states in the IRQ registers upon card insertion and removal during Pass Thru mode.

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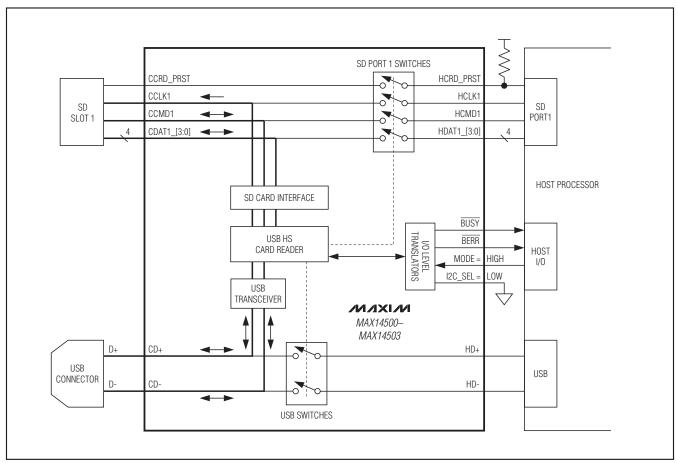


Figure 11. I2C\_SEL is connected low to enable simple control and MODE = 1 to enable Card Reader mode for SD card 1.

#### **Error Checking**

In simple control, the  $\overline{BERR}/INT$  output functions as  $\overline{BERR}$  and indicates if an error occurs during Card Reader mode. If  $\overline{BERR}$  asserts low to indicate an error, the MAX14500–MAX14503 stay in Card Reader mode. If the error clears, data transfer begins.  $\overline{BERR}$  asserts if KVBUS,  $V_{TM}$ , or  $V_{SD}$  are not present. It is recommended that MODE be pulled low when  $\overline{BERR}$  indicates an error to return the MAX14500–MAX14503 to Pass Thru mode for the host  $\mu P$  to clear the error.

In I<sup>2</sup>C control, BERR/INT functions as an interrupt output (INT) and asserts for errors encountered in Card Reader mode when interrupts are not masked. To find the source of the interrupt, read the interrupt request registers and status register.

#### Busy Indication (BSY)

The BUSY output is used in simple control and I2C control to indicate when Card Reader mode is active. In simple control, transitioning MODE high to low requests the internal microcontroller to enable Pass Thru mode. BUSY asserts low while in Card Reader mode and deasserts high in Pass Thru mode.

The BSY bit in <u>STATUS1</u> (0x12) behaves similarly with I<sup>2</sup>C control. The <u>BUSY</u> output is represented by the BSY bit. Requests to put the device to sleep or bypass (Pass Thru mode) while in Card Reader mode can be verified by checking the state of the <u>BUSY</u> signal or BSY bit. The <u>BUSY</u> output indicates the status of the <u>BUSY</u> flag in STATUS1. The BSY bit is 1 when the <u>BUSY</u> output asserts low. When enabled, changes in the busy flag cause an interrupt. In I<sup>2</sup>C control, either the BSY bit or the <u>BUSY</u> output give the status of the busy state.

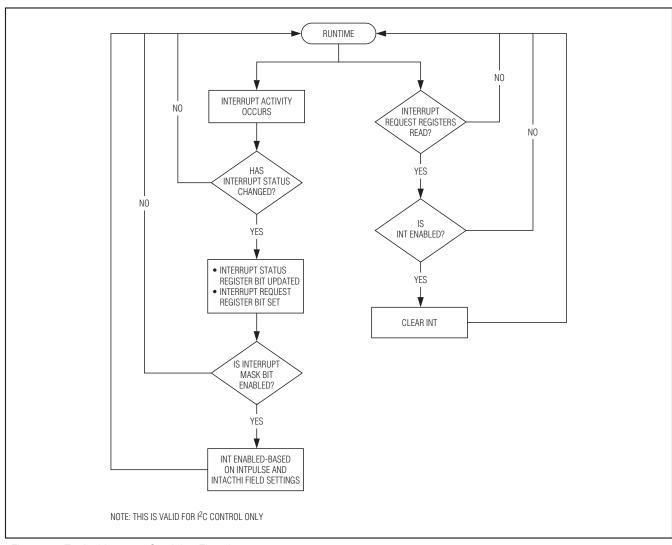


Figure 12. Typical Interrupt Servicing Flowchart

### Reset (RST)

Drive RST low to reset all the registers to the default value and minimize the supply current.

#### Sleep

The MAX14500–MAX14503 can be put to sleep by programming the WAKEUP bit to 0 in the control register with I<sup>2</sup>C control, or by driving the MODE input low in simple control. This turns off the internal microcontroller to minimize current. Reads and writes to the I<sup>2</sup>C are still functional, and registers can be updated with new values. Most register actions do not take effect until the internal microcontroller wakes up or when Card Reader mode is enabled. The SD port analog switches can

change states while the internal microcontroller is in Sleep mode. The *Register Map* section shows which registers are enabled in Sleep mode, at power-up, and upon entering Card Reader mode.

#### **Clock Configuration**

The MAX14500–MAX14503 come preprogrammed to accept a 12MHz, 13MHz, 19.2MHz, or 26MHz default clock input with the clock squarer enabled for low-amplitude TCXO signals (see the *Ordering Information/Selector Guide*). This clock is used for the USB and SD subsystems and is not required for operation of the I<sup>2</sup>C interface. This allows the clock frequency to be changed in the system. The PLL subsystem con-

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sists of two blocks: a clock squarer input (enabled by default), which accepts low-signal amplitude TCXO signals (down to 200mV), and a PLL with fixed dividers. The PLL sub system can be configured using the I<sup>2</sup>C interface. The complete list of PLL subsystem combinations are listed in Table 3.

#### **Table 3. Clock Source Bit Values**

CLKSOURCE	SOURCE (MHz)	NOTES
00000b	See Ordering Information/ Selector Guide	Default low-amplitude clock
00001b	19.2	Rail-to-rail square wave
00010b	19.2	Low-amplitude sine wave
00101b	13.0	Rail-to-rail square wave
00110b	13.0	Low-amplitude sine wave
01001b	12.0	Rail-to-rail square wave
01010b	12.0	Low-amplitude sine wave
01101b	26.0	Rail-to-rail square wave
01110b	26.0	Low-amplitude sine wave

### I<sup>2</sup>C Serial Interface

#### Serial Addressing

The MAX14500–MAX14503 operate as I<sup>2</sup>C slave devices that send and receive data through an I<sup>2</sup>C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master initiates all data transfers to and from the MAX14500-MAX14503, and generates the SCL clock that synchronizes the data transfer. The SDA line operates as both an input and an open-drain output requiring a pullup resistor on SDA. The SCL line operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output. Each transmission consists of a START (S) condition by a master, followed by the MAX14500-MAX14503's 7-bit slave address, plus a R/W bit, a register address byte, one or more data bytes, and finally a STOP (P) condition.

#### START and STOP Conditions

Both SCL and SDA remain high when the interface is idle. A master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high (Figure 13). When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

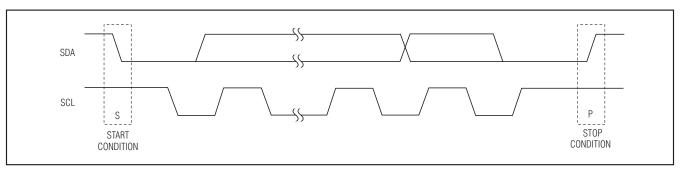


Figure 13. START and STOP Conditions

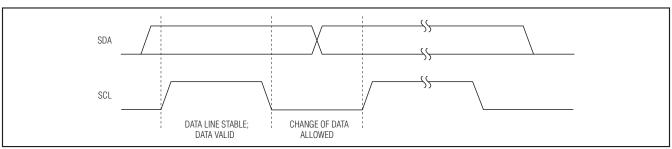


Figure 14. Bit Transfer

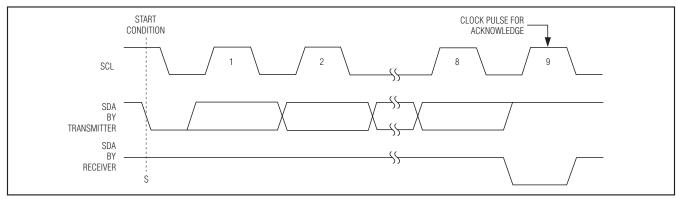


Figure 15. Acknowledge

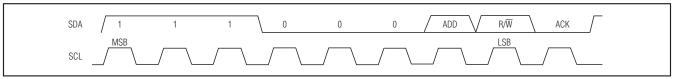


Figure 16. Slave Address

#### Bit Transfer

One data bit is transferred during each clock pulse (Figure 14). The data on SDA must remain stable while SCL is high.

#### Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 15), which the recipient uses to handshake receipt of each byte of data. Each byte transferred effectively requires nine bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse. The SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX14500–MAX14503, the MAX14500–MAX14503 generate the acknowledge bit because the MAX14500–MAX14503 are transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

#### Slave Addresses

The MAX14500–MAX14503 have a 7-bit long slave address. The bit following the 7-bit slave address is the R/W bit, which is low for a write command and high for a read command. The address bit ADD is externally driven high or low by the ADD input to select between two slave addresses to avoid conflict with other  $I^2C$  addresses (Figure 16). Table 4 shows the binary values for reads and writes.

**Table 4. Slave Addresses** 

ADD	FUNCTION	DEVICE ADDRESS							
High	Read	1	1	1	0	0	0	1	1
High	Write	1	1	1	0	0	0	1	0
GND	Read	1	1	1	0	0	0	0	1
GND	Write	1	1	1	0	0	0	0	0

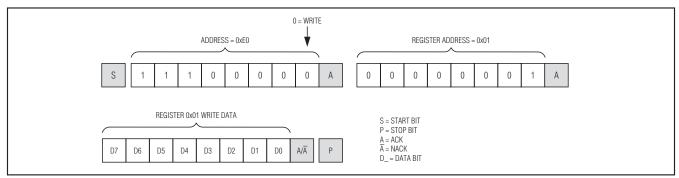


Figure 17. Format for I<sup>2</sup>C Write. In this example the register 0x01 is written.

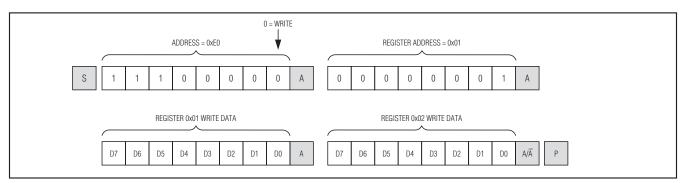


Figure 18. Format for Writing to Multiple Registers. In this example, registers 0x01 and 0x02 are written in sequence.

#### Format for Writing

A write to the MAX14500–MAX14503 comprises the transmission of the slave address with the R/W bit set to zero, followed by at least 1 byte of information. The first byte of information is the register address or command byte. The register address determines which register of the MAX14500–MAX14503 is to be written by the next byte if received. If a STOP condition is detected after the register address is received, then the MAX14500–MAX14503 take no further action beyond storing the register address (Figure 17).

Any bytes received after the register address are data bytes. The first data byte goes into the register selected by the register address and subsequent data bytes go into subsequent registers (Figure 18). If multiple data bytes are transmitted before a STOP condition, these bytes are stored in subsequent registers because the register address autoincrements.

#### Format for Reading

The MAX14500–MAX14503 are read using the internally stored register address as an address pointer, the same way the stored register address is used as an address pointer for a write. The pointer autoincrements

after each data byte is read using the same rules used for a write. Thus, a read is initiated by first configuring the register address by performing a write (Figure 19). The master can now read consecutive bytes from the MAX14500–MAX14503, with the first data byte being read from the register addressed pointed by the previously written register address (Figure 20). Once the master sends a NACK, the MAX14500–MAX14503 stop sending valid data.

### **Applications Information**

#### **SD Ports**

The MAX14500-MAX14503 support one or two SD cards or SD interface NAND flash memory.

#### SD Ports Configuration

There are three operational configurations:

- 40-pin TQFN version, containing one host port and one SD card (Figures 1, 2)
- 56-bump WLP version, containing two SD host ports and two SD cards. There are two SD hosts and two SD memory cards. Use this mode if the host has two SD ports (Figure 3).

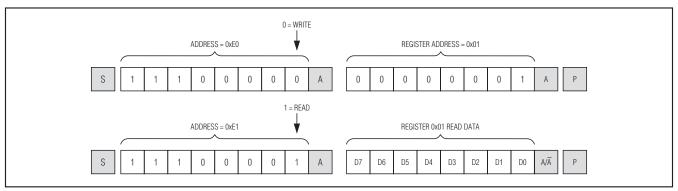


Figure 19. Format for Reading

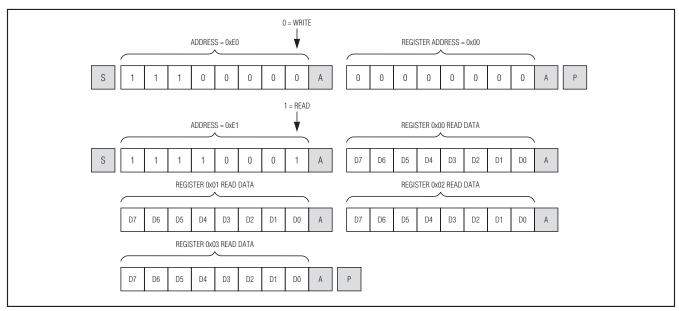


Figure 20. Format for Reading Multiple Registers

• 56-bump WLP version, containing one port and two SD cards. The host SD ports 1 and 2 are connected together at the host. This configuration allows two SD cards connected to one host, but only one SD card is connected to the host at a time. The host uses the MAX14500–MAX14503's internal SD port switches to multiplex between the cards. This configuration can also be used to limit the bus capacitive loading of having two cards connected at the same time to the bus (Figure 4).

#### SD Card Clock Frequency

The SD card clock frequency is the lower of the maximum the card can support as read from the SD card and base SD clock (base SD clock is determined from values shown in Table 5). The MAX14500-MAX14503

internally read the max frequency directly from the SD card. In I<sup>2</sup>C control, the maximum clock frequency is programmable to values lower than the maximum allowed by the SD card, helping with issues such as excessive bus capacitance causing data errors.

Table 5. Maximum SD Card Clock Frequency

INPUT FREQUENCY (MHz)	BASE SD CLOCK (MHz)
12	48
13	52
19.2	48
26	52

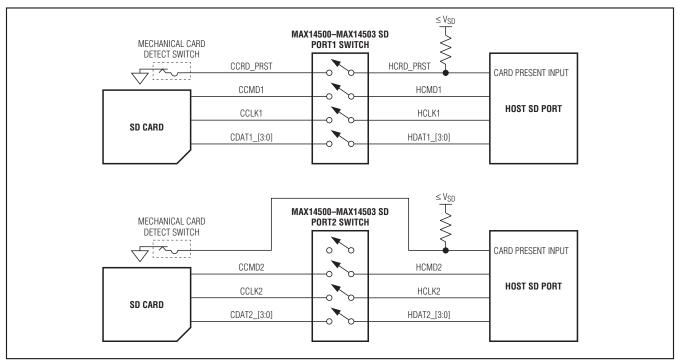


Figure 21. Host Card Detection Schemes

#### SD Port Switches

The SD port analog switches change states immediately whether the MAX14500–MAX14503 are in Sleep mode (WAKEUP = 0) or awake. If the internal USB Hi-Speed SD card reader is in operation, the SD card switches for the selected path are opened automatically. Any writes to the SD port switch bits for that path are ignored. The SD port analog switches for the path not being used for the card reader are controllable by the host  $\mu$ P, and any writes to these bits affect state changes immediately.

#### **Card Detection**

The MAX14500–MAX14503 provide an analog switch to pass the card present signal on SD card slot 1. This allows the host  $\mu P$  to continue using the SD slot card present switch (see Figure 21). The internal analog switch can be bypassed if an alternate algorithm is used to detect card data change. The second SD card path does not provide this analog switch so if this path is used for another SD card socket, an alternate card-detection mechanism for the host  $\mu P$  may be needed. If the second SD card path is used for an SD interface NAND chip, no card detection is required.

The MAX14500-MAX14503 do not use the SD card slot switch to detect insertion and removals. Instead, a pro-

tocol-based detection mechanism is used that polls for the presence or absence of an SD card. This allows both path 1 and path 2 to support an SD card slot with removable SD cards without a connection between the MAX14500–MAX14503 and the SD socket card present switch. The pullup voltage for the card slot detection may be any voltage equal to or less than VSD.

#### **Enumeration**

The MAX14500–MAX14503 enumerate to the USB mass storage class and appear as a USB mass storage device on most operating systems.

#### USB Hi-Speed vs. Full-Speed

The MAX14500–MAX14503 support USB Hi-Speed and full-speed operation. The MAX14500–MAX14503 operate at 480Mbps when plugged into a Hi-Speed USB host, and at 12Mbps when plugged into a full-speed host.

#### **USB VID/PID**

Using I<sup>2</sup>C, the MAX14500–MAX14503 have dedicated I<sup>2</sup>C registers for vendor identification (VID) and product identification (PID). The programmed 16-bit default values are shown in the *Register Map* section. The factory default values can be replaced with your company's VID and PID.

#### **Power-Supply Modes**

The MAX14500–MAX14503 have four power-supply inputs (Table 6). Bypass VCC, VIO, VSD, and VTM with high-frequency, surface-mount ceramic capacitors as close as possible to the supply pins.

#### Table 6. Power-Supply Inputs

SUPPLY	FUNCTION	RANGE (V)
V <sub>TM</sub>	USB transceiver and USB switch power	+2.91 to +3.4
Vcc	Digital core 1.8V LDO	+2.1 to +3.6
V <sub>SD</sub>	SD card level translator and SD switches	+2.0 to +3.6
V <sub>IO</sub>	Host microprocessor level translator	+1.5 to +3.6

#### Power-supply inputs:

- VTM USB Transceiver Power. This supply powers the USB analog switches, PLL subsystem, and the USB 2.0 transceiver. This regulator can be internal to a power-management IC, or it can be discrete and is recommended to be powered from USB VBUS. This supply must be present when the MAX14500– MAX14503 are used in Card Reader mode to pass USB signals in Pass Thru mode.
- VCC Digital Logic Power. This supply powers the digital logic/internal microcontroller/flash memory. There is an internal +1.8V LDO (CLDO) with shutdown controlled by the state of the MODE input and internal logic.
- V<sub>SD</sub> SD Card Power. This supply powers the SD card level translator and SD card switches. V<sub>SD</sub> needs to be present to pass SD signals in Pass Thru mode.
- 4) V<sub>IO</sub> Host Interface Power. This supply powers the digital I/O and I<sup>2</sup>C interface.

#### Power modes:

- 1) Idle. Only V<sub>IO</sub> is required to be present. I<sup>2</sup>C registers can be updated, but no operation is possible.
- 2) Pass Thru Mode. V<sub>IO</sub> needs to be present so the voltage level at MODE can be detected. To allow USB pass thru, the V<sub>TM</sub> supply needs to be present. To allow SD pass thru, V<sub>SD</sub> supply needs to be present. Each supply is independent from the others and no power-supply sequencing is required.
- 3) Card Reader Mode. All supplies are needed. When the card reader is actively transferring data, this mode draws the most current, mainly from VCC and VTM.

#### **Layout Considerations**

The MAX14500–MAX14503 support Hi-Speed USB and requires careful PCB layout. Use controlled-impedance matched traces of equal lengths to the USB connector with no discontinuities and a minimum number of feedthroughs. All SD traces (CLK, CMD, DAT\_) should be of equal lengths and as short as possible.

#### **Choosing Pullup Resistors**

I²C requires pullup resistors to provide a logic-high level to data and clock lines. There are tradeoffs between power dissipation and speed, and a compromise must be made in choosing pullup resistor values. Every device connected to the bus introduces some capacitance, even when the device is not in operation. I²C specifies 300ns rise time to go from low to high (30% to 70%) for fast mode, which is defined for data rates up to 400kbps. To meet the rise time requirement, choose pullup resistors so the rise time (tR) is less than 300ns where tR  $\approx 0.85 \times RPULLUP \times CBUS$ . If the transition time becomes too slow, the setup and hold times may not be met and waveforms may not be recognized.

### Register Map

FIELD NAME	READ WRITE	BITS	RESET	DESCRIPTION	VALID WHEN
CONTROL: Control Reg	ister (0x00)		•		
RFU	R/W	[7:5]	000	Reserved for future use	_
SD2SW	R/W	4	1	Setting of SD port 2 switches: 0 = open 1 = closed	Powered
SD1SW	R/W	3	1	Setting of SD port 1 switches: 0 = open 1 = closed	Powered
MODE	R/W	[2:1]	00	Activates PC USB Hi-Speed SD card reader: 00 = not active 01 = card reader active for SD port 1 10 = card reader active for SD port 2 11 = not active	WAKEUP = 1
WAKEUP	R/W	0	0	Wakes the internal μC: 0 = requests μC to shut down 1 = wakes μC	Powered
CONFIG1: Configuration	n Register 1	(0x01)	•		
SD2ONEBIT	R/W	7	0	Force the SD port 2 bus to 1 bit mode: 0 = SD bus 4-bit data mode 1 = SD bus 1-bit data mode	Enter Card Reader mode
SD10NEBIT	R/W	6	0	Force the SD port 1 bus to 1 bit mode: 0 = SD bus 4-bit data mode 1 = SD bus 1-bit data mode	Enter Card Reader mode
INTPULSE	R/W	5	0	INT assertion method: 0 = INT stays asserted until STATUS register is read 1 = INT asserts for 10ms pulse	WAKEUP = 1
INTACTHI	R/W	4	0	INT pin active level: 0 = active-low 1 = active-high	WAKEUP = 1
RFU	R/W	[3:0]	0000	Reserved for future use	
CONFIG2: Configuration	n Register 2	2 (0x02)			
RFU	R/W	7	0	Reserved for future use	_
CLKSOURCE	R/W	[6:2]	00000	Sets the configuration for the clock input:  00000 = default  00001 = 19.2MHz rail-to-rail square wave  00010 = 19.2MHz low-amplitude AC-coupled sine wave  00101 = 13MHz rail-to-rail square wave  00110 = 13MHz low-amplitude AC-coupled sine wave  01001 = 12MHz rail-to-rail square wave  01010 = 12MHz low-amplitude AC-coupled sine wave  01101 = 26MHz rail-to-rail square wave  01110 = 26MHz low-amplitude AC-coupled sine wave  All other values = default	Enter Card Reader mode

### Register Map (continued)

FIELD NAME	READ WRITE	BITS	RESET	DESCRIPTION	VALID WHEN
FORCEFS	R/W	1	0	Sets the maximum USB speed: 0 = Hi-Speed 1 = full speed	Enter Card Reader mode
RFU	R/W	0	0	Reserved for future use	_
CONFIG3: Configuration	n Register 3	3 (0x03)			
SD2MAXCLK	R/W	[7:4]	0000	Limits the max clock for SD card 2. The SD clock will be the minimum of either this register or the SD card max speed register.  0111 = base SD clock/64  0110 = base SD clock/32  0101 = base SD clock/16  0100 = base SD clock/8  0011 = base SD clock/4  0010 = base SD clock/2  0001 = base SD clock 0000 = default (base SD clock)	Enter Card Reader mode
SD1MAXCLK	R/W	[3:0]	0000	Limits the max clock for SD card 1. The SD clock will be the minimum of either this register or the SD card max speed register.  0111 = base SD clock/64  0110 = base SD clock/32  0101 = base SD clock/16  0100 = base SD clock/8  0011 = base SD clock/4  0010 = base SD clock/2  0001 = base SD clock 0000 = default (base SD clock)	Enter Card Reader mode
IE1: Interrupt Enable Re	egister 1 (0x	04)			
RFU	R/W	7	0	Reserved for future use	_
USBFS	R/W	6	0	Full-speed status change: 0 = disable contribution to INT 1 = enable contribution to INT	Powered
USBSR	R/W	5	0	USB suspend-resume status change: 0 = disable contribution to INT 1 = enable contribution to INT	Powered
VTM	R/W	4	0	V <sub>TM</sub> voltage-detector change: 0 = disable contribution to INT 1 = enable contribution to INT	Powered
VSD	R/W	3	0	V <sub>SD</sub> voltage-detector change: 0 = disable contribution to INT 1 = enable contribution to INT	Powered
KVBUS	R/W	2	0	VBUS voltage-detector change: 0 = disable contribution to INT 1 = enable contribution to INT	Powered

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### \_Register Map (continued)

FIELD NAME	READ WRITE	BITS	RESET	DESCRIPTION	VALID WHEN		
BUSY	R/W	1	0	BUSY state change: 0 = disable contribution to INT 1 = enable contribution to INT	Powered		
SDSTAT	R/W	0	0	SD card status change: 0 = disable contribution to INT 1 = enable contribution to INT Note: Reflects currently selected card in Card Reader mode	Powered		
IE2: Interrupt Enable Register 2 (0x05)							
FWUPD	R/W	7	0	Firmware update status change: 0 = disable contribution to INT 1 = enable contribution to INT	Powered		
RFU	R/W	[6:0]	0000000	Reserved for future use	_		
USBVIDH: USB Vendor I	D High Byt	te (0x06)					
VID 1	R/W	[7:0]	0x00	Bits 15–8 of USB vendor ID reported during card reader enumeration. If this register is written, the written value is used for USB enumeration, otherwise a default VID of 0x06BA (Maxim Integrated Products) is used.	Enter Card Reader mode		
USBVIDL: USB Vendor I	D Low Byt	e (0x07)	· I				
VID 2	R/W	[7:0]	0x00	Bits 7–0 of USB vendor ID reported during card reader enumeration. If this register is written, the written value is used for USB enumeration, otherwise a default VID of 0x06BA (Maxim Integrated Products) is used.	Enter Card Reader mode		
USBPIDH: USB Product	ID High By	rte (0x08)					
PID 1	R/W	[7:0]	0x00	Bits 15–8 of USB product ID reported during card reader enumeration. If this register is written, the written value is used for USB enumeration, otherwise a default PID of 0x38A4 is used.	Enter Card Reader mode		
USBPIDL: USB Product	ID Low Byt	te (0x09)					
PID 2	R/W	[7:0]	0x00	Bits 7–0 of USB product ID reported during card reader enumeration. If this register is written, the written value is used for USB enumeration, otherwise if zero, a default PID of 0x38A4 is used.	Enter Card Reader mode		
Test Register (0x0A)							
Test Register	R/W	_	0x00	Do not write to this register	_		
Test Register (0x0B)	_	_	_				
Test Register	R/W	_	0x00	Do not write to this register	_		
Test Register (0x0C)		ı	T				
Test Register	R/W	_	0x00	Do not write to this register	_		
Test Register (0x0D)		T	T				
Test Register	R/W	_	0x00	Do not write to this register	_		

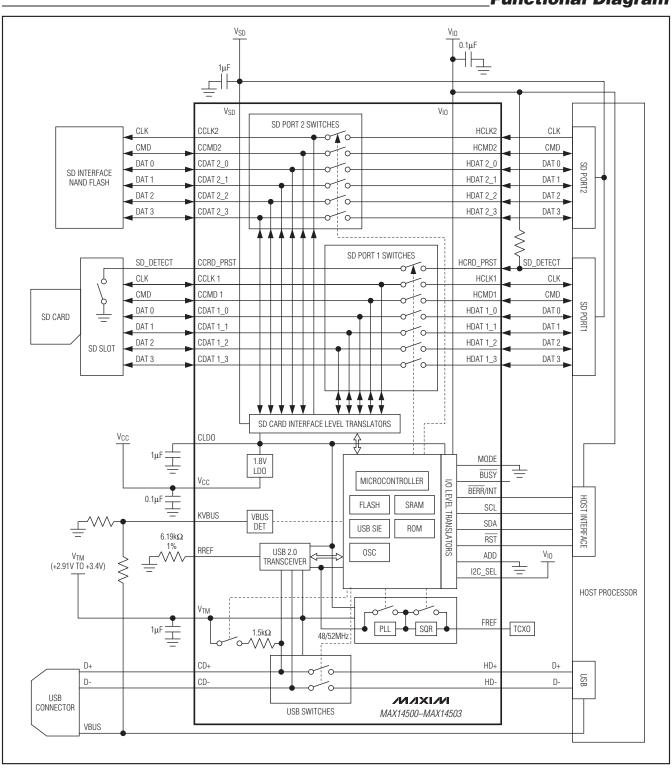
### Register Map (continued)

	l				
FIELD NAME	READ WRITE	BITS	RESET	DESCRIPTION	VALID WHEN
Test Register (0x0E)					•
Test Register	R/W	ĺ	0x00	Do not write to this register	_
FWP: Firmware Portal (0	x0F)				
Firmware Portal	R/W	[7:0]	0x00	Contact factory. Do not write to this register.	
IRQ1: Interrupt Request	Register 1	(0x10)			
RFU	R	7		Reserved for future use	
USBFS	R	6		0 = no change in USB full-speed mode status 1 = change in USB full-speed mode status	Enter Card Reader mode
USBSR	R	5		0 = no change in USB suspend/resume status 1 = change in USB suspend/resume status	Enter Card Reader mode
VTM	R	4		0 = no change in V <sub>TM</sub> detector status 1 = change in V <sub>TM</sub> detector status	WAKEUP = 1
VSD	R	3		0 = no change in V <sub>SD</sub> detector status 1 = change in V <sub>SD</sub> detector status	WAKEUP = 1
VBUS	R	2		0 = no change in VBUS detector status 1 = change in VBUS detector status	WAKEUP = 1
BSY	R	1		0 = no change in BUSY status 1 = change in BUSY status	WAKEUP = 1
SDSTAT	R	0		0 = no change in SD card present status 1 = change in SD card present status	Enter Card Reader mode
IRQ2: Interrupt Request	Register 2	(0x11)	•		
Firmware Update	R	7		Contact factory	Code download
RFU	R	[6:0]		Reserved for future use	_
STATUS1: Status Regist	er 1 (0x12)				
RFU	R	7		Reserved for future use	_
USBFS	R	6		0 = no connection or Hi-Speed connection 1 = full-speed connection	Enter Card Reader mode
USBSR	R	5		0 = USB resume 1 = USB suspend	Enter Card Reader mode
VTM	R	4		0 = no voltage 1 = V <sub>TM</sub> supply present	WAKEUP = 1
VSD	R	3		0 = no voltage 1 = V <sub>SD</sub> supply present	WAKEUP = 1
VBUS	R	2		0 = no voltage 1 = VBUS supply present	WAKEUP = 1
BSY	R	1		0 = not busy 1 = busy	WAKEUP = 1

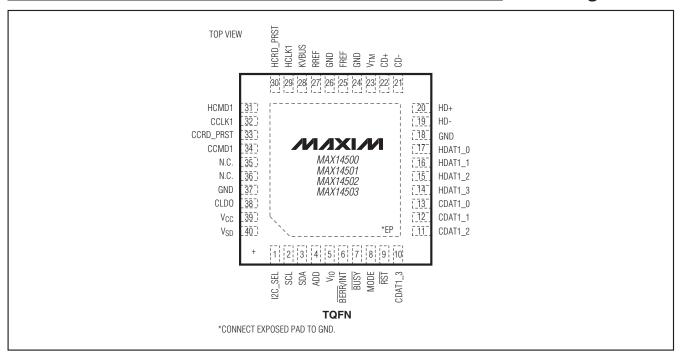
### Register Map (continued)

FIELD NAME	READ WRITE	BITS	RESET	DESCRIPTION	VALID WHEN
SDSTAT	R	0		The insert/removal status is only valid for the card currently set to Card Reader mode (Reg 0x00 bits 1-2) 0 = no card 1 = card present	Enter Card Reader mode
STATUS2: Status Regist	er 2 (0x13)		•		
RFU	R	[7:0]		Reserved for future use	_
FWUGRRH: Firmware Up	grade Res	ponse Da	ta High By	te (0x14)	
High Byte of Response Data	R	[7:0]		Contact factory	Code download
FWUPGRL: Firmware Up	grade Res	ponse Dat	a Low Byte	e (0x15)	
Low Byte of Response Data	R	[7:0]		Contact factory	Code download
RFU Register (0x16)					•
RFU	R	[7:0]		Reserved for future use	_
RFU Register (0x17)					
RFU	R	[7:0]		Reserved for future use	_
RFU Register (0x18)					
RFU	R	[7:0]		Reserved for future use	_
RFU Register (0x19)					
RFU	R	[7:0]		Reserved for future use	_
RFU Register (0x1A)					
RFU	R	[7:0]		Reserved for future use	_
Firmware Incremental Re	evision (0x	1B)			-
Firmware Incremental Revision	R	[7:0]		Firmware incremental revision	WAKEUP = 1
Firmware Minor Revision	1 (0x1C)				
Firmware Minor Revision	R	[7:0]		Firmware minor revision	WAKEUP = 1
Firmware Major Revision	ı (0x1D)				
Firmware Major Revision	R	[7:0]		Firmware major revision	WAKEUP = 1
Chip Revision (0x1E)			•		
Chip Revision	R	[7:0]		Chip revision	WAKEUP = 1
Package Type (0x1F)					
Package Type	R	[7:0]		0x00 = 40-lead TQFN 0x05 = 56-bump WLP 0xFF = unknown	WAKEUP = 1

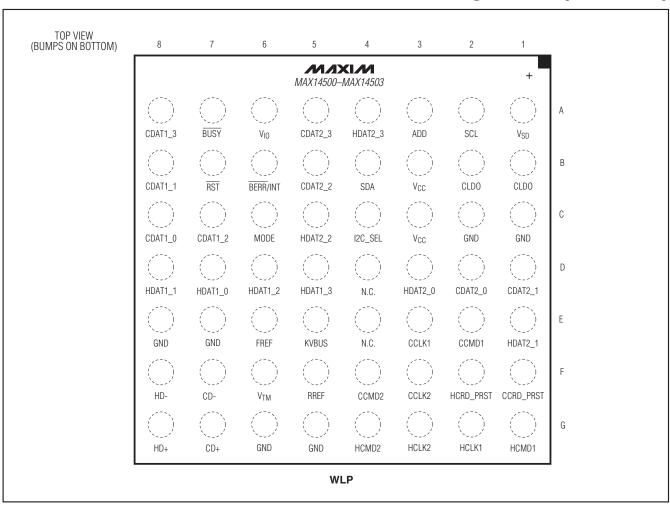
### Functional Diagram



### **Pin Configurations**



### **Pin Configurations (continued)**



#### **Chip Information**

PROCESS: CMOS

#### Package Information

For the latest package outline information and land patterns, go to <a href="www.maxim-ic.com/packages">www.maxim-ic.com/packages</a>. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
40 TQFN-EP	T4055-1	<u>21-0140</u>
56 WLP	W563B3+1	<u>21-0090</u>

\_ M/XI/M

### **Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/08	Initial release	_
1	4/09	Fixed data sheet to reflect new rev material including EC table, Pin Description, Applications Information, Functional Diagram, and Pin Configurations	1–41

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