LMH0303

LMH0303 3 Gbps HD/SD SDI Cable Driver with Cable Detect



Literature Number: SNLS285F



LMH0303

3 Gbps HD/SD SDI Cable Driver with Cable Detect

General Description

The LMH0303 3 Gbps HD/SD SDI Cable Driver with Cable Detect is designed for use in SMPTE 424M, SMPTE 292M, SMPTE 344M, and SMPTE 259M serial digital video applications. The LMH0303 drives 75Ω transmission lines (Belden 1694A, Belden 8281, or equivalent) at data rates up to 2.97 Gbps.

The LMH0303 includes intelligent sensing capabilities to improve system diagnostics. The cable detect feature senses near-end termination to determine if a cable is correctly attached to the output BNC. Input loss of signal (LOS) detects the presence of a valid signal at the input of the cable driver. These sensing features may be used to alert the user of a system fault and activate a deep power save mode, reducing the cable driver's power consumption to 4 mW. These features are accessible via an SMBus interface.

The LMH0303 provides two selectable slew rates for SMPTE 259M and SMPTE 424M / 292M compliance. The output amplitude is adjustable $\pm 10\%$ in 5 mV steps via the SMBus.

The LMH0303 is powered from a single 3.3V supply. Power consumption is typically 130 mW in SD mode and 155 mW in HD mode. The LMH0303 is available in a 16-pin LLP package.

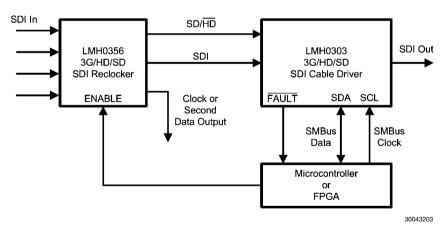
Features

- SMPTE 424M, SMPTE 292M, SMPTE 344M, and SMPTE 259M compliant
- Data rates to 2.97 Gbps
- Supports DVB-ASI at 270 Mbps
- Cable detect on output
- Loss of signal detect at input
- Output driver power down control
- Typical power consumption: 130 mW in SD mode and 155 mW in HD mode
- Power save mode typical power consumption: 4 mW
- Single 3.3V supply operation
- Differential input
- 75Ω differential output
- Selectable slew rate
- Industrial temperature range: -40°C to +85°C
- 16-pin LLP package
- Footprint compatible with the LMH0302

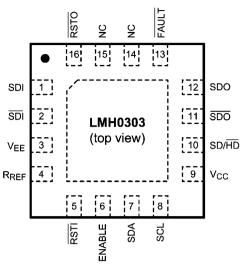
Applications

- SMPTE 424M, SMPTE 292M, SMPTE 344M, and SMPTE 259M serial digital interfaces
- Digital video routers and switches
- Distribution amplifiers

Typical Application



Connection Diagram



30043205

The exposed die attach pad is a negative electrical terminal for this device. It should be connected to the negative power supply voltage.

16-Pin LLP Order Number LMH0303SQ NS Package Number SQB16A

Ordering Information

Part Number	Package	Quantity
LMH0303SQ	16 Lead LLP	Reel of 1000
LMH0303SQE	16 Lead LLP	Reel of 250
LMH0303SQX	16 Lead LLP	Reel of 4500

Pin Descriptions

Pin	Name	Description
1	SDI	Serial data true input.
2	SDI	Serial data complement input.
3	V _{EE}	Negative power supply (ground).
4	R _{REF}	Bias resistor. Connect a 750 Ω resistor to V_{CC} .
5	RSTI	Reset input. RSTI has an internal pullup. H = Normal operation. L = Device reset. The device operates with default register settings. Forcing RSTI low also forces RSTO low.
6	ENABLE	Output driver enable. ENABLE has an internal pullup. H = Normal operation. L = Output driver powered off.
7	SDA	SMBus bidirectional data pin. When functioning as an output, it is open drain. This pin requires an external pullup.
8	SCL	SMBus clock input. SCL is input only. This pin requires an external pullup.
9	V _{CC}	Positive power supply (+3.3V).
10	SD/HD	Output slew rate control. SD/HD has an internal pulldown. H = Output rise/fall time complies with SMPTE 259M. L = Output rise/fall time complies with SMPTE 424M / 292M.
11	SDO	Serial data complement output.
12	SDO	Serial data true output.
13	FAULT	Fault open drain output flag. Requires external pullup resistor and may be wire ORed with multiple cable drivers. H = Normal operation. L = Loss of signal or termination fault for any output.
14	NC	No connect. Not bonded internally.
15	NC	No connect. Not bonded internally.
16	RSTO	Reset output. RSTO is automatically set to 1 when register 0 is written. It can be reset back to zero by forcing RSTI to zero to reset the device. Used to daisy chain multiple cable drivers on the same SMBus.
DAP	V _{EE}	Connect exposed DAP to negative power supply (ground).

Absolute Maximum Ratings (Note 1)

Supply Voltage: -0.5 V to 3.6 VInput Voltage (all inputs) $-0.3 \text{V to } \text{V}_{\text{CC}} + 0.3 \text{V}$ Output Current 28 mAStorage Temperature Range $-65 ^{\circ}\text{C} \text{ to } +150 ^{\circ}\text{C}$

Lead Temperature
(Soldering 4 Sec) +260°C

Package Thermal Resistance

Junction Temperature

 θ_{JA} 16-pin LLP +43°C/W θ_{JC} 16-pin LLP +7°C/W

 ESD Rating (HBM)
 8 kV

 ESD Rating (MM)
 400V

 ESD Rating (CDM)
 2 kV

Recommended Operating Conditions

Supply Voltage ($V_{CC} - V_{EE}$): 3.3V ±5% Operating Free Air Temperature (T_A) -40°C to +85°C

DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 2, Note 3).

+125°C

Symbol	Parameter	Conditions	Reference	Min	Тур	Max	Units
V _{CMIN}	Input Common Mode Voltage		SDI, SDI	1.6 + V _{SDI} /2		V _{CC} – V _{SDI} /2	٧
V _{SDI}	Input Voltage Swing	Differential		100		2200	mV _{P-P}
V _{CMOUT}	Output Common Mode Voltage		SDO, SDO		V _{CC} - V _{SDO}		٧
V _{SDO}	Output Voltage Swing	Single-ended, 75Ω load, $R_{REF} = 750\Omega$ 1%		720	800	880	mV _{P-P}
V _{IH}	Input Voltage High Level		SD/HD,	2.0			V
$\overline{V_{IL}}$	InputVoltage Low Level		ENABLE			0.8	V
I _{CC}	Supply Current	SD/HD = 0, SDO/SDO enabled			47	57	mA
		SD/HD = 1, SDO/SDO enabled			40	47	mA
		SDO/SDO disabled			1.3	2.5	mA
SMBus [OC Specifications						
V_{SIL}	Data, Clock Input Low Voltage					0.8	V
V_{SIH}	Data, Clock Input High Voltage			2.1		V_{SDD}	V
I _{SPULLUP}	Current through pullup resistor or current source	V _{OL} = 0.4 V		4			mA
V _{SDD}	Nominal Bus Voltage			3.0		3.6	V
I _{SLEAKB}	Input Leakage per bus segment	(Note 6)		-200		200	μΑ
I _{SLEAKP}	Input Leakage per pin			-10		10	μΑ
C _{SI}	Capacitance for SDA and SCL	(Note 6, Note 7)				10	pF

AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 3).

Symbol	Parameter	Conditions	Reference	Min	Тур	Max	Units
DR _{SDI}	Input Data Rate		SDI, SDI			2970	Mbps
t _{jit}	Additive Jitter	2.97 Gbps	SDO, SDO		20		ps _{P-P}
		1.485 Gbps			18		ps _{P-P}
		270 Mbps			15		ps _{P-P}
t _r ,t _f	Output Rise Time, Fall Time	SD/HD = 0, 20% - 80%,			90	130	ps
		SD/HD = 1, 20% - 80%		400		800	ps
	Mismatch in Rise/Fall Time	SD/HD = 0				30	ps
		SD/HD = 1				50	ps
	Duty Cycle Distortion	SD/HD = 0, 2.97 Gbps, (<i>Note 4</i>)				27	ps
		SD/HD = 0, 1.485 Gbps, (<i>Note 4</i>)				30	ps
		SD/HD = 1, (<i>Note 4</i>)	7			100	ps
t _{os}	Output Overshoot	SD/HD = 0, (<i>Note 4</i>)	7			10	%
		SD/HD = 1, (<i>Note 4</i>)	7			8	%
RL _{SDO}	Output Return Loss	5 MHz - 1.5 GHz, (<i>Note 5</i>)	7	15			dB
		1.5 GHz - 3.0 GHz, (<i>Note 5</i>)	7	10			dB
SMBus A	AC Specifications						
f _{SMB}	Bus Operating Frequency			10		100	kHz
t _{BUF}	Bus free time between Stop and Start Condition			4.7			μs
t _{HD:STA}	Hold time after (repeated) Start Condition. After this period, the first clock is generated.	At I _{SPULLUP} = MAX		4.0			μs
t _{SU:STA}	Repeated Start Condition setup time			4.7			μs
t _{SU:STO}	Stop Condition setup time			4.0			μs
t _{HD:DAT}	Data hold time			300			ns
t _{SU:DAT}	Data setup time			250			ns
t _{LOW}	Clock low period			4.7			μs
t _{HIGH}	Clock high period			4.0		50	μs
t _F	Clock/Data Fall Time					300	ns
t _R	Clock/Data Rise Time					1000	ns
t _{POR}	Time in which device must be operational after power on					500	ms

Note 1: "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be guaranteed. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of "Electrical Characteristics" specifies acceptable device operating conditions.

5

Note 2: Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to $V_{\text{EE}} = 0$ Volts.

Note 3: Typical values are stated for V_{CC} = +3.3V and T_A = +25°C.

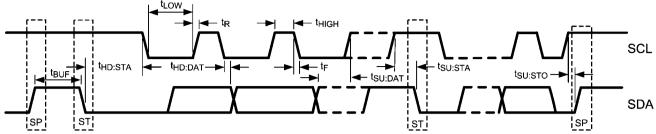
Note 4: Specification is guaranteed by characterization.

Note 5: Output return loss is dependent on board design. The LMH0303 meets this specification on the SD303 evaluation board.

Note 6: Recommended value — Parameter not tested.

Note 7: Recommended maximum capacitive load per bus segment is 400 pF.

Timing Diagram



SMBus Timing Parameters

30043206

Device Operation

INPUT INTERFACING

The LMH0303 accepts either differential or single-ended input. For single-ended operation, the unused input must be properly terminated.

OUTPUT INTERFACING

The LMH0303 uses current mode outputs. Single-ended output levels are 800 mV_{P-P} into 75 Ω AC-coupled coaxial cable with an R_{REF} resistor of 750 Ω . The R_{REF} resistor is connected between the R_{REF} pin and V_{CC}. The only resistor value that should be used for R_{RFF} is 750 Ω .

The R_{REF} resistor should be placed as close as possible to the R_{REF} pin. In addition, the copper in the plane layers below the R_{REF} network should be removed to minimize parasitic capacitance.

OUTPUT SLEW RATE CONTROL

The LMH0303 output rise and fall times are selectable for either SMPTE 259M or SMPTE 424M / 292M compliance via the SD/HD pin. For slower rise and fall times, or SMPTE 259M compliance, SD/HD is set high. For faster rise and fall times, or SMPTE 424M and SMPTE 292M compliance, SD/HD is set low. SD/HD may also be controlled using the SMBus, provided the SD/HD pin is held low. SD/HD has an internal pulldown.

OUTPUT ENABLE

The SDO/SDO output driver can be enabled or disabled with the ENABLE pin. When set low, the output driver is powered off and the LMH0303 enters a deep power save mode. ENABLE has an internal pullup.

INPUT LOS OF SIGNAL DETECTION (LOS)

The LMH0303 detects when the input signal does not have a video-like pattern. Self oscillation and low levels of noise are rejected. This loss of signal detect allows a very sensitive input stage that is robust against coupled noise without any degradation of jitter performance.

Via the SMBus, the loss of signal detect can either add an input offset or mute the outputs. An offset is added by default. Additionally, the loss of signal detect can be linked to the ENABLE functionality so that when the $\overline{\text{LOS}}$ goes low, ENABLE will also go low.

OUTPUT CABLE DETECTION

The LMH0303 detects when an output is locally terminated. When a video signal (or AC test signal) is present on SDI, the device senses the SDO and $\overline{\text{SDO}}$ amplitudes. If the output is not properly terminated (via a terminated cable or local terminated)

mination), the amplitude will be higher than expected, and the Termination Fault signal is asserted. The Termination Fault signal is de-asserted when the proper termination is applied. This feature allows the system designer the flexibility to react to cable attachment and removal. Note that a long length of cable will look like a proper termination at the device output.

The cable driver must be enabled for the termination detection to operate. If the Termination Fault will be used to power down the LMH0303, then periodic polling (enabling) is recommended to monitor the output termination. For example, when a Fault condition is triggered, ENABLE can be driven low to power down the device. The LMH0303 should be re-enabled periodically to check the status of the output termination. The LMH0303 needs to be powered on for roughly 4 ms for Termination Fault detection to work.

SMBus Interface

The System Management Bus (SMBus) is a two-wire interface designed for the communication between various system component chips. By accessing the control functions of the circuit via the SMBus, pincount is kept to a minimum while allowing a maximum amount of versatility. The LMH0303 has several internal configuration registers which may be accessed via the SMBus.

The 7-bit default address for the LMH0303 is 17h. The LSB is set to 0b for a WRITE and 1b for a READ, so the 8-bit default address for a WRITE is 2Eh and the 8-bit default address for a READ is 2Fh. The SMBus address may be dynamically changed

In applications where there might be several LMH0303s, the SDA, SCL, and FAULT pins can be shared. The SCL, SDA, and FAULT pins are open drain and require external pullup resistors. Multiple LMH0303s may have the FAULT pin wire ORed. This signal becomes active when either loss of signal is detected or any termination faults are detected. The registers may be read in order to determine the cause. Additionally, each signal can be masked from the FAULT pin.

TRANSFER OF DATA VIA THE SMBus

During normal operation the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

START: A High-to-Low transition on SDA while SCL is High indicates a message START condition.

STOP: A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.

IDLE: If SCL and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

SMBus TRANSACTIONS

The device supports WRITE and READ transactions. See Register Description table for register address, type (Read/Write, Read Only), default value and function information.

WRITING A REGISTER

To write a register, the following protocol is used (see SMBus 2.0 specification).

- The Host drives a START condition, the 7-bit SMBus address, and a "0" indicating a WRITE.
- The Device (Slave) drives the ACK bit ("0").
- 3. The Host drives the 8-bit Register Address.
- 4. The Device drives an ACK bit ("0").
- 5. The Host drives the 8-bit data byte.
- 6. The Device drives an ACK bit ("0").
- 7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

READING A REGISTER

To read a register, the following protocol is used (see SMBus 2.0 specification).

- 1. The Host drives a START condition, the 7-bit SMBus address, and a "0" indicating a WRITE.
- 2. The Device (Slave) drives the ACK bit ("0").
- 3. The Host drives the 8-bit Register Address.
- 4. The Device drives an ACK bit ("0").
- 5. The Host drives a START condition.
- The Host drives the 7-bit SMBus Address, and a "1" indicating a READ.
- 7. The Device drives an ACK bit "0".
- 8. The Device drives the 8-bit data value (register contents).
- The Host drives a NACK bit "1" indicating end of the READ transfer.
- 10. The Host drives a STOP condition.

Application Information

Figure 1 shows the application circuit for the LMH0303.

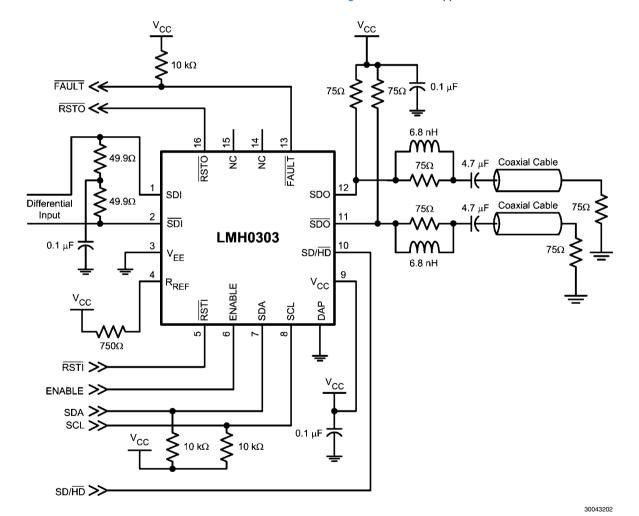
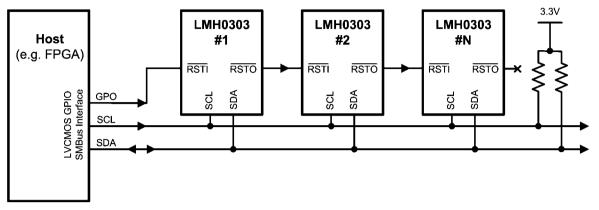


FIGURE 1. Application Circuit

COMMUNICATING WITH MULTIPLE LMH0303 CABLE DRIVERS VIA THE SMBus

A common application for the LMH0303 will utilize multiple cable driver devices. Even though the LMH0303 devices all have the same default SMBus device ID (address), it is still possible for them share the SMBus signals as shown in *Figure 2*. A third signal is required from the host to the first

device. This signal acts as a "Enable / Reset" signal. Additional LMH0303s are controlled from the upstream device. In this control scheme, multiple LMH0303s may be controlled via the two-wire SMBus and the use of one GPO (General Purpose Output) signal. Other SMBus devices may also be connected to the two wires, assuming they have their own unique SMBus addresses.



30043207

FIGURE 2. SMBus Configuration for Multiple LMH0303 Cable Drivers

The $\overline{\text{RSTI}}$ pin of the first device is controlled by the system with a GPO pin from the host. The first LMH0303 $\overline{\text{RSTO}}$ pin is then daisy chained to the next device's $\overline{\text{RSTI}}$ pin. That device's $\overline{\text{RSTO}}$ pin is connected to the next device and so on.

The procedure at initialization is to:

- Hold the host GPO pin Low in RESET, to the first device.
 RSTO output default is also Low which holds the next device in RESET in the chain.
- Raise the host GPO signal to LMH0303 #1 RSTI input pin.
- Write to Address 8'h2E (7'h17) Register 0 with the new address value (e.g. 8'h2C (7'h16).
- 4. Upon writing Register 0 in LMH0303 #1, its RSTO signal will switch High. Its new address is 8'h2C (7'h16), and

- the next LMH0303 in the chain will now respond to the default address of 8'h2E (7'h17).
- 5. The process is repeated until all LMH0303 devices have a unique address loaded.
- 6. Direct SMBus writes and reads may now take place between the host and any addressed device.

The 7-bit address field allows for 128 unique addresses. The above procedure allows for the reprogramming of the LMH0303 devices such that multiple devices may share the two-wire SMBus. Make sure all devices on the bus have unique device IDs.

If power is toggled to the system, the SMBus address routine needs to be repeated.

SMBus Registers

TABLE 1. SMBus Registers

Address	R/W	Name	Bits	Field	Default	Description	
00h	R/W	ID	7:1	DEVID	0010111	Device ID. Writing this register will force the RSTO pin high.	
						Further accesses to the device must use this 7-bit address.	
			0	RSVD	0	Reserved as 0. Always write 0 to this bit.	
01h	R	STATUS	7:3	RSVD	00000	Reserved.	
			2	TFN	0	Termination Fault for SDI.	
						0: No Termination Fault Detected.	
						1: Termination Fault Detected.	
			1	TFP	0	Termination Fault for SDI.	
						0: No Termination Fault Detected.	
						1: Termination Fault Detected.	
			0	LOS	0	Loss Of Signal (LOS) detect at input.	
						0: No Signal Detected.	
						1: Signal Detected.	
02h	R/W	MASK	7	SD	0	SD Rate select bit. If the SD/ $\overline{\text{HD}}$ pin is set to V_{CC} , it overrides	
						this bit. With the SD/HD pin set to ground, this bit selects the	
						output edge rate as follows:	
						0: HD edge rate.	
						1: SD edge rate.	
			6	RSVD	0	Reserved as 0. Always write 0 to this bit.	
			5	PD	0	Power Down for SDO output stage. If the ENABLE pin is set	
						to ground, it overrides this bit. With the ENABLE pin set to	
						V _{CC} , PD functions as follows:	
						0: SDO active.	
						1: SDO powered down.	
			4:3	RSVD	00	Reserved as 00. Always write 00 to these bits.	
			2	MTFN	0	Mask TFN from affecting FAULT pin.	
						0: TFN=1 will cause FAULT to be 0.	
						1: TFN=1 will not affect FAULT; the condition is masked off.	
			1	MTFP	0	Mask TFP from affecting FAULT pin.	
						0: TFP=1 will cause FAULT to be 0.	
						1: TFP=1 will not affect FAULT; the condition is masked off.	
			0	MLOS	0	Mask LOS from affecting FAULT pin.	
						0: LOS=0 will cause FAULT to be 0.	
						1: LOS=0 will not affect FAULT; the condition is masked off.	

9

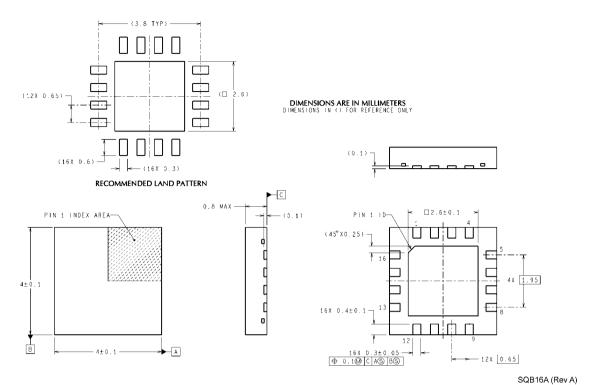
Address R/W		Bits	F: - 1 - 1		
03h R/W			Field	Default	Description
	/ DIRECTION	7	HDTFThreshLSB	1	Least Significant Bit for HDTFThresh detection threshold.
					Combines with HDTFThresh bits in register 04h.
		6	SDTFThreshLSB	1	Least Significant Bit for SDTFThresh detection threshold.
					Combines with SDTFThresh bits in register 05h.
		5:3	RSVD	000	Reserved as 000. Always write 000 to these bits.
		2	DTFN	0	Direction of TFN that affects FAULT pin (when not masked).
					0: TFN=1 will cause FAULT to be 0 (when the condition is
					not masked off).
					1: TFN=0 will cause FAULT to be 0 (when the condition is
					not masked off).
		1	DTFP	0	Direction of TFP that affects FAULT pin (when not masked).
					0: TFP=1 will cause FAULT to be 0 (when the condition is
					not masked off).
					1: TFP=0 will cause FAULT to be 0 (when the condition is
					not masked off).
		0	DLOS	0	Direction of $\overline{\text{LOS}}$ that affects $\overline{\text{FAULT}}$ pin (when not masked).
					0: $\overline{\text{LOS}}=0$ will cause $\overline{\text{FAULT}}$ to be 0 (when the condition is
					not masked off).
					1: LOS=1 will cause FAULT to be 0 (when the condition is
					not masked off).
04h R/W	OUTPUT	7:5	HDTFThresh	100	Sets the Termination Fault threshold for SDO, when SD is
					set to HD rates (0). Combines with HDTFThreshLSB in
					register 03h (default for combined value is 1001).
		4:0	AMP	10000	SDO output amplitude in roughly 5 mV steps.

Address	R/W	Name	Bits	Field	Default	Description
05h	R/W	OUTPUTCTRL	7	RSVD	0	Reserved as 0. Always write 0 to this bit.
			6	FLOSOF	0	Force \overline{\text{IOS}} to always OFF in regard to its effect on the output signal. This forces the device into either the mute or "add offset" state. The \overline{\text{IOS}} bit in register 01h still reflects the correct state of \overline{\text{IOS}}. 0: \overline{\text{IOS}} operates normally, muting or adding offset as specified by the MUTE bit. 1: Muting or adding offset is always in place as specified by the MUTE bit.
			5	FLOSON	0	Force LOS to always ON in regard to its effect on the output signal. This prevents the device from muting or adding offset. The LOS bit in register 01h still reflects the correct state of LOS. 0: LOS operates normally, muting or adding offset as specified in the MUTE bit. 1: Muting or adding offset never occurs.
			4	LOSEN	0	Configures $\overline{\text{LOS}}$ to be combined with the ENABLE functionality. 0: Only the PD bit and ENABLE pin affect the power down state of the output drivers. 1: If the ENABLE pin is set to ground, it powers down the output drivers regardless of the state of $\overline{\text{LOS}}$ or the PD bit. With the ENABLE pin set to V_{CC} , $\overline{\text{LOS}}$ =0 will power down the output drivers, and $\overline{\text{LOS}}$ =1 will leave the power down state dependent on the PD bit.
			3	MUTE	0	Selects whether the device will MUTE when loss of signal is detected or add an offset to prevent self oscillation. When an input signal is detected (LOS=1), the device will operate normally. 0: Loss of signal will force a small offset to prevent self oscillation. 1: Loss of signal will force the channel to MUTE.
			2:0	SDTFThresh	010	Sets the Termination Fault threshold for SDO, when SD is set to SD rates (1). Combines with SDTFThreshLSB in register 03h (default for combined value is 0101).
06h	R/W	RSVD	7:0	RSVD	00000000	Reserved as 00000000. Always write 00000000 to these bits.
07h	R/W	RSVD	7:0	RSVD	00000000	Reserved as 00000000. Always write 00000000 to these bits.
08h	R/W	TEST	7:5	CMPCMD	0000	Compare command. Determines whether the peak value or the current value of the Termination Fault counters is read in registers 0Ah and 0Bh. 000: Resets compare value to 00; registers 0Ah and 0Bh show current counter values. Sets detection to look for MAX peak values. 001: Capture counter 0. Register 0Ah shows peak value. 010: Capture counter 1. Register 0Bh shows peak value. 011, 100: Reserved. 101: Resets compare value to 1Fh. Sets detection to look for MIN peak values. 110, 111: Reserved.
		I		1	1	

11

Address	R/W	Name	Bits	Field	Default	Description
09h	R	REV	7:5	RSVD	000	Reserved.
			4:3	DIREV	10	Die Revision.
			2:0	PARTID	011	Part Identifier. Note that single output devices (LMH0303) have the LSB=1. Dual output devices (LMH0307) have the LSB=0.
0Ah	R	TFPCOUNT	7:5	RSVD	000	Reserved.
			4:0	TFPCOUNT	00000	This is either the current value of TFP Counter, or the peak value of the counter, depending on CMPCMD in register 08h.
0Bh	R	TFNCOUNT	7:5	RSVD	000	Reserved.
			4:0	TFNCOUNT	00000	This is either the current value of TFN Counter, or the peak value of the counter, depending on CMPCMD in register 08h.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Pin LLP Order Number LMH0303SQ NS Package Number SQB16A

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at: www.national.com

Pr	oducts	Design Support		
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench	
Audio	www.national.com/audio	App Notes	www.national.com/appnotes	
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns	
Data Converters	www.national.com/adc	Samples	www.national.com/samples	
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards	
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging	
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green	
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts	
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality	
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback	
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy	
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions	
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero	
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic	
PLL/VCO	www.national.com/wireless	PowerWise® Design University	www.national.com/training	

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2011 National Semiconductor Corporation

For the most current product information visit us at www.national.com



National Semiconductor Americas Technical Support Center Email: support@nsc.com Tel: 1-800-272-9959 National Semiconductor Europe Technical Support Center Email: europe.support@nsc.com National Semiconductor Asia Pacific Technical Support Center Email: ap.support@nsc.com

National Semiconductor Japan Technical Support Center Email: jpn.feedback@nsc.com

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products Applications

Audio www.ti.com/audio Communications and Telecom www.ti.com/communications **Amplifiers** amplifier.ti.com Computers and Peripherals www.ti.com/computers dataconverter.ti.com Consumer Electronics www.ti.com/consumer-apps **Data Converters DLP® Products** www.dlp.com **Energy and Lighting** www.ti.com/energy DSP dsp.ti.com Industrial www.ti.com/industrial Clocks and Timers www.ti.com/clocks Medical www.ti.com/medical Interface interface.ti.com Security www.ti.com/security

Logic Space, Avionics and Defense <u>www.ti.com/space-avionics-defense</u>

Power Mgmt power.ti.com Transportation and Automotive www.ti.com/automotive
Microcontrollers microcontroller.ti.com Video and Imaging www.ti.com/video

RFID <u>www.ti-rfid.com</u>
OMAP Mobile Processors www.ti.com/omap

Wireless Connectivity <u>www.ti.com/wirelessconnectivity</u>

TI E2E Community Home Page <u>e2e.ti.com</u>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2011, Texas Instruments Incorporated