# 32-Channel 256 Gray-Shade High Voltage Driver 

## Ordering Information

| Device | Package Option |  |
| :---: | :---: | :---: |
|  | 64-Lead 3-Sided Plastic Gullwing | Die |
| HV62208 | HV62208PG | HV62208X |

## Features

- $\mathrm{HVCMOS}^{\circledR}$ technology
- 5V CMOS inputs
- Up to 80 V output voltage
- PWM gray shade conversion
- Capable of 256 levels of gray shading
- Balanced shift clock complies with RS-422
- 8 MHz shift and count clock frequency
- 16 MHz data throughput rate
- 8 bit data bus
- 32 outputs per device
- BLANK function


## General Description

## Not recommended for new designs. Please use HV632 instead.

The HV622 is a 32-channel gray-shade column driver IC designed for driving electrofluorescent displays. Using Supertex's unique $\mathrm{HVCMOS}^{\circledR}$ technology, it is capable of 256 levels of gray shading by PWM conversion.
The shift clock is a balanced clock with electrical characteristics complying with EIA RS-422 standard. Input data, in groups of eight, is latched into a set of data latches on both edges of the shift clock. The data shifted in the first data latch corresponds to $\mathrm{HV}_{\text {OUT }} 1$, the second data latch corresponds to $\mathrm{HV}_{\text {OUT }}{ }^{2}$, and so on. These data are compared to the contents of the master binary counter which counts on both edges of the count clock. Each time the master counter begins to decrement from 1111 1111, the data in the data latches are compared with the contents of the counter; if they match, the corresponding outputs will go high. The master counter counts down to 00000001 and then starts to count up again. The outputs that are at high will stay at high until the contents of the counter match the data in the data latches again. Therefore, the higher the binary data in the data latches, the longer the outputs will stay at high. Thus, different high voltage pulse widths are produced. When the counter reaches its 11111111 count while counting up, the device is ready for the next operation cycle. A data value of 00000000 produces no pulse; the output stays low.
The BLANK input signal will reset the master counter to all ones (1111 1111) and set all high voltage outputs to low.

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## Electrical Characteristics

(Over recommended conditions of $\mathrm{V}_{\mathrm{DD}}=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{PP}}=70 \mathrm{~V}, \mathrm{~V}_{\mathrm{NN}}=-10 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise noted)

## Low-Voltage DC Characteristics (Digital)

| Symbol | Parameter | Min | Max | Units | Conditions |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{DD}}$ | Low-voltage digital supply voltage | 4.5 | 5.5 | V |  |
| $\mathrm{I}_{\mathrm{DD}}$ | $\mathrm{V}_{\mathrm{DD}}$ supply current |  | 25 | mA | $\mathrm{f}_{\mathrm{SC}}=8 \mathrm{MHz}, \mathrm{f}_{\mathrm{CC}}=8 \mathrm{MHz}$ |
| $\mathrm{I}_{\mathrm{DDQ}}$ | Quiescent $\mathrm{V}_{\mathrm{DD}}$ supply current |  | 100 | $\mu \mathrm{~A}$ | $\mathrm{All} \mathrm{V}_{\mathrm{IN}}=\mathrm{GND}$, Count Clock $=\mathrm{V}_{\mathrm{DD}}$ |
| $\mathrm{I}_{\mathrm{IH}}$ | High-level input current |  | 10 | $\mu \mathrm{~A}$ | $\mathrm{~V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{DD}}$ |
| $\mathrm{I}_{\mathrm{IL}}$ | Low-level input current |  | -10 | $\mu \mathrm{~A}$ | $\mathrm{~V}_{\mathrm{IL}}=\mathrm{GND}$ |
| $\mathrm{I}_{\mathrm{OH}}$ | High-level output current | -1.0 |  | mA |  |
| $\mathrm{I}_{\mathrm{OL}}$ | Low-level ouptut current | 1.0 |  | mA |  |


| Symbol | Parameter | Max | Units | Conditions |  |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{DD}}$ | Low-voltage analog supply voltage | 4.5 | 5.5 | V |  |
| $\mathrm{I}_{\mathrm{DD}}$ | $\mathrm{V}_{\mathrm{DD}}$ supply current |  | 100 | $\mu \mathrm{~A}$ | $\mathrm{f}_{\mathrm{SC}}=8 \mathrm{MHz}, \mathrm{f}_{\mathrm{CC}}=8 \mathrm{MHz}$ |
| $\mathrm{I}_{\mathrm{DDQ}}$ | Quiescent $\mathrm{V}_{\mathrm{DD}}$ supply current |  | 100 | $\mu \mathrm{~A}$ | $\mathrm{All} \mathrm{V}_{\mathrm{IN}}=\mathrm{GND}$, Count Clock $=\mathrm{V}_{\mathrm{DD}}$ |

High-Voltage DC Characteristics

| Symbol | Parameter | Min | Max | Units | Conditions |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\text {PPQ }}$ | Quiescent $\mathrm{V}_{\text {PP }}$ supply current |  | 100 | $\mu \mathrm{~A}$ | All HV ${ }_{\text {OUT }}$ low or high |
| $\mathrm{I}_{\text {OUT(p) }}$ | P-channel output current | -4.0 |  | mA |  |
| $\mathrm{I}_{\text {OUT(n) }}$ | N-channel output current | 4.0 |  | mA |  |

## AC Characteristics

| Symbol | Parameter | Min | Max | Units | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{f}_{\mathrm{Sc}}$ | Shift clock frequency |  | 8.0 | MHz |  |
| $\mathrm{f}_{\mathrm{CC}}$ | Count clock frequency |  | 8.0 | MHz |  |
| $\mathrm{f}_{\text {DIN }}$ | Data In frequency |  | 16 | MHz |  |
| $\mathrm{t}_{\mathrm{CW}}$ | Chip select pulse width | 80 |  | ns |  |
| $\mathrm{t}_{\text {css }}$ | Chip select to shift clock set-up time | 15 |  | ns |  |
| $\mathrm{t}_{\mathrm{CSH}}$ | Chip select to shift clock hold time | 45 |  | ns |  |
| $\mathrm{t}_{\text {ScC }}$ | Shift clock cycle time | 125 |  | ns |  |
| $\mathrm{t}_{\text {DSS }}$ | Data to shift clock set-up time | 10 |  | ns |  |
| $\mathrm{t}_{\text {DSH }}$ | Data to shift clock hold time | 52 |  | ns |  |
| $\mathrm{t}_{\mathrm{DW}}$ | Data In pulse width | 62 |  | ns |  |
| tLCW | Load count pulse width | 75 |  | ns |  |
| $\mathrm{t}_{\mathrm{ccw}}$ | Count clock pulse width | 62.5 |  | ns |  |
| $\mathrm{t}_{\mathrm{ccc}}$ | Count clock cycle time | 125 |  | ns |  |
| $\mathrm{t}_{\text {LCD }}$ | Load count to count clock delay | 100 |  | ns |  |
| $\mathrm{t}_{\mathrm{CCD}}$ | Count clock to $\mathrm{HV}_{\text {OUT }}$ turn-on/turn-off |  | 600 | ns | $\mathrm{C}_{\mathrm{L}}=15 \mathrm{pF}$ |
| $\mathrm{t}_{\text {BLW }}$ | BLANK pulse width | 700 |  | ns |  |
| $\mathrm{t}_{\text {BLD }}$ | BLANK to $\mathrm{HV}_{\text {OUT }}$ delay |  | 500 | ns | $C_{L}=15 \mathrm{pF}$ |
| $\mathrm{t}_{\text {CDD }}$ | Count clock delay between count down and count up cycles | 500 |  | ns |  |

## Recommended Operating Conditions

| Symbol | Parameter | Min | Max | Units | Conditions |
| :--- | :--- | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{DD}}$ | Logic supply voltage | 4.5 | 5.5 | V |  |
| $\mathrm{~V}_{\mathrm{PP}}$ | Positive high-voltage supply | 12 | 70 | V |  |
| $\mathrm{~V}_{\mathrm{NN}}$ | Negative high-voltage supply | -8 | -10 | V |  |
| $\mathrm{~V}_{\mathrm{IL}}$ | Low-level input voltage | 0 | 1 | V |  |
| $\mathrm{~V}_{\mathrm{IH}}$ | High-level input voltage | $\mathrm{V}_{\mathrm{DD}}-1$ | $\mathrm{~V}_{\mathrm{DD}}$ | V |  |
| $\mathrm{f}_{\mathrm{SC}}$ | Shift clock frequency |  | 8 | MHz |  |
| $\mathrm{f}_{\mathrm{CC}}$ | Count clock frequency |  | 8 | MHz |  |
| $\mathrm{T}_{\mathrm{A}}$ | Operating temperature | -40 | +85 | ${ }^{\circ} \mathrm{C}$ |  |

## Pin Definitions

| Pin \# | Name | I/O | Function |
| :--- | :--- | :---: | :--- |
| $27-30$ | D1 - D8 |  |  |
| $36-29$ |  | I | Inputs for binary-format parallel data <br> (D8 is the most significant bit) |
| 34 | Shift Clock | I | Triggers data on both edges |
| 35 | Shift Clock | I | Triggers data on both edges |
| 31 | Count Clock | I | Input to the counter |
| 24 | CSI | I | Chip select input to enable the device to accept data |
| 25 | CSO | O | Chip select output to enable the next device |
| 33 | Load Count | I | Input to initiate the counting |
| 26 | Blank | I | Input to reset the counter and HV |
| $4-19$ | HV | OUT $1-H V_{\text {OUT }} 32$ | O |
| $46-61$ | High-voltage outputs |  |  |
| 23,43 | V $_{\text {PP }}$ | - | Positive high-voltage supply |
| 41 | $\mathrm{~V}_{\text {DD }}$ (Analog) | - | Low-voltage analog supply voltage |
| 40 | $\mathrm{~V}_{\text {DD }}$ (Digital) | - | Low-voltage digital supply voltage |
| 22,44 | $\mathrm{~V}_{\text {NN }}$ | - | Negative high-voltage supply |
| $20-21$ | GND (Digital) | - | Digital ground |
| 42 | GND (Analog) |  | Analog ground |

## Input and Output Equivalent Circuits



Functional Block Diagram


## Timing Diagrams



Timing Diagrams


## Pin Configurations

Package Outline



[^0]:    02/96/022
    
    
    
    

