



ISO7240A ISO7241A ISO7242A

SLLS905E -MAY 2008-REVISED JANUARY 2010

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1-Mbps QUAD DIGITAL ISOLATORS

Check for Samples: ISO7240A, ISO7241A, ISO7242A

FEATURES

- 4000-V_{peak} Isolation, 560-V_{peak} V_{IORM}
 - UL 1577, IEC 60747-5-2 (VDE 0884, Rev 2),
 IEC 61010-1, IEC 60950-1 and CSA
 Approved
- 4 kV ESD Protection
- Operate With 3.3-V or 5-V Supplies
- Typical 25-Year Life at Rated Working Voltage (See Application Note (SLLA197) and Figure 10)
- High Electromagnetic Immunity (See Application Report (SLLA181))
- –40°C to 125°C Operating Range

APPLICATIONS

- Industrial Fieldbus
- Computer Peripheral Interface
- Servo Control Interface
- Data Acquisition

DESCRIPTION

See the Product Notification section. The ISO7240A, ISO7241A and ISO7242A are quad-channel digital isolators with multiple channel configurations and output enable functions. These devices have logic input and output buffers separated by Ti's silicon dioxide (SiO₂) isolation barrier. Used in conjunction with isolated power supplies, these devices block high voltage, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

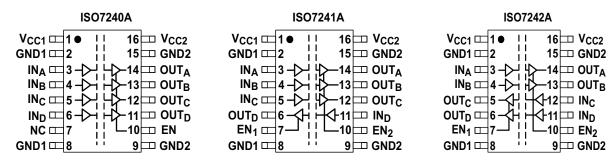
The ISO7240A has all four channels in the same direction while the ISO7241A has three channels the same direction and one channel in opposition. The ISO7242A has two channels in each direction.

The devices have TTL input thresholds and a noise-filter at the input that prevents transient pulses from being passed to the output of the device.

A periodic update pulse is sent across the barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic high state. (See ISO7240CF (SLLS869) or contact TI for a logic low failsafe option).

These devices may be powered from either 3.3-V or 5-V supplies on either side in any 3.3-V / 3.3-V, 5-V / 5-V, 5-V / 3.3-V, or 3.3-V / 5-V combination. Note that the signal input pins are 5-V tolerant regardless of the voltage supply level being used.

These devices are characterized for operation over the ambient temperature range of -40°C to 125°C.





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTION DIAGRAM

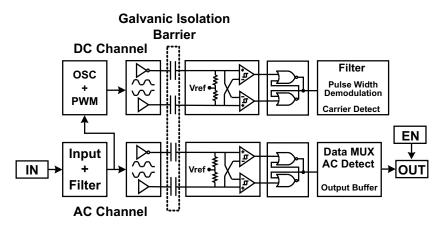


Table 1. Device Function Table ISO724x (1)

INPUT V _{CC}	OUTPUT V _{CC}	INPUT (IN)	OUTPUT ENABLE (EN)	OUTPUT (OUT)
		Н	H or Open	Н
DU	PU	L	H or Open	L
PU		Х	L	Z
		Open	H or Open	Н
PD	PU	Х	H or Open	Н
PD	PU	Х	L	Z

(1) PU = Powered Up; PD = Powered Down; X = Irrelevant; H = High Level; L = Low Level

AVAILABLE OPTIONS

PRODUCT	SIGNALING RATE	INPUT THRESHOLD	CHANNEL CONFIGURATION	MARKED AS	ORDERING NUMBER ⁽¹⁾
ISO7240ADW	1 Mbps	~1.5 V (TTL)	4/0	ISO7240A ISO724	
1307240ADW	1 Mbps	(CMOS compatible)	4/0	13072408	ISO7240ADWR (reel)
ISO7241ADW	1 Mbpo	~1.5 V (TTL)	3/1	ISO7241A	ISO7241ADW (rail)
1507241ADW	1 Mbps	(CMOS compatible)	3/1	1507241A	ISO7241ADWR (reel)
10070404 DW	4 1 1 1 1 1 1	~1.5 V (TTL)	0/0	10070404	ISO7242ADW (rail)
ISO7242ADW	1 Mbps (CMOS c		2/2	ISO7242A	ISO7242ADWR (reel)

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI
website at www.ti.com.



ABSOLUTE MAXIMUM RATINGS(1)

NSTRUMENTS

					VALUE	UNIT	
V_{CC}	Supply voltag	je ⁽²⁾ , V _{CC1} , V _{CC2}			-0.5 to 6	V	
V_{I}	Voltage at IN	, OUT, EN			-0.5 to 6	V	
IO	Output current					mA	
		Human Body Model	JEDEC Standard 22, Test Method A114-C.01		±4	kV	
ESD	Electrostatic discharge	Field-Induced-Charged Device Model	JEDEC Standard 22, Test Method C101	All pins	±1		
		Machine Model	ANSI/ESDS5.2-1996		±200	V	
T_{J}	Maximum jun	ction temperature			170	°C	

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage ⁽¹⁾ , V _{CC1} , V _{CC2}		3.15		5.5	V
I _{OH}	High-level output current				4	mA
I _{OL}	Low-level output current					mA
t _{ui}	Input pulse width	ISO724xA	1			μS
1/t _{ui}	Signaling rate	ISO724xA	0		1000	kbps
V_{IH}	High-level input voltage (IN) (EN on all devices)	ISO724xA	2		V_{CC}	V
V_{IL}	Low-level input voltage (IN) (EN on all devices)	150724XA	0		0.8	٧
T_{J}	Junction temperature				150	ů
Н	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification				1000	A/m

⁽¹⁾ For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

IEC 60747-5-2 INSULATION CHARACTERISTICS(1)

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	SPECIFICATIONS	UNIT
V _{IORM}	Maximum working insulation voltage		560	V
		After Input/Output Safety Test Subgroup 2/3 $V_{PR} = V_{IORM} \times 1.2$, $t = 10 \text{ s}$, Partial discharge < 5 pC	672	V
V_{PR}	Input to output test voltage	Method a, $V_{PR} = V_{IORM} \times 1.6$, Type and sample test with t = 10 s, Partial discharge < 5 pC	896	V
		Method b1, V _{PR} = V _{IORM} × 1.875, 100 % Production test with t = 1 s, Partial discharge < 5 pC	1050	V
V _{IOTM}	Transient overvoltage	t = 60 s	4000	V
R _S	Insulation resistance	V _{IO} = 500 V at T _S	>10 ⁹	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

⁽²⁾ All voltage values are with respect to network ground terminal and are peak voltage values.



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ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V⁽¹⁾ OPERATION

, over recommended operating conditions (unless otherwise noted)

	PAR	AMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPL	Y CURRENT		•	•		•	
	10070404	Quiescent	V V OV All shounds as lead EN OV		1	3	^
	ISO7240A	1 Mbps	$V_1 = V_{CC}$ or 0 V, All channels, no load, EN ₂ at 3 V		1	3	mA
	ISO7241A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN ₁ at 3 V,		6.5	44	A
I _{CC1}	1507241A	1 Mbps	EN ₂ at 3 V		0.5	11	mA
	ISO7242A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN ₁ at 3 V,		10	16	mA
	1501242A	1 Mbps	EN ₂ at 3 V		10	16	IIIA
	ISO7240A	Quiescent	V V or O.V. All channels no load EN et 2.V.		15	22	mA
	1507240A	1 Mbps	$V_1 = V_{CC}$ or 0 V, All channels, no load, EN ₂ at 3 V		16	22	MA
	ISO7241A	Quiescent	$V_1 = V_{CC}$ or 0 V, All channels, no load, EN ₁ at 3 V,		13	20	mA
-	1307241A	1 Mbps	EN ₂ at 3 V		13	20	ША
	ISO7242A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN ₁ at 3 V,		10	16	mA
	1301242A	1 Mbps	EN ₂ at 3 V		10	16	IIIA
ELECT	RICAL CHAR	ACTERISTICS					
I _{OFF}	Sleep mode	e output current	EN at 0 V, Single channel		0		μΑ
V	High lovel o	output voltage	I _{OH} = -4 mA, See Figure 1	V _{CC} - 0.8			V
V _{OH}	i ligit-level (Julput Vollage	$I_{OH} = -20 \mu A$, See Figure 1	$V_{CC} - 0.1$			V
V	Low lovel o	utput voltage	I _{OL} = 4 mA, See Figure 1			0.4	V
V _{OL}	Low-level o	utput voltage	I_{OL} = 20 μ A, See Figure 1			0.1	V
V _{I(HYS)}	Input voltag	e hysteresis			150		mV
I _{IH}	High-level i	nput current	IN from 0 \/ to \/			10	^
I _{IL}	Low-level in	nput current	IN from 0 V to V _{CC}	-10			μА
Cı	Input capac	itance to ground	IN at V_{CC} , $V_I = 0.4 \sin (4E6\pi t)$		2		pF
CMTI	Common-m	node transient immunity	V _I = V _{CC} or 0 V, See Figure 4	25	50		kV/μs

⁽¹⁾ For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} , t _{PHL}	Propagation delay	Con Figure 4	40		95	
PWD	Pulse-width distortion ⁽¹⁾ t _{PHL} - t _{PLH}	See Figure 1			10	ns
t _{sk(o)}	Channel-to-channel output skew (2)				2	ns
t _r	Output signal rise time	0		2		
t _f	Output signal fall time	See Figure 1		2		ns
t _{PHZ}	Propagation delay, high-level-to-high-impedance output			15	20	
t _{PZH}	Propagation delay, high-impedance-to-high-level output	Con Figure 2		15	20	
t _{PLZ}	Propagation delay, low-level-to-high-impedance output	See Figure 2		15	20	ns
t _{PZL}	Propagation delay, high-impedance-to-low-level output			15	20	
t _{fs}	Failsafe output delay time from input power loss	See Figure 3		12		μS

⁽¹⁾ Also referred to as pulse skew.

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⁽²⁾ $t_{sk(0)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.



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ELECTRICAL CHARACTERISTICS: V_{CC1} at 5-V, V_{CC2} at 3.3-V⁽¹⁾ OPERATION

over recommended operating conditions (unless otherwise noted)

	PARAME	TER	TEST CONI	DITIONS	MIN	TYP	MAX	UNIT
SUPPL	Y CURRENT						•	
	10070404	Quiescent	\\ \\ \ = 0 \\ All = b =	and the stand		1	3	1
	ISO7240A	1 Mbps	$V_I = V_{CC}$ or 0 V, All channels	, no load, EN ₂ at 3 V		1	3	mA
	10070444	Quiescent	V _I = V _{CC} or 0 V, All channels	, no load, EN ₁ at 3 V,		0.5	4.4	A
I _{CC1}	ISO7241A	1 Mbps	EN ₂ at 3 V			6.5	11	mA
	10070404	Quiescent	V _I = V _{CC} or 0 V, All channels	$V_I = V_{CC}$ or 0 V, All channels, no load, EN ₁ at 3 V,		10	16	mA
	ISO7242A	1 Mbps	EN ₂ at 3 V			10	16	IIIA
	10070404	Quiescent	\\ \\ \ = 0 \\ All = b =	and the stand		9.5	15	1
	ISO7240A	1 Mbps	$V_I = V_{CC}$ or 0 V, All channels	, no load, EN ₂ at 3 V		10	15	mA
	10070444	Quiescent	VI - VC Ci C V, 7tii Gridinicis, no lodd, E141 dt C V,		8	13	1	
I _{CC2}	ISO7241A	1 Mbps				8	13	mA
	10070404	Quiescent	V _I = V _{CC} or 0 V, All channels	, no load, EN ₁ at 3 V,		6	10	1
	ISO7242A	1 Mbps	EN ₂ at 3 V	•		6		mA
ELECT	RICAL CHARAC	TERISTICS					•	
I _{OFF}	Sleep mode or	utput current	EN at 0 V, Single channel			0		μА
			A mA Coo Figure 4	ISO7240A	V _{CC} - 0.4			V
V_{OH}	High-level outp	out voltage	I _{OH} = -4 mA, See Figure 1	ISO724x (5-V side)	V _{CC} - 0.8			
			$I_{OH} = -20 \mu A$, See Figure 1		V _{CC} - 0.1			
\/	Law laval auto	ut voltoge	I _{OL} = 4 mA, See Figure 1				0.4	V
V _{OL}	Low-level outp	ut voitage	I_{OL} = 20 μ A, See Figure 1				0.1	V
$V_{I(HYS)}$	Input voltage h	nysteresis				150		mV
I _{IH}	High-level inpu	ıt current	INI frame O.V. to V.	N. (10	^
I _{IL}	Low-level inpu	t current	IN from 0 V to V _{CC}		-10			μА
Cı	Input capacita	nce to ground	IN at V_{CC} , $V_{I} = 0.4 \sin (4E6\pi)$	i)		2		pF
CMTI	Common-mod	e transient immunity	V _I = V _{CC} or 0 V, See Figure 4		25	50		kV/μs

⁽¹⁾ For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 5-V, V_{CC2} at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} , t _{PHL}	Propagation delay	See Figure 1	40		100	
PWD	Pulse-width distortion ⁽¹⁾ t _{PHL} - t _{PLH}	See Figure 1			11	ns
	Channel to show all output allow (2)				3	
t _{sk(o)}	Channel-to-channel output skew (2)			0	1	ns
t _r	Output signal rise time	Con Figure 4		2		
t _f	Output signal fall time	See Figure 1		2		ns
t _{PHZ}	Propagation delay, high-level-to-high-impedance output			15	20	
t _{PZH}	Propagation delay, high-impedance-to-high-level output	Can Figure 0		15	20	
t _{PLZ}	Propagation delay, low-level-to-high-impedance output	See Figure 2		15	20	ns
t _{PZL}	Propagation delay, high-impedance-to-low-level output			15	20	
t _{fs}	Failsafe output delay time from input power loss	See Figure 3		18		μS

⁽¹⁾ Also known as pulse skew

⁽²⁾ t_{sk(o)} is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.



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ELECTRICAL CHARACTERISTICS: V_{CC1} at 3.3-V, V_{CC2} at 5-V⁽¹⁾ OPERATION

over recommended operating conditions (unless otherwise noted)

	PARAMET	ER	TEST CON	DITIONS	MIN	TYP	MAX	UNIT
SUPPLY	' CURRENT				•		,	
	ISO7240A	Quiescent	V _I = V _{CC} or 0 V, All channels, no	load, EN ₂ at 3 V		0.5	1 2	mA
		1 Mbps				1 4	7	
I _{CC1}	ISO7241A	Quiescent 1 Mbps	$V_I = V_{CC}$ or 0 V, All channels, no	load, EN ₁ at 3 V, EN ₂ at 3 V		4	7	mA
		Quiescent				6	10	
	ISO7242A	1 Mbps	$V_I = V_{CC}$ or 0 V, All channels, no	$V_{I} = V_{CC}$ or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V		6	10	mA
	ISO7240A	Quiescent	\\ \\ ar 0 \\ All channels no	lood FN at 2 V		15	22	mA
1307240A		1 Mbps	$V_I = V_{CC}$ or 0 V, All channels, no	VCC of V V, All Chamiles, no load, Live at V		16	22	mA
I _{CC2}	ISO7241A	Quiescent	$V_{I} = V_{CC}$ or 0 V, All channels, no load, EN ₁ at 3 V, EN ₂ at 3 V			13	20	mA
.002		1 Mbps	1, 1,00 0. 0 1,7 0.1.0			13	20	
	ISO7242A	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no	load, EN ₁ at 3 V, EN ₂ at 3 V		10	16	mA
	1 Mbps V ₁ = V _{CC} or 0 V, All charmers, no load, Ein ₁ at 3 V, Ein ₂ at ECTRICAL CHARACTERISTICS					10	16	
ELECTR			I					
I _{OFF}	Sleep mode	output current	EN at V _{CC} , Single channel			0		μΑ
			I _{OH} = -4 mA, See Figure 1	ISO7240A	V _{CC} - 0.4			
V_{OH}	High-level c	output voltage	ISO724x (5-V side)		$V_{CC} - 0.8$			V
			$I_{OH} = -20 \mu A$, See Figure 1		$V_{CC} - 0.1$			
V_{OL}	I ow-level o	utput voltage	I _{OL} = 4 mA, See Figure 1				0.4	V
V OL	2011 10101 0		I_{OL} = 20 μ A, See Figure 1				0.1	
$V_{I(HYS)}$	Input voltag	e hysteresis				150		mV
I _{IH}	High-level in	nput current	INI from 0 \/ to \/				10	
$I_{\rm IL}$	Low-level in	put current	IN from 0 V to V _{CC}		-10			μΑ
C _I	Input capac ground	itance to	IN at V_{CC} , $V_{I} = 0.4 \sin (4E6\pi t)$	IN at V_{CC} , $V_{I} = 0.4 \sin (4E6\pi t)$		2		pF
CMTI	Common-m	ode transient	V _I = V _{CC} or 0 V, See Figure 4		25	50		kV/μs

⁽¹⁾ For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} at 3.3-V and V_{CC2} at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} , t _{PHL}	Propagation delay	Con Figure 4	40		100	
PWD	Pulse-width distortion ⁽¹⁾ t _{PHL} - t _{PLH}	See Figure 1			11	ns
	Observation also and automatical and (2)				2.5	
t _{sk(o)}	Channel-to-channel output skew (2)			0	1	ns
t _r	Output signal rise time	0		2		
t _f	Output signal fall time	See Figure 1		2		ns
t _{PHZ}	Propagation delay, high-level-to-high-impedance output			15	20	
t _{PZH}	Propagation delay, high-impedance-to-high-level output	0 Firms 0		15	20	
t _{PLZ}	Propagation delay, low-level-to-high-impedance output	See Figure 2		15	20	ns
t _{PZL}	Propagation delay, high-impedance-to-low-level output			15	20	
t _{fs}	Failsafe output delay time from input power loss	See Figure 3		12		μS

⁽¹⁾ Also known as pulse skew

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⁽²⁾ t_{sk(o)} is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.



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ELECTRICAL CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3 $V^{(1)}$ OPERATION

over recommended operating conditions (unless otherwise noted)

	PARAME	TER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPL	Y CURRENT			•		•	
	10070404	Quiescent	V V and V all abounds and local EN at 0 V		0.5	1	1
	ISO7240A	1 Mbps	$V_I = V_{CC}$ or 0 V, all channels, no load, EN ₂ at 3 V		1	2	mA
	10070444	Quiescent	$V_1 = V_{CC}$ or 0 V, all channels, no load, EN ₁ at 3 V,		4	7	
I _{CC1}	ISO7241A	1 Mbps	EN ₂ at 3 V		4	7	A
	ISO7242A	Quiescent	$V_1 = V_{CC}$ or 0 V, all channels, no load, EN ₁ at 3 V,		6	10	mA
	1507242A	1 Mbps	EN ₂ at 3 V		6	10	
•	ISO7240A	Quiescent	V V or 0 V all channels no load EN at 2 V		9.5	15	mA
	1507240A	1 Mbps	$V_I = V_{CC}$ or 0 V, all channels, no load, EN_2 at 3 V		10	15	mA
	ISO7241A	Quiescent	$V_1 = V_{CC}$ or 0 V, all channels, no load, EN ₁ at 3 V,		8	13	
	1307241A	1 Mbps	EN ₂ at 3 V		8	13	mA
	ISO7242A	Quiescent	$V_I = V_{CC}$ or 0 V, all channels, no load, EN ₁ at 3 V,		6	10	IIIA
	1307242A	1 Mbps	EN ₂ at 3 V		6	10	
ELECTI	RICAL CHARACT	ERISTICS					
I _{OFF}	Sleep mode out	put current	EN at 0 V, single channel		0		μΑ
V	High-level outpu	ıt voltago	I _{OH} = -4 mA, See Figure 1	V _{CC} - 0.4			V
V _{OH}	r light-level outpu	it voltage	$I_{OH} = -20 \mu A$, See Figure 1	$V_{CC} - 0.1$			V
V	Low-level outpu	t voltogo	I _{OL} = 4 mA, See Figure 1			0.4	V
V _{OL}	Low-level outpu	i voltage	I _{OL} = 20 μA, See Figure 1			0.1	V
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I _{IH}	High-level input	current	IN from 0 \/ or \/			10	^
I _{IL}	Low-level input	current	IN from 0 V or V _{CC}	-10			μА
Cı	Input capacitano	ce to ground	IN at V _{CC} , V _I = 0.4 sin (4E6πt)		2		pF
CMTI	Common-mode	transient immunity	V _I = V _{CC} or 0 V, See Figure 4	25	50		kV/μs

⁽¹⁾ For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

SWITCHING CHARACTERISTICS: V_{CC1} and V_{CC2} at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

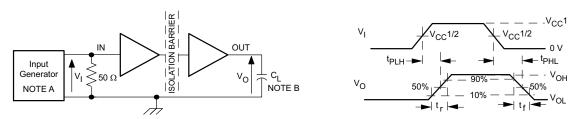
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t _{PLH} , t _{PHL}	Propagation delay	See Figure 4	45		110		
PWD	Pulse-width distortion t _{PHL} - t _{PLH} ⁽¹⁾	See Figure 1			12	ns	
	Channel to showed output alread (2)				3.5		
t _{sk(o)}	Channel-to-channel output skew (2)			0	1		
t _r	Output signal rise time	0		2		ns	
t _f	Output signal fall time	See Figure 1		2			
t _{PHZ}	Propagation delay, high-level-to-high-impedance output			15	20		
t _{PZH}	Propagation delay, high-impedance-to-high-level output	See Figure 2		15	20		
t _{PLZ}	Propagation delay, low-level-to-high-impedance output	See Figure 2		15	20	ns	
t _{PZL}	Propagation delay, high-impedance-to-low-level output			15	20		
t _{fs}	Failsafe output delay time from input power loss	See Figure 3		18		μS	

¹⁾ Also referred to as pulse skew.

⁽²⁾ t_{sk(o)} is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

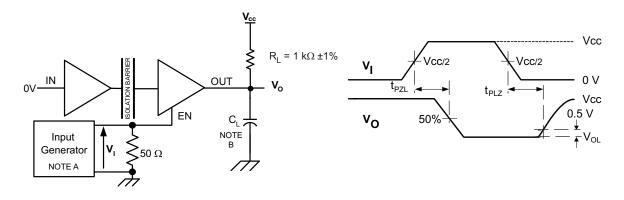


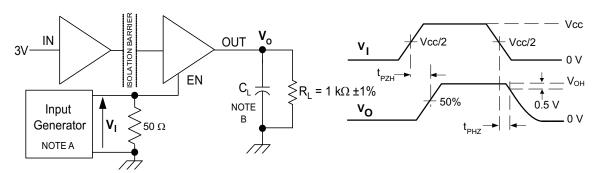
PARAMETER MEASUREMENT INFORMATION



- A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 50 kHz, 50% duty cycle, $t_r \leq$ 3 ns, $t_f \leq$ 3 ns, $Z_O = 50\Omega$.
- B. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms





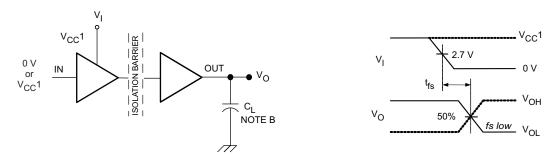
- A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 50 kHz, 50% duty cycle, $t_r \leq$ 3 ns, $t_f \leq$ 3 ns, $Z_O = 50\Omega$.
- B. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 2. Enable/Disable Propagation Delay Time Test Circuit and Waveform

INSTRUMENTS

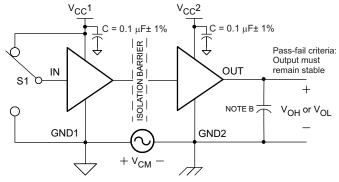
SLLS905E -MAY 2008-REVISED JANUARY 2010

PARAMETER MEASUREMENT INFORMATION (continued)



- A. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.
- B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 50 kHz, 50% duty cycle, $t_r \leq$ 3 ns, $t_f \leq$ 3 ns, $Z_O = 50\Omega$.

Figure 3. Failsafe Delay Time Test Circuit and Voltage Waveforms



- A. $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.
- B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 50 kHz, 50% duty cycle, $t_r \leq$ 3 ns, $t_f \leq$ 3 ns, $Z_O = 50\Omega$.

Figure 4. Common-Mode Transient Immunity Test Circuit and Voltage Waveform



DEVICE INFORMATION

PACKAGE CHARACTERISTICS

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal-to-terminal distance through air	8.34			mm
L(102)	Minimum external tracking (Creepage)	Shortest terminal-to-terminal distance across the package surface	8.1			mm
C _{TI}	Tracking resistance (comparative tracking index)	DIN IEC 60112/VDE 0303 Part 1	≥ 175			V
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R _{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device		>10 ¹²		Ω
C _{IO}	Barrier capacitance Input to output	V _I = 0.4 sin (4E6πt)		2		pF
Cı	Input capacitance to ground	V _I = 0.4 sin (4E6πt)		2		pF

IEC 60664-1 RATINGS TABLE

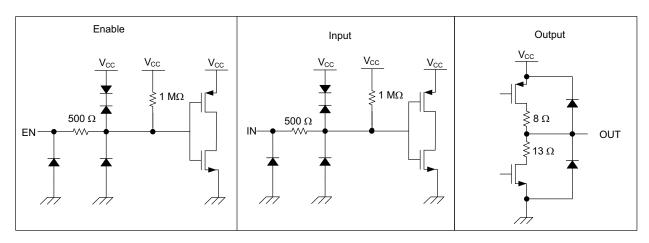
PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	IIIa
Installation classification	Rated mains voltage ≤150 VRMS	I-IV
Installation classification	Rated mains voltage ≤300 VRMS	I-III

REGULATORY INFORMATION

VDE	CSA	UL			
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program (1)			
File Number: 40016131	File Number: 1698195	File Number: E181974			

(1) Production tested ≥ 3000 Vrms for 1 second in accordance with UL 1577.

DEVICE I/O SCHEMATICS



THERMAL CHARACTERISTICS

INSTRUMENTS

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air	Low-K Thermal Resistance ⁽¹⁾		168		°C/W
	Junction-to-air	High-K Thermal Resistance	n-K Thermal Resistance 96.1			C/VV
θ_{JB}	Junction-to-Board Thermal Resistance			61		°C/W
θ_{JC}	Junction-to-Case Thermal Resistance			48		°C/W
P _D	Device Power Dissipation	V _{CC1} = V _{CC2} = 5.5 V, T _J = 150°C, C _L = 15 pF, Input a 50% duty cycle square wave			220	mW

⁽¹⁾ Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

TYPICAL CHARACTERISTIC CURVES

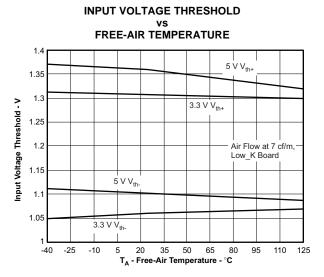


Figure 5.

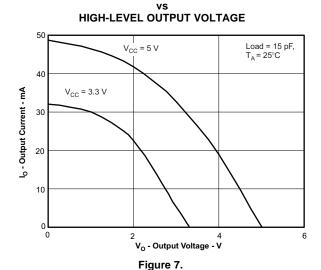
HIGH-LEVEL OUTPUT CURRENT

FREE-AIR TEMPERATURE V_{CC} at 5 V or 3.3 V, 2.0 Load = 15 pF, Air Flow at 7/cf/m, V_{CC1} - Failsafe Threshold - V 2.8 Low-K Board 2.7 2.6 2.5 2.4 2.3 2.2 -25 -10 110 35 50 65 80 95 125 -40 T_A - Free-Air Temperature - °C

V_{CC1} FAILSAFE THRESHOLD

Figure 6.

LOW-LEVEL OUTPUT CURRENT



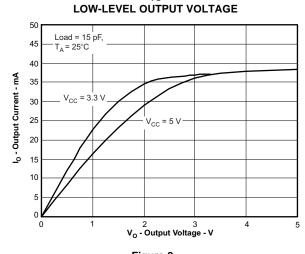


Figure 8.



APPLICATION INFORMATION

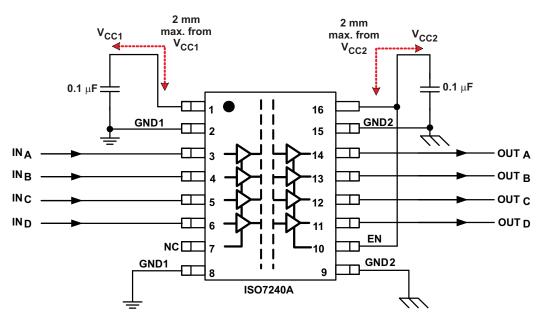


Figure 9. Typical ISO7240A Application Circuit

LIFE EXPECTANCY vs. WORKING VOLTAGE

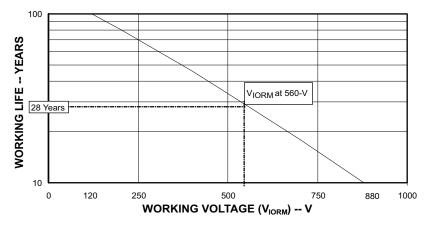


Figure 10. Time-Dependant Dielectric Breakdown Testing Results

PRODUCT NOTIFICATION

INSTRUMENTS

An ISO724xA anomaly occurs when a negative-going pulse below the specified 1 μ s minimum bit width is input to the device. The output locks in a logic-low condition until the next rising edge occurs after a 1 μ s period.

Positive noise edges in pulses of less than the minimum specified 1 μ s have no effect on the device, and are properly filtered.

To prevent noise from interfering with ISO724xA performance, it is recommended that an appropriately sized capacitor be placed on each input of the device

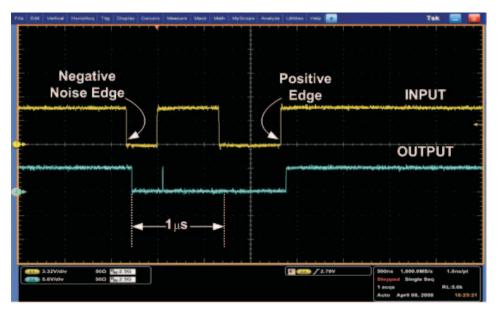


Figure 11. ISO724xA Anomaly

REVISION HISTORY

_	hanges from Original (May 2008) to Revision A	Page
•	Changed In the PACKAGE CHARACTERISTICS table, line 1, change L _(IO1) MIN value from 7.7mm to	8.34mm 10
CI	hanges from Revision A (July 2008) to Revision B	Page
•	Added information to the 1st Feature bullet to include CSA and IEC 60950-1 certification	1
•	Changed Figure 9 From: 20mm max.from V _{CCx} To: 2mm max. from V _{CCx}	12
CI	hanges from Revision B (December 2008) to Revision C	Page
•	Changed I _{CC1} for Quiescent and 1Mbps From: 10mA To: 11mA	
		4
<u>.</u>	Changed I _{CC1} for Quiescent and 1Mbps From: 10mA To: 11mA	
• CI	Changed I _{CC1} for Quiescent and 1Mbps From: 10mA To: 11mA	

Not Recommended for New Designs

ISO7240A ISO7241A ISO7242A



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Cł	nanges from Revision D (December 2009) to Revision E	Page
•	Added the IEC 60747-5-2 INSULATION CHARACTERISTIC table	3
•	Added C _{TI} - Tracking resistance (comparative tracking index to the PACKAGE CHARACTERISTICS table	10
•	Added the IEC 60664-1 RATINGS TABLE	10



2-Apr-2012

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
ISO7240ADW	NRND	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7240ADWG4	NRND	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7240ADWR	NRND	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7240ADWRG4	NRND	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7241ADW	NRND	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7241ADWG4	NRND	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7241ADWR	NRND	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7241ADWRG4	NRND	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7242ADW	NRND	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7242ADWG4	NRND	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7242ADWR	NRND	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7242ADWRG4	NRND	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

2-Apr-2012

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL. Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF ISO7241A:

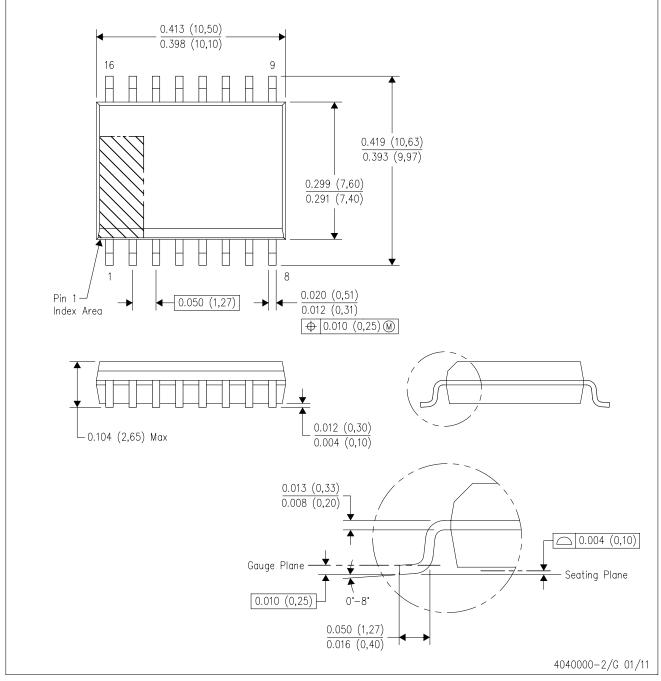
Enhanced Product: ISO7241A-EP

NOTE: Qualified Version Definitions:

Enhanced Product - Supports Defense, Aerospace and Medical Applications

DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



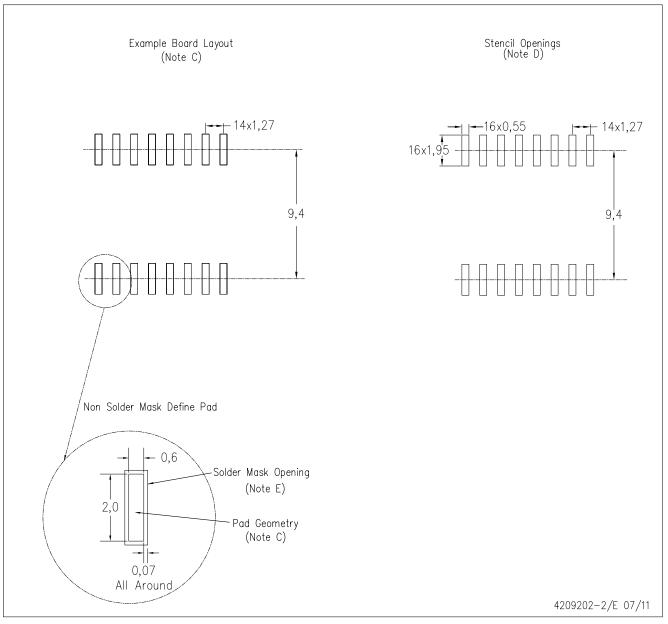
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AA.



DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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