Freescale Semiconductor Advance Information

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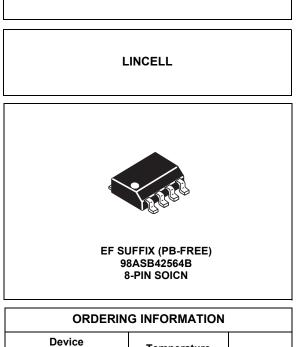
LIN 2.1 / SAEJ2602-2, LIN Physical Layer

The Local Interconnect Network (LIN) is a serial communication protocol, designed to support automotive networks in conjunction with a Controller Area Network (CAN). As the lowest level of a hierarchical network, LIN enables cost-effective communication with sensors and actuators when all the features of CAN are not required.

The three 33662 versions are designed to operate at different maximum baud rates. The MC33662LEF and MC33662SEF offer a normal baud rate (20 kbps), and the MC33662JEF, a slow baud rate (10 kbps). They integrate a fast baud rate (above 100 kbps), as reported by the RXD pin for test and programming modes. They provide excellent EMC (Electromagnetic Compatibility) and Radiated Emission performance, ESD (Electrostatic Discharge) robustness, and safe behavior, in the event of a LIN bus short-to-ground, or a LIN bus leakage during low-power mode.

Features

- Operational from a V_{SUP} of 7.0 to 18V DC, functional up to 27V DC, and handles 40 V during Load Dump
- Compatible with LIN Protocol Specification 1.3, 2.0, 2.1, and SAEJ2602-2
- Active bus wave shaping, offering excellent radiated emission performance
- Sustains up to 15.0 kV minimum ESD IEC61000-4-2 on the LIN Bus, 20 kV on the WAKE pin, and 25 kV on the VSUP pin
- · Very high immunity against electromagnetic interference
- Low standby current in Sleep mode
- Over-temperature protection
- · Local and remote Wake-up capability reported by the RXD pin
- · Fast baud rate selection reported by RXD pin
- · 5.0 V and 3.3 V compatible digital inputs without any required external components



33662

ORDERING INFORMATION					
Device (Add an R2 suffix for Tape and Reel orders)	Temperature Range (T _A)	Package			
MC33662LEF					
MC33662JEF	-40 to 125°C	8 SOICN			
MC33662SEF					

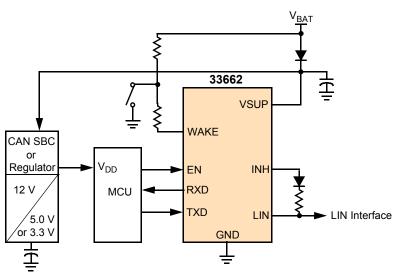


Figure 1. 33662 Master LIN Bus Simplified Application Diagram

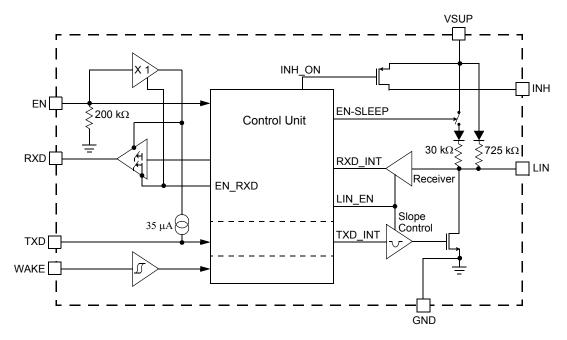


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DEVICE VARIATIONS

Table 1. Device Variations

Freescale Part No. (Add an R2 suffix for Tape and Reel orders)	Maximum Baud Rate	Temperature Range (T _A)	Package
MC33662LEF	20 kbps		
MC33662SEF	20 kbps with restricted limits for transmitter and receiver symmetry	-40 to 125°C	8 SOICN
MC33662JEF	10 kbps		



INTERNAL BLOCK DIAGRAM



PIN CONNECTIONS

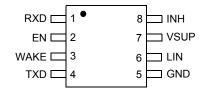


Figure 3. 33662 8-SOICN Pin Connections

Table 2. 33662 8-SOICN Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 23.

Pin	PIN NAME	Pin Function	Formal Name	Definition
1	RXD	Output	Data Output	This pin is the receiver output of the LIN interface which reports the state of the bus voltage to the MCU interface.
2	EN	Input	Enable Control	This pin controls the operation mode of the interface.
3	WAKE	Input	Wake Input	This pin is a high-voltage input used to wake-up the device from Sleep mode.
4	TXD	Input	Data Input	This pin is the transmitter input of the LIN interface which controls the state of the bus output.
5	GND	Ground	Ground	This pin is the device ground pin.
6	LIN	Input/Output	LIN Bus	This bidirectional pin represents the single-wire bus transmitter and receiver.
7	VSUP	Power	Power Supply	This pin is the device battery level power supply.
8	INH	Output	Inhibit Output	This pin can have two main functions: controlling an external switchable voltage regulator having an inhibit input, or driving an external bus resistor in the master node application.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS	1		
Power Supply Voltage			V
Normal Operation (DC)	V _{SUP(SS)}	-0.3 to 27	
Transient input voltage with external component (according to ISO7637-2 & ISO7637- 3 & "Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications" specification Rev1.1 / December 2nd, 2009) (See <u>Table 4</u> and <u>Figure 4</u>)			
- Pulse 1 (test up to the limit for Damage - Class A ⁽¹⁾)	V _{SUP(S1)}	-100	
- Pulse 2a (test up to the limit for Damage - Class $A^{(1)}$)	V _{SUP(S2A)}	+75	
- Pulse 3a (test up to the limit for Damage - Class $A^{(1)}$)	V _{SUP(S3A)}	-150	
- Pulse 3b (test up to the limit for Damage - Class $A^{(1)}$)	V _{SUP(S3B)}	+100	
- Pulse 5b (Class A) ⁽¹⁾	V _{SUP(S5B)}	-0.3 to 40	
WAKE			V
Normal Operation within series 2*18 k Ω resistor (DC)	V _{WAKE(SS)}	-27 to 40	
Transient input voltage with external component (according to ISO7637-2 & ISO7637- 3 & "Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications" specification Rev1.1 / December 2nd, 2009) (See <u>Table 4</u> and <u>Figure 5</u>)			
- Pulse 1 (test up to the limit for Damage - Class D ⁽²⁾)	V _{WAKE(S1)}	-100	
- Pulse 2a (test up to the limit for Damage - Class $D^{(2)}$)	V _{WAKE(S2A)}	+75	
- Pulse 3a (test up to the limit for Damage - Class D ⁽²⁾)	V _{WAKE(S3A)}	-150	
- Pulse 3b (test up to the limit for Damage - Class D ⁽²⁾)	V _{WAKE(S3B)}	+100	
Logic Voltage (RXD, TXD, EN Pins)	V _{LOG}	-0.3 to 5.5	V
LIN Bus Voltage			V
Normal Operation (DC)	V _{BUS(SS)}	-27 to 40	
Transient (Coupled Through 1.0 nF Capacitor, according to ISO7637-2 & ISO7637-3 & "Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications" specification Rev1.1 / December 2nd, 2009) (See <u>Table 4</u> and <u>Figure 6</u>)			
- Pulse 1 (test up to the limit for Damage - Class D ⁽²⁾)	V _{BUS(S1)}	-100	
- Pulse 2a (test up to the limit for Damage - Class $D^{(2)}$)	V _{BUS(S2A)}	+75	
- Pulse 3a (test up to the limit for Damage - Class $D^{(2)}$)	V _{BUS(S3A)}	-150	
- Pulse 3b (test up to the limit for Damage - Class $D^{(2)}$)	V _{BUS(S3B)}	+100	
INH Voltage/Current			V
DC Voltage	V _{INH}	-0.3 to V _{SUP} +0.3	
Transient (Coupled Through 1.0 nF Capacitor, according to ISO7637-2 & ISO7637-3 & "Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications" specification Rev1.1 / December 2nd, 2009) (See <u>Table 4</u> and <u>Figure 7</u>)			
- Pulse 1 (test up to the limit for Damage - Class D ⁽²⁾)	V _{INH(S1)}	-100	
- Pulse 2a (test up to the limit for Damage - Class D ⁽²⁾)	V _{INH(S2A)}	+75	
- Pulse 3a (test up to the limit for Damage - Class D ⁽²⁾)	V _{INH(S3A)}	-150	
- Pulse 3b (test up to the limit for Damage - Class D ⁽²⁾)	V _{INH(S3B)}	+100	

Notes

1. Class A: All functions of a device/system perform as designed during and after exposure to disturbance.

2. Class D: At least one function of the transceiver stops working properly during the test, and will return to proper operation automatically when the exposure to the disturbance has ended. No physical damage of the IC occurs.

Table 3. Maximum Ratings (continued)

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS (CONTINUED)			I
ESD Capability - AECQ100			V
Human Body Model - JESD22/A114 (C _{ZAP} = 100 pF, R _{ZAP} = 1500 Ω)			
LIN pin versus GND	V _{ESD1-1}	±10.0 k	
Wake pin versus GND	V _{ESD1-2}	±8.0 k	
INH pin versus GND	V _{ESD1-3}	±8.0 k	
All other pins	V _{ESD1-4}	±4.0 k	
Charge Device Model - JESD22/C101 (C _{ZAP} = 4.0 pF)			
Corner pins (Pins 1, 4, 5 and 8)	V _{ESD2-1}	±750	
All other pins (Pins 2, 3, 6 and 7)	V _{ESD2-2}	±500	
Machine Model - JESD22/A115 (C _{ZAP} = 220 pF, R_{ZAP} = 0 Ω)			
All pins	V _{ESD3-1}	±200	
According to "Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications" specification Rev1.1 / December 2nd, 2009 (C_{ZAP} = 150 pF,			
$R_{ZAP} = 330 \Omega$			
Contact Discharge, Unpowered	V _{ESD4-1}	±15 k	
LIN pin with 200 p E conseitor	V _{ESD4-2}	±15 k	
LIN pin with 220 pF capacitor	V _{ESD4-3}	±25 k	
VSUP (10 μF to ground) WAKE (2*18 kΩ serial resistor)	V _{ESD4-4}	±20 k	
INH pin	V _{ESD4-5}	±2.0 k	
LIN pin with 220 pF capacitor and indirect ESD coupling (according to ISO10605	V _{ESD4-6}	>±15 k	
- Annex F)	* ESD4-0		
According to ISO10605 - Rev 2008 test specification			
(2.0 k Ω / 150 pF) - Unpowered - Contact discharge	V _{ESD5-1}	±20 k	
LIN pin without capacitor	VESD5-1 V _{ESD5-2}	±20 k ±25 k	
LIN pin with 220 pF capacitor	VESD5-2 V _{ESD5-3}	±25 k	
VSUP (10 µF to ground)		±25 k	
WAKE (2*18 k Ω serial resistor)	V _{ESD5-4}	120 K	
(2.0 k Ω / 330 pF) - Powered - Contact discharge	N/	104	
LIN pin without capacitor	V _{ESD6-1}	±8 k	
LIN pin with 220 pF capacitor	V _{ESD6-2}	±10 k	
VSUP (10 µF to ground)	V _{ESD6-3}	±12 k	
WAKE (2*18 kΩ serial resistor)	V _{ESD6-4}	±15 k	

THERMAL RATINGS

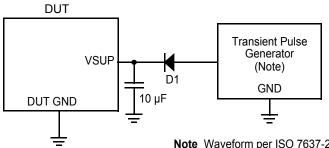
Operating Temperature			°C
Ambient Junction	T _A T _J	-40 to 125 -40 to 150	
Storage Temperature	T _{STG}	-40 to 150	°C
Thermal Resistance, Junction to Ambient	R _{θJA}	150	°C/W
Peak Package Reflow Temperature During Solder Mounting $^{(3)}$	T _{SOLDER}	240	°C
Thermal Shutdown Temperature	T _{SHUT}	150 to 200	°C
Thermal Shutdown Hysteresis Temperature	T _{HYST}	20	°C

Notes

3. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

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Test Pulse	V _S [V]	Pulse repetition frequency [Hz] (1/T ₁)	Test Duration [min]	R _i [Ω]	Remarks
1	-100	2		10	t ₂ = 0 s
2a	+75	2	1 for function test	2	
3a	-150	10000	10 for damage test	50	
3b	+100	10000		50	



Note Waveform per ISO 7637-2. Test Pulses 1, 2a, 3a, 3b.



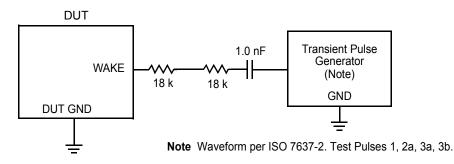


Figure 5. Test Circuit for Transient Test Pulses (WAKE)

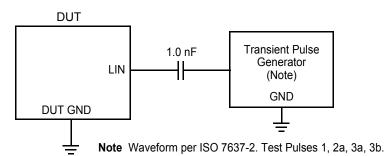


Figure 6. Test Circuit for Transient Test Pulses (LIN)

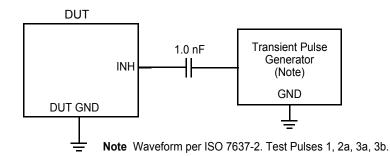


Figure 7. Test Circuit for Transient Test Pulses (INH)

STATIC ELECTRICAL CHARACTERISTICS

Table 5. Static Electrical Characteristics

Characteristics under conditions 7.0 V \leq V_{SUP} \leq 18 V, -40°C \leq T_A \leq 125°C, GND = 0 V, unless otherwise noted. Typical values reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Тур	Max	Unit
/SUP PIN (DEVICE POWER SUPPLY)					
Nominal Operating Voltage	V _{SUP}	7.0	13.5	18.0	V
Functional Operating Voltage ⁽⁴⁾	V _{SUPOP}	6.7	_	27	V
Load Dump	V _{SUPLD}	_	_	40	V
Power-On Reset (POR) Threshold	V _{POR}				V
V _{SUP} Ramp Down and INH goes High to Low		3.5	-	5.3	
Power-On Reset (POR) Hysteresis	V _{PORHYST}	_	270	-	mV
V _{SUP} Under-voltage Threshold (positive and negative)	V _{UVL} , V _{UVH}				V
Transmission disabled and LIN bus goes in recessive state		5.8	-	6.7	
V _{SUP} Under-voltage Hysteresis (V _{UVL} - V _{UVH})	V _{UVHYST}	-	130	-	mV
Supply Current in Sleep Mode					μA
$V_{SUP} \le 13.5 \text{ V}$, Recessive State	I _{S1}	_	6.0	11	
13.5 V < V _{SUP} < 27 V	I _{S2}	—	—	20	
$V_{SUP} \leq 13.5$ V, Shorted to GND	I _{S3}	—	24	70	
Supply Current in Normal or Slow or Fast Mode					mA
Bus Recessive, Excluding INH Output Current	I _{S(REC)}	_	4.0	6.0	
Bus Dominant, Excluding INH Output Current	I _{S(DOM)}	_	6.0	8.0	
RXD OUTPUT PIN (LOGIC)					•
Low Level Output Voltage	V _{OL}				V
$I_{IN} \le 1.5 \text{ mA}$		0	—	0.9	
High Level Output Voltage	V _{OH}				V
V_{EN} = 5.0 V, I _{OUT} \leq 250 μ A		4.25	—	5.25	
V_{EN} = 3.3 V, $I_{OUT} \le 250 \ \mu A$		3.0	—	3.5	
TXD INPUT PIN (LOGIC)			1		
Low Level Input Voltage	V _{IL}	_	_	0.8	V
High Level Input Voltage	V _{IH}	2.0	_	_	V
Input Threshold Voltage Hysteresis	V _{INHYST}	100	300	600	mV
Pull-up Current Source	I _{PU}				μA
V _{EN} = 5.0 V, 1.0 V < V _{TXD} < 3.5 V		-60	-35	-20	
IN INPUT PIN (LOGIC)				1	1
Low Level Input Voltage	V _{IL}	_	_	0.8	V
High Level Input Voltage	V _{IH}	2.0	_	_	V
Input Voltage Threshold Hysteresis	V _{INHYST}	100	400	600	mV
Pull-down Resistor	R _{PD}	100	230	350	kohm
4 For the functional operating voltage, the device is functional at					

4. For the functional operating voltage, the device is functional and all features are operating. The electrical parameters are noted under conditions 7.0 V \leq V_{SUP} \leq 18 V, -40°C \leq T_A \leq 125° C, GND = 0 V.

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Table 5. Static Electrical Characteristics (continued)

Characteristics under conditions 7.0 V \leq V_{SUP} \leq 18 V, -40°C \leq T_A \leq 125°C, GND = 0 V, unless otherwise noted. Typical values reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Тур	Max	Unit
LIN PHYSICAL LAYER - TRANSCEIVER LIN ⁽⁵⁾					
Operating Voltage Range ⁽⁶⁾	V _{BAT}	8.0	_	18	V
Supply Voltage Range	V _{SUP}	7.0	_	18	V
Voltage Range (within which the device is not destroyed)	V _{SUP_NON_OP}	-0.3	_	40	V
Current Limitation for Driver Dominant State Driver ON, V _{BUS} = 18 V	I _{BUS_LIM}	40	90	200	mA
Input Leakage Current at the Receiver Driver off; V _{BUS} = 0 V; V _{BAT} = 12 V	I _{BUS_PAS_DOM}	-1.0	_	_	mA
Leakage Output Current to GND Driver Off; 8.0 V < V _{BAT} < 18 V; 8.0 V < V _{BUS} < 18 V; V _{BUS} \ge V _{BUS} \ge V _{BUS}	IBUS_PAS_REC	-	_	20	μA
Control Unit Disconnected from Ground ⁽⁷⁾ GND _{DEVICE} = V _{SUP} ; V _{BAT} = 12 V; 0 < V _{BUS} < 18 V	I _{BUS_NO_GND}	-1.0	_	1.0	mA
V_{BAT} Disconnected; $V_{SUP_{DEVICE}}$ = GND; 0 V < V_{BUS} < 18 V ⁽⁸⁾	I _{BUSNO_BAT}	-	-	10	μA
Receiver Dominant State ⁽⁹⁾	V _{BUSDOM}	_	_	0.4	V _{SUP}
Receiver Recessive State ⁽¹⁰⁾	V _{BUSREC}	0.6	-	-	V _{SUP}
Receiver Threshold Center (V _{TH_DOM} + V _{TH_REC})/2	V _{BUS_CNT}	0.475	0.5	0.525	V _{SUP}
Receiver Threshold Hysteresis (V _{TH_REC} - V _{TH_DOM})	V _{HYS}	_	_	0.175	V _{SUP}
LIN dominant level with 500 $\Omega,$ 680 Ω and 1.0 k\Omega load on the LIN bus	V _{LINDOM_LEVEL}	_	_	0.3	V _{SUP}
V _{BAT} _SHIFT	V _{SHIFT_BAT}	0	_	11.5%	V _{BAT}
GND_SHIFT	V _{SHIFT_GND}	0	_	11.5%	V _{BAT}
LIN Wake-up Threshold from Sleep Mode	V _{BUSWU}	_	4.3	5.0	V
LIN Pull-up Resistor to V _{SUP}	R _{SLAVE}	20	30	60	kΩ
LIN Internal Capacitor ⁽¹¹⁾	C _{LIN}			30	pF
Over-temperature Shutdown ⁽¹²⁾	T _{LINSD}	150	160	200	°C
Over-temperature Shutdown Hysteresis	T _{LINSD_HYS}	_	20	-	°C

Notes

- 5. Parameters guaranteed for 7.0 V \leq V_{SUP} \leq 18 V.
- 6. Voltage range at the battery level, including the reverse battery diode.
- 7. Loss of local ground must not affect communication in the residual network.
- 8. Node has to sustain the current that can flow under this condition. The bus must remain operational under this condition.
- 9. LIN threshold for a dominant state.
- 10. LIN threshold for a recessive state.
- 11. This parameter is guaranteed by process monitoring but not production tested.
- 12. When an over-temperature shutdown occurs, the LIN transmitter and receiver are in recessive state and INH switched off. This parameter is tested with a test mode on ATE and characterized at laboratory.

Table 5. Static Electrical Characteristics (continued)

Characteristics under conditions 7.0 V \leq V_{SUP} \leq 18 V, -40°C \leq T_A \leq 125°C, GND = 0 V, unless otherwise noted. Typical values reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Тур	Max	Unit
INH OUTPUT PIN					
Driver ON Resistance (Normal Mode)	INH _{ON}				Ω
I _{INH} = 50 mA		_	_	50	
Current load capability	I _{INH_LOAD}				mA
From 7.0 V < V _{SUP} < 18 V		—	—	30	
Leakage Current (Sleep Mode)	I _{LEAK}				μA
0 < V _{INH} < V _{SUP}		-5.0	_	5.0	
Over-temperature Shutdown ⁽¹³⁾	T _{INHSD}	150	160	200	°C
Over-temperature Shutdown Hysteresis	T _{INHSD_HYS}	_	20	—	°C
WAKE INPUT PIN					
High to Low Detection Threshold (5.5 V < V_{SUP} < 7 V)	V _{WUHL1}	2.0	—	3.9	V
Low to High Detection Threshold (5.5 V < V_{SUP} < 7 V)	V _{WULH1}	2.4	—	4.3	V
Hysteresis (5.5 V < V _{SUP} < 7 V)	V _{WUHYS1}	0.2	_	0.8	V
High to Low Detection Threshold (7 V \leq V_{SUP} < 27 V)	V _{WUHL2}	2.4	_	3.9	V
Low to High Detection Threshold (7 V \leq V_{SUP} < 27 V)	V _{WULH2}	2.9	_	4.3	V
Hysteresis (7 V \leq V _{SUP} < 27 V)	V _{WUHYS2}	0.2	_	0.8	V
Wake-up Input Current (V _{WAKE} < 27 V)	I _{WU}	_	_	5.0	μA

Notes

13. When an over-temperature shutdown occurs, the INH high side is switched off and the LIN transmitter and receiver are in recessive state. This parameter is tested with a test mode on ATE and characterized at laboratory.

DYNAMIC ELECTRICAL CHARACTERISTIC

Table 6. Dynamic Electrical Characteristics

Characteristics under conditions 7.0 V \leq V_{SUP} \leq 18 V, -40°C \leq T_A \leq 125°C, GND = 0 V, unless otherwise noted. Typical values reflect the approximate parameter means at $T_A = 25^{\circ}C$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Тур	Max	Unit

LIN PHYSICAL LAYER DRIVER CHARACTERISTICS FOR NORMAL SLEW RATE - 20.0 KBIT/SEC ACCORDING TO LIN PHYSICAL LAYER SPECIFICATION^{(14), (15)} 33662L AND 33662S DEVICES

Duty Cycle 1:	D1				
$TH_{REC(MAX)} = 0.744 * V_{SUP}$					
TH _{DOM(MAX)} = 0.581 * V _{SUP}					%
D1 = $t_{BUS_REC(MIN)}/(2 \text{ x } t_{BIT})$, t_{BIT} = 50 µs, 7.0 V \leq V $_{SUP} \leq$ 18 V		0.396	—	—	
Duty Cycle 2:	D2				
TH _{REC(MIN)} = 0.422 * V _{SUP}					
TH _{DOM(MIN)} = 0.284 * V _{SUP}					
D2 = $t_{BUS_REC(MAX)}/(2 \text{ x } t_{BIT})$, t_{BIT} = 50 µs, 7.6 V \leq V $_{SUP} \leq$ 18 V		—	—	0.581	

LIN PHYSICAL LAYER DRIVER CHARACTERISTICS FOR SLOW SLEW RATE - 10.4 KBIT/SEC ACCORDING TO LIN PHYSICAL LAYER SPECIFICATION^{(14), (16)} 33662J DEVICE

Duty Cycle 3:	D3				
$TH_{REC(MAX)} = 0.778 * V_{SUP}$					
TH _{DOM(MAX)} = 0.616 * V _{SUP}					%
D3 = t_{BUS_REC(MIN)}/(2 x t_{BIT}), t_{BIT} = 96 $\mu s, 7.0 \ V \leq V_{SUP} \leq$ 18 V		0.417	—	—	
Duty Cycle 4:	D4				
TH _{REC(MIN)} = 0.389 * V _{SUP}					
TH _{DOM(MIN)} = 0.251 * V _{SUP}					
D4 = t_{BUS_REC(MAX)}/(2 x t_{BIT}), t_{BIT} = 96 $\mu s, 7.6 \; V \leq V_{SUP} \leq$ 18 V		—	—	0.590	
LIN PHYSICAL LAYER DRIVER CHARACTERISTICS FOR FAST SLEW RATE					
Fast Bit Rate (Programming Mode)	BR _{FAST}	_	_	100	kBit/s
LIN PHYSICAL LAYER TRANSMITTER CHARACTERISTICS FOR NORMAL SLEW RATE - 20.0 KBIT/SEC ⁽¹ 33662S DEVICE	7)				
Symmetry of Transmitter delay ⁽¹⁸⁾					μS
t _{TRAN_SYM} = MAX (t _{TRAN_SYM60%} , t _{TRAN_SYM40%})	t _{TRAN_SYM}	-7.25	—	7.25	
t _{tran_sym60%} = t _{tran_pdf60% -} t _{tran_pdr60%}					
t _{TRAN_SYM40%} = t _{TRAN_PDF40%} - t _{TRAN_PDR40%}					
LIN PHYSICAL LAYER RECEIVER CHARACTERISTICS ACCORDING LIN2.1 ⁽¹⁷⁾ 33662L AND 33662J AND 33662S DEVICES					
Propagation Delay and Symmetry ⁽¹⁹⁾					μS
Propagation Delay of Receiver, t _{REC_PD} = MAX (t _{REC_PDR} , t _{REC_PDF})	t _{REC_PD}	—	—	6.0	
Symmetry of Receiver Propagation Delay, t _{REC_PDF} - t _{REC_PDR}	t _{REC_SYM}	-2.0	—	2.0	

Table 6. Dynamic Electrical Characteristics (continued)

Characteristics under conditions 7.0 V \leq V_{SUP} \leq 18 V, -40°C \leq T_A \leq 125°C, GND = 0 V, unless otherwise noted. Typical values reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Тур	Max	Unit
Notes					

Bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 8.

15. See Figure 9.

16. See Figure 10.

V_{SUP} from 7.0 to 18 V, bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 8.

18. See Figure 11

19. See Figure 12.

Table 6. Dynamic Electrical Characteristics (continued)

Characteristics under conditions 7.0 V \leq V_{SUP} \leq 18 V, -40°C \leq T_A \leq 125°C, GND = 0 V, unless otherwise noted. Typical values reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Тур	Max	Unit
LIN PHYSICAL LAYER RECEIVER CHARACTERISTICS WITH TIGHTEN LIMITS ⁽²⁰⁾ 33662S DEVICE					
Propagation Delay and Symmetry ⁽²¹⁾					μS
Propagation Delay of Receiver, t _{REC_PD} = MAX (t _{REC_PDR} , t _{REC_PDF})	t _{REC_PD_S}	_	—	5.0	
Symmetry of Receiver Propagation Delay, t _{REC_PDF} - t _{REC_PDR}	t _{REC_SYM_S}	-1.3	—	1.3	
LIN PHYSICAL LAYER RECEIVER CHARACTERISTICS - LIN SLOPE 1.0 V/ns ⁽²⁰⁾ 33662S DEVICE	· · · · · ·				
Propagation Delay and Symmetry ⁽²²⁾					μS
Propagation Delay of Receiver, t _{REC_PD_FAST} = MAX (t _{REC_PDR_FAST} ,	t _{REC_PD_FAST}	_	_	6.0	
t _{REC_PDF_FAST})					
Symmetry of Receiver Propagation Delay, $t_{REC_PDF_FAST} - t_{REC_PDR_FAST}$	t _{REC_SYM_FAST}	-1.3	—	1.3	
SLEEP MODE AND WAKE-UP TIMINGS					
Sleep Mode Delay Time ⁽²³⁾	t _{SD}				μs
after EN High to Low to INH High to Low with 100 μA load on INH		50	—	91	
NAKE-UP TIMINGS					•
Bus Wake-up Deglitcher (Sleep Mode) (24)	t _{WUF}	40	70	100	μS
EN Wake-up Deglitcher ⁽²⁵⁾	t _{LWUE}				μS
EN High to INH Low to High		_	—	15	
Wake-up Deglitcher ⁽²⁶⁾	t _{WF}				μs
Wake state change to INH Low to High		10	48	70	
FXD TIMING					
TXD Permanent Dominant State Delay ⁽²⁷⁾	t _{TXDDOM}	3.75	5.0	6.25	ms
FIRST DOMINANT BIT VALIDATION	• • • • • •		•	•	
First dominate bit validation delay when device in Normal Mode ⁽²⁸⁾	t _{FIRST_DOM}	_	50	80	μs
FAST BAUD RATE TIMING			1		1
EN Low Pulse Duration to Enter in Fast Baud Rate using Toggle Function ⁽²⁹⁾	t ₁				μS
EN High to Low and Low to High		—	—	45	
TXD Low Pulse Duration to Enter in Fast Baud Rate using Toggle Function ⁽²⁹⁾	t ₂	12.5	—	—	μs
Delay Between EN Falling Edge and TXD Falling Edge to Enter in Fast Baud Rate Using Toggle Function $^{\rm (29)}$	t ₃	12.5	_	_	μs
Delay Between TXD Rising Edge and EN Rising Edge to Enter in Fast Baud Rate Using Toggle Function ⁽²⁹⁾	t ₄	12.5	_	_	μs
RXD Low Level duration after EN rising edge to validate the Fast Baud Rate entrance ⁽²⁹⁾	t ₅	1.875		6.25	μs

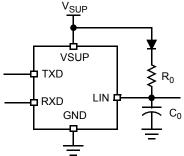
Table 6. Dynamic Electrical Characteristics (continued)

Characteristics under conditions 7.0 V \leq V_{SUP} \leq 18 V, -40°C \leq T_A \leq 125°C, GND = 0 V, unless otherwise noted. Typical values reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Тур	Max	Unit
Notes					

- V_{SUP} from 7.0 to 18 V, bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 8.
- 21. See Figure 12
- 22. See Figure 13
- 23. See Figure 25 and 26
- 24. See Figure 16, 19, and Figure 20
- 25. See Figure 14, 17, Figure 21, Figure 25 and Figure 26
- 26. See Figure 15, 18, Figure 25 and Figure 26
- 27. The LIN is in recessive state and the receiver is still active.
- 28. See Figure 14, 17, 15, 18, 16, 19 and Figure 24
- 29. See Figure 22 and 23

TIMING DIAGRAMS



Note R₀ and C₀: 1.0 k Ω /1.0 nF, 660 Ω /6.8 nF, and 500 Ω /10 nF.

Figure 8. Test Circuit for Timing Measurements

ELECTRICAL CHARACTERISTICS TIMING DIAGRAMS

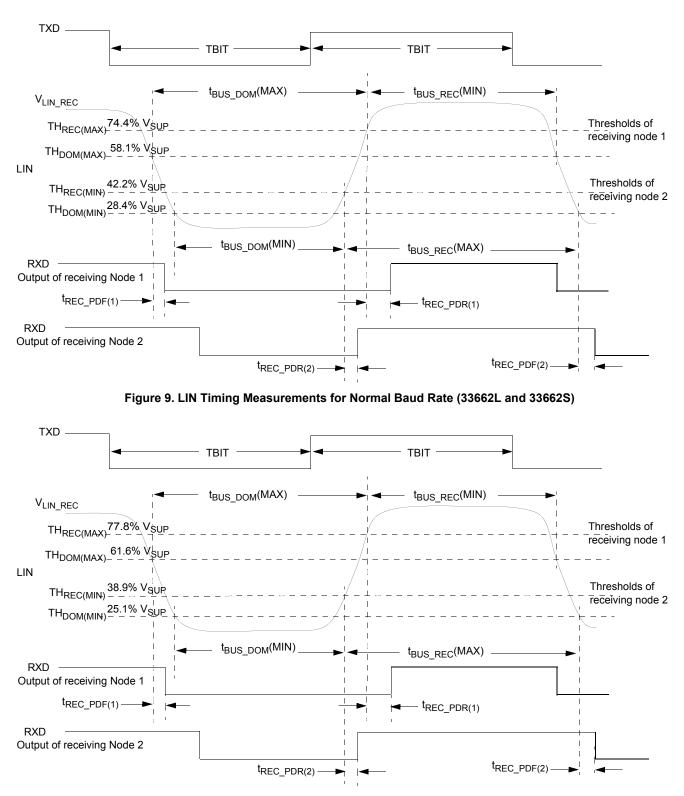
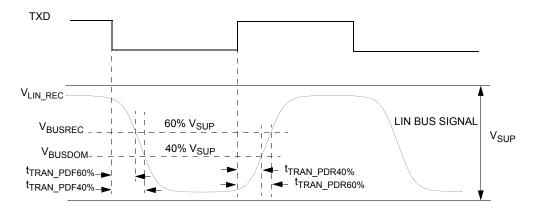


Figure 10. LIN Timing Measurements for Slow Baud Rate (33662J)

33662





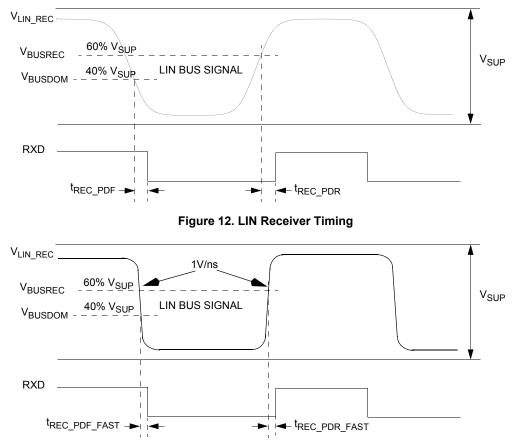


Figure 13. LIN Receiver Timing LIN slope 1V/ns

FUNCTIONAL DIAGRAMS

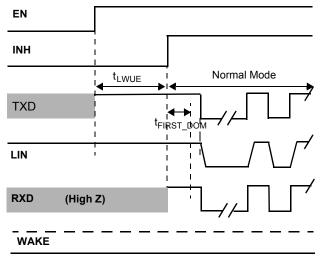
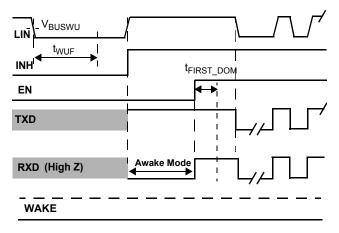


Figure 14. EN Pin Wake-up with TXD High





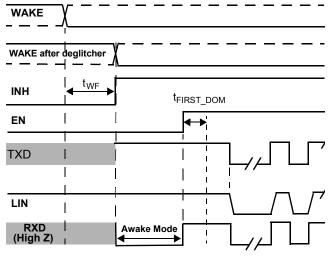


Figure 15. WAKE Pin Wake-up with TXD High

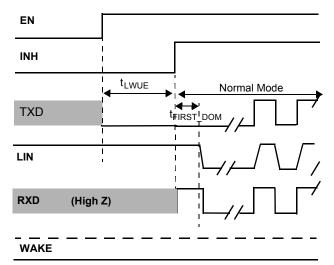
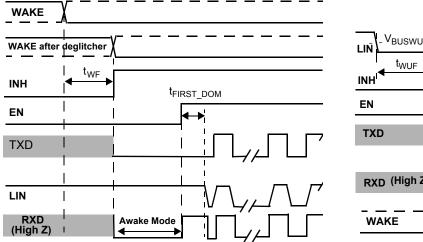


Figure 17. EN Pin Wake-up with TXD Low



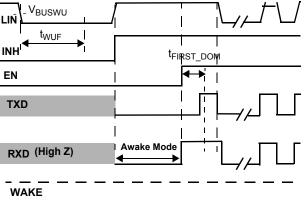


Figure 18. WAKE Pin Wake-up with TXD Low

Figure 19. LIN Bus Wake-up with TXD Low

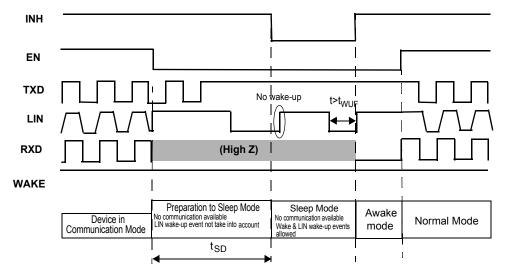
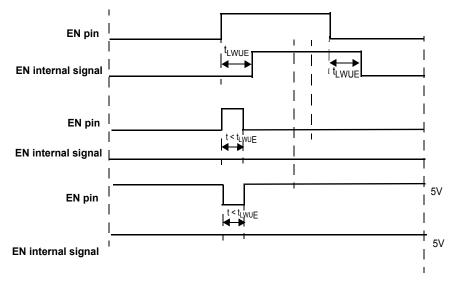
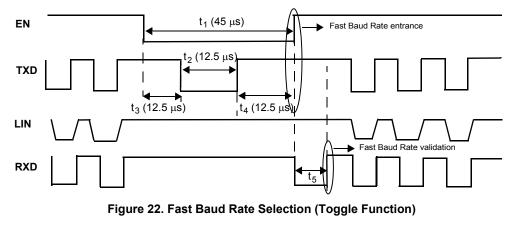


Figure 20. LIN Bus Wake-up with LIN bus in Dominant During the Preparation to Sleep Mode

ELECTRICAL CHARACTERISTICS FUNCTIONAL DIAGRAMS







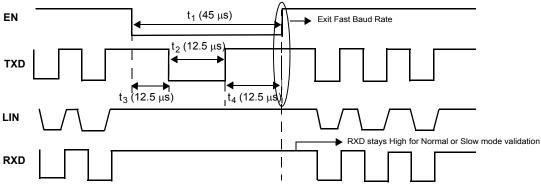


Figure 23. Fast Baud Rate Mode Exit (back to Normal or Slow slew rate)



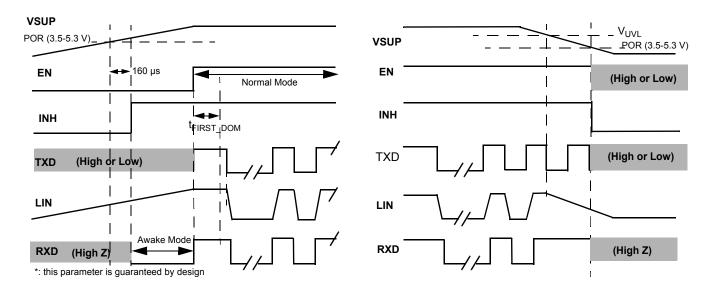


Figure 24. Power Up and Down Sequences

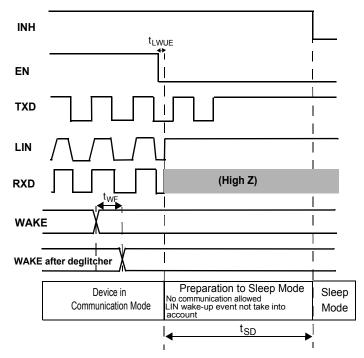
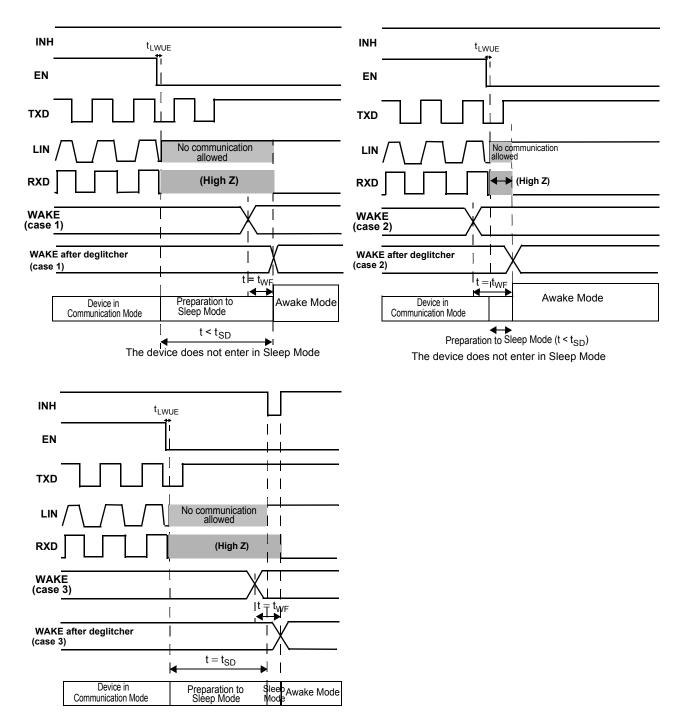
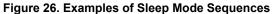


Figure 25. Sleep Mode Sequence

ELECTRICAL CHARACTERISTICS FUNCTIONAL DIAGRAMS





FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33662L, 33662J, and 33662S are a physical layer component dedicated to automotive LIN sub-bus applications.

The 33662L and 33662S features include a 20 kbps baud rate and the 33662J a 10 kbps baud rate. They integrate fast baud rate for test and programming modes, excellent ESD robustness, immunity against disturbance, and radiated emission performance. They have safe behavior in case of a

LIN bus short-to-ground, or a LIN bus leakage during low power mode.

Digital inputs are 5.0 and 3.3 V compatible without any external required components.

The INH output can be used to control an external voltage regulator, or to drive a LIN bus pull-up resistor.

FUNCTIONAL PIN DESCRIPTION

POWER SUPPLY PIN (VSUP)

The VSUP supply pin is the power supply pin for the 33662L, or 33662J, or 33662S. In an application, the pin is connected to a battery through a serial diode, for reverse battery protection. The DC operating voltage is from 7.0 to 18 V. This pin can sustain a standard automotive load dump condition up to 40 V. To avoid a false bus message, an under-voltage on VSUP disables the transmission path (from TXD to LIN) when V_{SUP} falls below 6.7 V. Supply current in Sleep mode is typically 6.0 μ A.

GROUND PIN (GND)

In case of a ground disconnection at the module level, the 33662L, 33662J, and 33662S do not have significant current consumption on the LIN bus pin when in the recessive state.

LIN BUS PIN (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems, and is compliant to the LIN bus specification 1.3, 2.0, 2.1, and SAEJ2602-2.

The LIN interface is only active during Normal mode (See Figure 27).

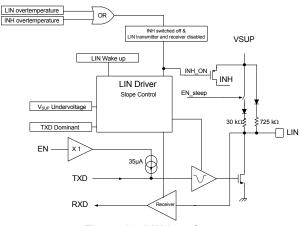


Figure 27. LIN Interface

Transmitter Characteristics

The LIN driver is a low side MOSFET with internal overcurrent thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated so no external pull-up components are required for the application in a slave node. An additional pull-up resistor of 1.0 k Ω must be added when the device is used in the master node.

The LIN pin exhibits no reverse current from the LIN bus line to V_{SUP}, even in the event of a GND shift or V_{SUP} disconnection. The 33662 is tested according to the application conditions (i.e. in normal mode and recessive state during communication).

The transmitter has a 20 kbps baud rate (Normal baud rate) for the 33662L and 33662S devices, or 10 kbps baud rate (Slow baud rate) for the 33662J device.

As soon as the device enters in Normal mode, the LIN transmitter will be able to send the first dominant bit only after the t_{FIRST_DOM} delay. t_{FIRST_DOM} delay has no impact on the receiver. The receiver will be enabled as soon as the device enters in Normal mode.

Receiver Characteristics

The receiver thresholds are ratiometric with the device supply pin.

If the V_{SUP} voltage goes below the V_{SUP} under-voltage threshold (V_{UVL}, V_{UVH}), the bus enters into a recessive state even if communication is sent to TXD.

In case of LIN thermal shutdown, the transceiver and receiver are in recessive and INH turned off. When the temperature is below the T_{LINSD} , INH and LIN will be automatically enabled.

The Fast Baud Rate selection is reported by the RXD pin. Fast Baud Rate is activated by the toggle function (See Figure 22). At the end of the toggle function, just after EN rising edge, RXD pin is kept low for t_5 to flag the Fast Baud Rate entry (See Figure 22).

To exit the Fast Baud Rate and return in Normal or Slow baud rate, a toggle function is needed. At the end of the toggle function, the RXD pin stays high to signal Fast Baud Rate exit (See <u>Figure 23</u>). The device enters into Fast Baud Rate at room and hot temperature.

DATA INPUT PIN (TXD)

The TXD input pin is the MCU interface to control the state of the LIN output. When TXD is LOW (dominant), LIN output is LOW; when TXD is HIGH (recessive), the LIN output transistor is turned OFF. TXD pin thresholds are 3.3 V and 5.0 V compatible.

This pin has an internal pull-up current source to force the recessive state if the input pin is left floating.

If the pin stays low (dominant sate) more than 5.0 ms (typical value), the LIN transmitter goes automatically into recessive state.

DATA OUTPUT PIN (RXD)

RXD output pin is the MCU interface, which reports the state of the LIN bus voltage.

In Normal or Slow baud rate, LIN HIGH (recessive) is reported by a high voltage on RXD; LIN LOW (dominant) is reported by a low voltage on RXD.

The RXD output structure is a tristate output buffer (See Figure 28).

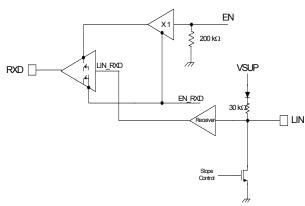


Figure 28. RXD Interface

The RXD output pin is the receiver output of the LIN interface. The low level is fixed. The high level is dependent on EN voltage. If EN is set at 3.3 V, RXD V_{OH} is 3.3 V. If EN is set at 5.0 V, RXD V_{OH} is 5.0 V.

In Sleep mode, RXD is high-impedance. When a wake-up event is recognized from the WAKE pin or from the LIN bus pin, RXD is pulled LOW to report the wake-up event. An external pull-up resistor may be needed.

ENABLE INPUT PIN (EN)

EN input pin controls the operation mode of the interface. If EN = 1, the interface is in Normal mode, TXD to LIN after t_{FIRST_DOM} delay and LIN to RXD paths are both active. EN pin thresholds are 3.3 V and 5.0 V compatible. RXD V_{OH}

level follows EN pin high level. The device enters the Sleep mode by setting EN LOW for a delay higher than t_{SD} (70 µs typ. value) and if the WAKE pin state doesn't change during this delay (see Figure 25).

A combination of the logic levels on the EN and TXD pins allows the device to enter into the Fast Baud Rate mode of operation (see Figure 22).

INHIBIT OUTPUT PIN (INH)

The INH output pin is connected to an internal high side power MOSFET. The pin has two possible main functions. It can be used to control an external switchable voltage regulator having an inhibit input. It can also be used to drive the LIN bus external resistor in the master node application, thanks to its high drive capability. This is illustrated in <u>Figure 30</u> and <u>31</u>.

In Sleep mode, INH is turned OFF. If a voltage regulator inhibit input is connected to INH, the regulator will be disabled. If the master node pull-up resistor is connected to INH, the pull-up resistor will be unpowered and left floating.

In case of a INH thermal shutdown, the high side is turned off and the LIN transmitter and receiver are in recessive state.

An external 10 to 100 pF capacitor on INH pin is advised in order to improve EMC performances.

WAKE INPUT PIN (WAKE)

The WAKE pin is a high voltage input used to wake-up the device from the Sleep mode. WAKE is usually connected to an external switch in the application.

The WAKE pin has a special design structure and allows wake-up from both HIGH to LOW or LOW to HIGH transitions. When entering into Sleep mode, the device monitors the state of the WAKE pin and stores it as a reference state. The opposite state of this reference state will be the wake-up event used by the device to enter again into Normal mode.

If the Wake pin state changes during the Sleep mode Delay Time (t_{SD}) or before EN goes low with a deglitcher lower than t_{WF} , the device will not enter the Sleep mode, but will go into Awake mode (See Figure 26).

An internal filter is implemented to avoid a false wake-up event due to parasitic pulses (See Figure 15 and 18). WAKE pin input structure exhibits a high-impedance, with extremely low input current when voltage at this pin is below 27 V. Two serial resistors should be inserted in order to limit the input current mainly during transient pulses and ESD. The total recommended resistor value is 33 k Ω . An external 10 to 100 nF capacitor is advised for better EMC and ESD performances.

Important The WAKE pin should *not* be left open. If the wake-up function is not used, WAKE should be connected to ground to avoid a false wake-up.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

As described below and depicted in Figure 29 and Table 7, the 33662L, 33662J, and 33662S have two operational modes, Normal and Sleep. In addition, there are two transitional modes: Awake mode and Preparation to Sleep mode. The Awake mode allows the device to go into Normal mode. The Preparation to Sleep mode allows the device to go into Sleep mode.

NORMAL OR SLOW BAUD RATE

In the Normal mode, the LIN bus can transmit and receive information.

The 33662L and 33662S (20 kbps) have a slew rate and timing compatible with Normal Baud Rate and LIN protocol specification 1.3, 2.0, and 2.1.

The 33662J (10 kbps) has a slew rate and timing compatible with Low Baud Rate.

From Normal mode, the three devices can enter into Fast Baud Rate (Toggle function).

FAST BAUD RATE

In Fast Baud Rate, the slew rate is around 10 times faster than the Normal Baud Rate. This allows very fast data transmission (>100 kbps) -- for instance, for electronic control unit (ECU) tests and microcontroller program download. The bus pull-up resistor might be adjusted to ensure a correct RC time constant in line with the high baud rate used.

Fast Baud Rate is entered via a special sequence (called toggle function) as follows:

1- EN pin set LOW while TXD is HIGH

- 2- TXD stays HIGH for 12.5 µs min
- 3- TXD set LOW for 12.5 µs min
- 4- TXD pulled HIGH for 12.5 µs min
- 5- EN pin set LOW to HIGH while TXD still HIGH

The device enters into the Fast Baud Rate if the delay between Step 1 to Step 5 is 45 µs maximum. The toggle function is described in Figures 22. Once in Fast Baud Rate, the same toggle function just described previously is used to bring the device back into Normal Baud Rate.

Fast Baud Rate selection is reported to the MCU by RXD pin. Once the device enters in this Fast Baud Rate, the RXD pin goes at low level for t_5 . When the device returns in Normal Baud Rate with the same toggle function, the RXD pin stays high. Both sequences are illustrated in <u>Figures 22</u> and <u>23</u>.

PREPARATION TO SLEEP MODE

To enter the Preparation to Sleep mode, EN must be low for a delay higher than $t_{\mbox{LWUE}}.$

If the WAKE pin state doesn't change during t_{SD} and t_{LWUE} then the 33662 goes into Sleep mode.

If the WAKE pin state changes during t_{SD} and if t_{WF} is reached after end of t_{SD} then the device goes into Sleep mode after the end of t_{SD} timing.

If the WAKE pin state changes during t_{SD} and t_{WF} delay has been reached before the end of t_{SD} then the device goes into Awake mode.

If the WAKE pin state changes before t_{SD} and the delay t_{WF} ends during t_{SD} then the device goes into Awake mode.

If EN goes high for a delay higher than $\rm t_{LWUE},$ the 33662 returns to Normal mode.

SLEEP MODE

To enter into Sleep mode, EN must be low for a delay longer than t_{SD} and the Wake pin must stay in the same state (High or Low) during this delay.

The device conditions to not enter in Sleep mode but enter in Awake mode are detailed in the Preparation into Sleep mode chapter. See <u>Figure 26</u>.

In Sleep mode, the transmission path is disabled and the device is in Low Power mode. Supply current from V_{SUP} is very low (6.0 µA typical value). Wake-up can occur from LIN bus activity, from the EN pin and from the WAKE input pin. If during the preparation to Sleep mode delay (t_{SD}), the LIN bus goes low due to LIN network communication, the device still enters into the Sleep mode. The device can be awakened by a recessive to dominant start, followed by a dominant to recessive state after t > t_{WUF} .

After a Wake-up event, the device enters into Awake mode.

In the Sleep mode, the internal 725 kOhm pull-up resistor is connected and the 30 kOhm is disconnected.

DEVICE POWER-UP (Awake Transitional Mode)

At power-up (V_{SUP} rises from zero), when V_{SUP} is above the Power On Reset voltage, the device automatically switches after a 160 µs delay time to the Awake transitional mode. It switches the INH pin to a HIGH state and RXD to a LOW state. See Figure 24.

DEVICE WAKE-UP EVENTS

The 33662L, 33662J, and 33662S can be awakened from Sleep mode by three wake-up events:

- Remote wake-up via LIN bus activity
- Via the EN pin
- · Toggling the WAKE pin

Remote Wake from LIN Bus (Awake Transitional Mode)

The device is awakened by a LIN dominant pulse longer than t_{WUF} . Dominant pulse means: a recessive to dominant transition, wait for t > t_{WUF} , then a dominant to recessive

FUNCTIONAL DEVICE OPERATION OPERATIONAL MODES

transition. This is illustrated in <u>Figure 16</u> and <u>19</u>. Once the wake-up is detected (during the dominant to recessive transition), the device enters into Awake mode, with INH HIGH and RXD pulled LOW.

Once in the Awake mode, the EN pin has to be set to 3.3 V or 5.0 V (depending on the system) to enter into Normal mode. Once in Normal mode, the device has to wait t_{first_dom} delay before transmitting the first dominant bit.

Wake-up from EN pin

The device can be waked-up by a LOW to HIGH transition of the EN pin. When EN is switched from LOW to HIGH and stays HIGH for a delay higher than t_{LWUE} , the device is awakened and enters into Normal mode. See Figure 14 and

FAIL-SAFE FEATURES

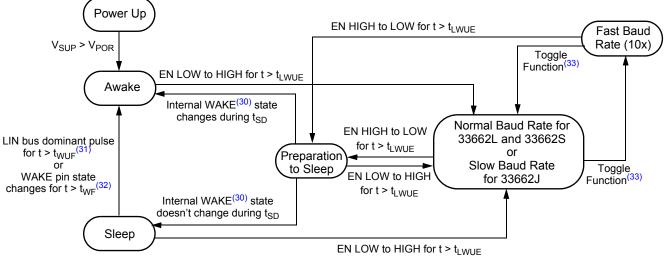
The table below describes the 33662 protections.

 $\underline{17}$. Once in Normal mode, the device has to wait t_{FIRST_DOM} delay before transmitting the first dominant bit.

Wake-up from WAKE Pin (Awake Transitional Mode)

Just before entering the Sleep mode, the WAKE pin state is stored. A change in the level longer than the deglitcher time (70 μ s maximum) will generate a wake-up, and the device enters into the Awake Transitional mode, with INH HIGH and RXD pulled LOW. See <u>Figure 15</u> and <u>18</u>. The device goes into Normal mode when EN is switched from LOW to HIGH and stays HIGH for a delay higher than t_{LWUE}. Once in Normal mode, the device has to wait t_{FIRST_DOM} delay before transmitting the first dominant bit.

BLOCK	FAULT	FUNCTIONAL MODE	CONDITION	RESPONSE	RECOVERY CONDITION	RECOVERY FUNCTIONALITY MODE
Power Supply	Power on Reset (POR)	All modes	V _{SUP} < 3.5 V (min) then power up	No internal supplies	Condition gone	Device goes in Awake mode whatever the previous device mode
INH	INH Thermal Shutdown	Normal, Awake & Preparation to Sleep modes	Temperature > 160 °C (typ)	INH high side turned off. LIN transmitter and receiver in recessive state	Condition gone	Device returns in same functional mode
	V _{SUP} under-voltage	Normal	V _{SUP} < V _{UVL}	LIN transmitter in recessive state	Condition gone	Device returns in same functional mode
	TXD Pin Permanent Dominant	Normai	TXD pin low for more than 5.0 ms (typ)	LIN transmitter in recessive state	Condition gone	Device returns in same functional mode
LIN	LIN Thermal Shutdown	Normal mode	Temperature > 160 °C (typ)	LIN transmitter and receiver in recessive state INH high side turned off	Condition gone	Device returns in same functional mode



Notes

- 30. Internal WAKE is the WAKE signal filtered by t_{WF} (WAKE deglitcher)
- 31. See Figure 15 and Figure 18
- 32. See figures Figure 14 and Figure 17
- 33. The Toggle Function is guaranteed at ambient and hot temperature

Figure 29. Operational and Transitional Modes State Diagram

Table 7. Explanation of Operational and Transitional Modes State Diagram
--

Operational/ Transitional	LIN	INH	EN	ТХД	RXD
	Recessive state, driver off with 725 k Ω pull-up	OFF (low)	LOW	X	High-impedance. HIGH if external pull-up to V _{DD}
Awake	Recessive state, driver off. 725 k Ω pull-up active	ON (high)	LOW	Х	LOW. If external pull-up, HIGH-to-LOW transition reports wake-up
Preparation to Sleep mode	Recessive state, driver off with 725 k Ω pull-up	ON (high)	LOW	X	High-impedance. HIGH if external pull-up to V _{DD}
Normal mode	Driver active. 30 kΩ pull-up active Normal Baud Rate for 33662L and 33662S Slow Baud Rate for 33662J Fast Baud Rate (> 100 kbps) for 33662L, 33662S, & 33662J	ON (high)	HIGH	LOW to drive LIN bus in dominant HIGH to drive LIN bus in recessive	Report LIN bus state: • Low LIN bus dominant • High LIN bus recessive

X = Don't care.

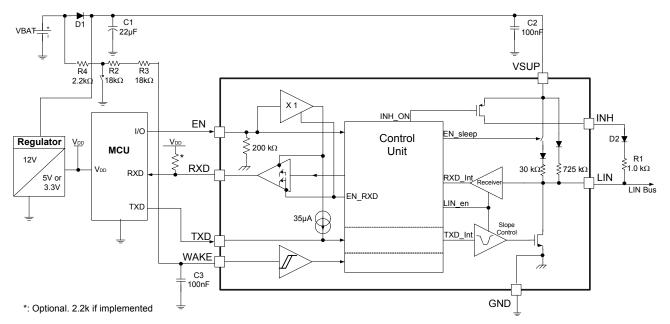
COMPATIBILITY WITH LIN1.3

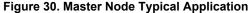
Following the Consortium LIN specification Package, Revision 2.1, November 24, 2006, Chapter 1.1.7.1 Compatibility with LIN1.3, page 15. The LIN 2.1 physical layer and is backward compatible with the LIN 1.3 physical layer, but not the other way around. The LIN 2.1 physical layer sets harder requirements, i.e. a node using the LIN 2.1 physical layer can operate in a LIN 1.3 cluster.

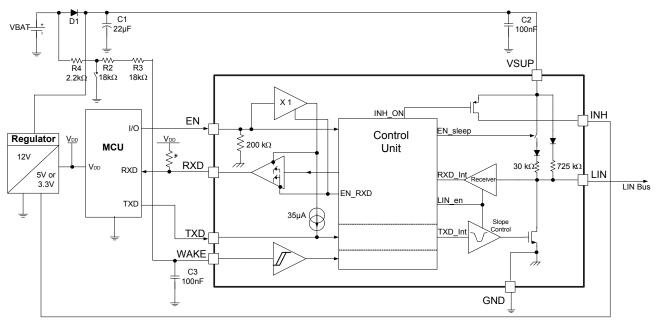
33662

TYPICAL APPLICATIONS

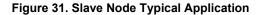
The 33662 can be configured for several applications. <u>Figure 30</u> and <u>31</u> show master and slave node applications. An additional pull-up resistor of 1.0 k Ω in series with a diode between the INH and LIN pins must be added when the device is used in the master node.







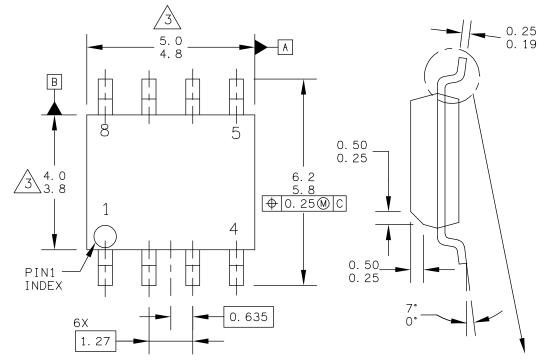
*: Optional. 2.2k if implemented

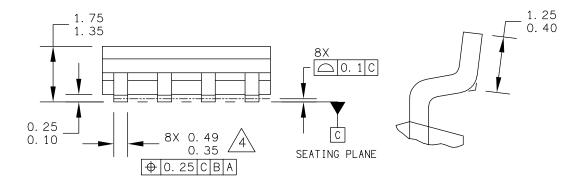


PACKAGING

PACKAGE DIMENSIONS

Important For the most current revision of the package, visit www.Freescale.com and do a keyword search on the 98A drawing number below.





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TITLE:		DOCUMENT NO): 98ASB42564B	REV: V
8LD SOIC NARROW	BODY	CASE NUMBER	8: 751–07	20 NOV 2007
		STANDARD: JE	DEC MS-012AA	

EF SUFFIX 8-PIN 98ASB42564B REVISION V



NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- A DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
- A DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

EF SUFFIX 8-PIN 98ASB42564B REVISION V

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES			
3.0	8/2011	Initial release			
4.0	9/2011	Changed the PC part numbers in the Ordering Information Table to MC			

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