



14-BIT FULL DUPLEX SERIALIZER/DESERIALIZER

FEATURES

- 10 MHz to 100 MHz Shift Clock Support
- 175 Mbytes/sec In TX/RX Modes
- Reduces Cable Size, Cost, and System EMI
- Bidirectional Data Communication
- Total Power < 360 mW Typ at 100-MHz Worst Case Pattern
- Power-Down Mode: < 500 μW Typ
- No External Components Required for PLL
- Inputs and Outputs Compatible with TIA/EIA-644 LVDS Standard
- ESD Rating > 5 kV (HBM)

- Integrated Termination Resistor
- Supports Spread Spectrum Clocking
- 64-Pin TQFP Package (PAG)

APPLICATIONS

- Flash Memory Cards
- Plain Paper Copiers
- Printers

DESCRIPTION

The SN75LVDT1422 Full Duplex Serializer/Deserializer incorporates a 14-bit serializer and a 14-bit deserializer. Operation of the serializer is independent of the operation of the deserializer. The 14-bit serializer accepts 14 TTL input lines and generates 2 LVDS high-speed serial streams plus one LVDS clock signal. The 14-bit deserializer accepts 3 LVDS input signals (2 high-speed serial streams and one LVDS clock signal) and drives out 14 TTL data signals plus one TTL clock.

The serializer loads 14 data bits into registers upon the rising or falling edge of the input clock signal (CLK IN). Rising or falling edge operation can be selected via the R/F select pin for the transmitter only. The frequency of CLK IN is multiplied seven times and then used to unload the data registers in 7-bit slices. The two high-speed serial streams and a phase-locked clock (TCLK±) are then output to LVDS output drivers. The frequency of TCLK± is the same as the input clock, CLK IN.

The deserializer accepts data on two high-speed LVDS data lines. High-speed data is received and loaded into registers at the rate seven times the LVDS input clock (RCLK±). The data is then unloaded to a 14-bit wide LVTTL parallel bus at the RCLK± rate. The SN75LVDT1422 presents valid data on the falling edge of the output clock (CLK OUT).

The SN75LVDT1422 provides three termination resistors for the differential LVDS inputs thus minimizing cost, and board space, while providing better overall signal integrity (SI). The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only user interventions are as follows:

Possible use of the TX ENABLE and RX ENABLE feature. Both the TX and RX ENABLE circuits are active-high inputs that independently enable the serializer and deserializer. When TX is disabled, the LVDS outputs go to high impedance. When RX is disabled, the TTL outputs go to a known low state.

The SN75LVDT1422 is characterized for operation over the free-air temperature range of -10°C to 70°C.



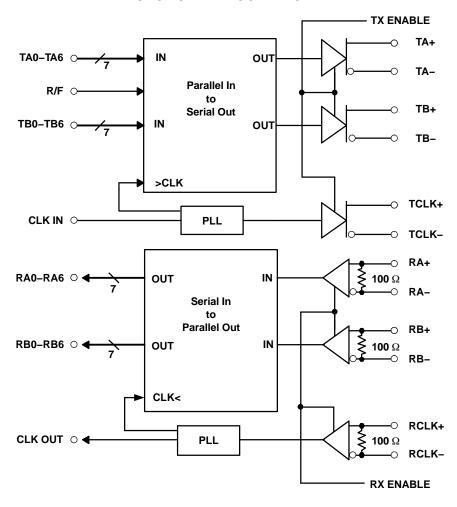
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



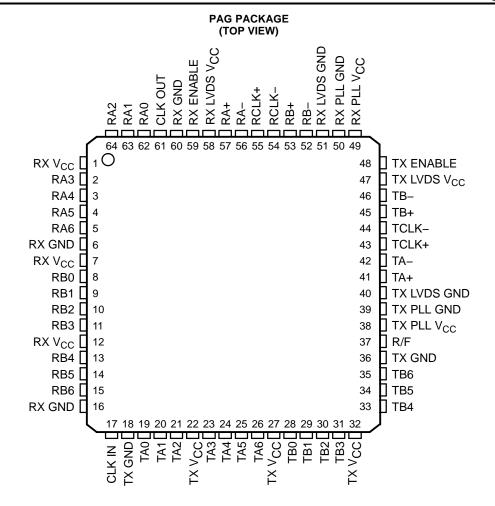


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM









TERMINAL FUNCTIONS

TERI	MINAL		
NAME	NO.	TYPE	DESCRIPTION
CLK IN	17	LVTTL Input	CMOS/LVTTL Clock input
CLK OUT	61	LVTTL Output	LVTTL Clock output
R/F	37	LVTTL Input	Input clock triggering edge select. High: Rising edge Low: Falling edge
RA+, RA-	57, 56	LVDS Input	LVDS Data inputs
RA[0:6]	62, 63, 64, 2, 3, 4, 5	LVTTL Output	Single-ended data outputs
RB+, RB-	53, 52	LVDS Input	LVDS Data inputs
RB[0:6]	8, 9, 10, 11, 13, 14, 15	LVTTL Output	Single-ended data outputs
RCLK+, RCLK-	55, 54	LVDS Input	LVDS Clock inputs
RX ENABLE	59	LVTTL Input	Receiver enable: When asserted (low input), the receiver outputs go to a known low state.
RX GND	6, 16, 60		Ground pins for RX TTL outputs
RX LVDS GND	51		Ground pin for RX LVDS inputs
RX LVDS V _{CC}	58	Dower Cumply	Power supply pin for RX LVDS inputs
RX PLL GND	50	Power Supply	Ground pin for PLL RX circuitry
RX PLL V _{CC}	49		Power supply pin for PLL RX circuitry
RX V _{CC}	1, 7, 12		Power supply pins for RX TTL outputs
TA+, TA-	41, 42	LVDS Output	LVDS Data outputs
TA[0:6]	19, 20, 21, 23, 24, 25, 26	LVTTL Input	Single-ended data inputs
TB+, TB-	45, 46	LVDS Output	LVDS Data outputs
TB[0:6]	28, 29, 30, 31, 33,34, 35	LVTTL Input	Single-ended data inputs
TCLK+, TCLK-	43, 44	LVDS Output	LVDS Clock outputs
TX ENABLE	48	LVTTL Input	Transmitter enable: When asserted (low input), the driver outputs are high-impedance.
TX GND	18, 36		Ground pins for TX TTL inputs
TX LVDS GND	40		Ground pin for TX LVDS outputs
TX LVDS V _{CC}	47	Power Supply	Power supply pin for TX LVDS outputs
TX PLL GND	39	1.0Met Subbit	Ground pin for PLL TX circuitry
TX PLL V _{CC}	38		Power supply pin for PLL TX circuitry
TX V _{CC}	22, 27, 32		Power supply pins for TX TTL inputs

ORDERING INFORMATION(1)

PRODUCT	PACKAGE	ORDERING NUMBER
SN75LVDT1422	TQFP (PAG)	SN75LVDT1422

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



ABSOLUTE MAXIMUM RATINGS(1)

		UNIT
Supply voltage range, V _{CC}	(2)	-0.5 V to 4 V
Voltage range at any terminal		-0.3 V to V _{CC} + 0.3 V
	Human Body Model (3) (All pins)	±5 kV
Electrostatic discharge	Machine Model (4)(All pins)	±200 V
	Charged-Device Model ⁽⁵⁾ (All pins)	±500 V
Continuous power dissipation See Dissipation		See Dissipation Rating Table
Storage temperature range		−65°C to 125°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltage values are with respect to the GND terminals
- In accordance with JEDEC Standard 22, Test Method A114-A. In accordance with JEDEC Standard 22, Test Method A115.
- In accordance with JEDEC Standard 22, Test Method C101.

DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	T _A ≤ 25°C	DERATING FACTOR ⁽¹⁾ ABOVE T _A = 25°C	T _A = 70°C POWER RATING
TQFP (PAG)	Low-K ⁽²⁾	813 mW	8.13 mW/°C	448 mW
TQFP (PAG)	High-K ⁽³⁾	1076 mW	10.76 mW/°C	592 mW

- This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
- In accordance with the Low-K thermal metric definitions of EIA/JESD51-2.
- In accordance with the High-K thermal metric definitions of EIA/JESD51-6.

THERMAL CHARACTERISTICS

PARAMETER			TEST CONDITIONS	VALUE	UNIT
$R_{\theta JB}$	BJB Junction-to-board thermal resistance			69.5	°C/W
$R_{\theta JC}$	Junction-to-case thermal res	istance		39.2	C/ VV
D	Davisa naver dissination	Typical	$V_{CC} = 3.3 \text{ V}, T_A = 25^{\circ}\text{C}, f = 100 \text{ MHz}$	357.4	m)\/
P _D	Device power dissipation	Maximum	V _{CC} = 3.6 V, T _A = 70°C , f = 100 MHz	455.8	mW

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	GND		0.8	V
$ V_{ID} $	Magnitude of differential input voltage	0.1		0.6	V
V_{IC}	Common-mode input voltage range, receiver	VID /2		2.4 – VID /2	V
T _A	Operating free-air temperature	-10		70	°C
V_N	Supply noise voltage, V _{CC}	-50		50	mV
f _c	Clock frequency	10		100	MHz



RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IT+}	Positive-going differential input threshold voltage				100	mV
V _{IT}	Negative-going differential input threshold voltage		-100			mV
V _{OH}	High-level output voltage	I _{OH} = -4 mA	2.4			V
V_{OL}	Low-level output voltage	I _{OL} = 4 mA			0.4	V
V_{IK}	Input clamp voltage	I _I = -18 mA	-1.5	-0.8		V
I	Input current with integrated termination	$V_{I} = 0 \text{ V or } 2.4 \text{ V}, V_{CC} = 3.6 \text{ V}$	-45		45	μΑ
I _{I(OFF)}	Power-off input current	V _{CC} = 0 V, V _I = 2.4 V	-10		10	μΑ
R _T	Termination resistance	V_{ID} = 100 mV, V_{IC} = 0.05 V to 2.4 V	90	110	132	Ω
Ci	Input capacitance			2		pF

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

TRANSMITTER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
$ V_{OD} $	Differential output voltage magnitude	$R_L = 100 \Omega$	250	365	450	mV
$\Delta V_{OD} $	Change in differential output voltage magnitude between logic states		-35		35	mV
V _{OC(SS)}	Steady-state common-mode output voltage		1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		-35		35	mV
V _{OC(PP)}	Peak-to-peak common-mode output voltage			30	80	mV
I _{IH}	High-level input current	V _{IH} = 2 V			20	μΑ
I _{IL}	Low-level input current	V _{IL} = 0.8 V	-10		10	μΑ
V _{IK}	Input clamp voltage	I _I = -18 mA	-1.5	-0.8		V
	Chart singuit autout auronat	V_{O+} or $V_{O-} = 0 \text{ V}$	-24		24	Λ
los	Short-circuit output current	V _{OD} = 0 V	-12		12	mA
I _{O(OFF)}	Power-off output current	$V_{CC} = 0 \text{ V}, V_{O} = 2.4 \text{ V}$	-10		10	μΑ
Ci	Input capacitance			3		pF

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

TRANSMITTER SUPPLY CURRENT

PARAMETER		TEST CONDITIONS		MIN TYP(1)	MAX	UNIT
	-	f = 10 MHz	17	23		
		f = 25 MHz	19	27		
	L Cupply ourrent (worst acce)	See Figure 1 and Figure 2	f = 40 MHz	22	30	A
I _{CC} Supply current (worst case)	See Figure 1 and Figure 2	f = 65 MHz	29	34	mA	
		f = 85 MHz	34	45	ı	
			f = 100 MHz	38	49	

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



RECEIVER SUPPLY CURRENT

PARAMETER		TEST CONDITIONS		MIN TYP(1)	MAX	UNIT
0			f = 10 MHz	19	35	
		f = 25 MHz	27	42		
	Supply current (worst case)	See Figure 1 and Figure 3	f = 40 MHz	35	45	
ICC			f = 65 MHz	49	69	mA
			f = 85 MHz	60	81	
			f = 100 MHz	69	90	

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SUPPLY CURRENT⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN TYP(2)	MAX	UNIT
I _{CC(DIS)}	Disable supply current	TX/RX ENABLEs = GND	150	800	μΑ

⁽¹⁾ CMOS inputs have to connect to ground.

TRANSMITTER INPUT TIMING REQUIREMENTS

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{t(CLK)}	Transition time, CLK IN	See Figure 5	1.0		6.0 ⁽²⁾	ns
t _{c(CLK)}	Input clock period, CLK IN		10	Т	100	ns
t _{wH(CLK)}	Pulse duration, clock high, CLK IN	See Figure 6	0.35T	0.5T	0.65T	ns
t _{wL(CLK)}	Pulse duration, clock low, CLK IN		0.35T	0.5T	0.65T	ns
t _{t(EN)}	Transition time, TX ENABLE, TAx/TBx		1.5		6.0	ns

TRANSMITTER SWITCHING CHARACTERISTICS

	PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t _r	LVDS Rise time	See Figure 4		0.38	0.7	ns
t _f	LVDS Fall time	See Figure 4		0.38	0.7	ns
t ₀	Output pulse position for bit 0		-0.8	0	0.8	
t ₁	Output pulse position for bit 1		13.49	14.29	15.09	
t ₂	Output pulse position for bit 2		27.77	28.57	29.37	
t ₃	Output pulse position for bit 3	f = 10 MHz, See Figure 12	42.06	42.86	43.66	ns
t ₄	Output pulse position for bit 4		56.34	57.14	57.94	
t ₅	Output pulse position for bit 5		70.63	71.43	72.23	
t ₆	Output pulse position for bit 6		84.91	85.71	86.51	
t ₀	Output pulse position for bit 0		-0.45	0	0.45	
t ₁	Output pulse position for bit 1		5.26	5.71	6.16	
t ₂	Output pulse position for bit 2		10.98	11.43	11.83	
t ₃	Output pulse position for bit 3	f = 25 MHz, See Figure 12	16.69	17.14	17.54	ns
t ₄	Output pulse position for bit 4		22.41	22.86	23.26	
t ₅	Output pulse position for bit 5		28.12	28.57	28.97	
t ₆	Output pulse position for bit 6		33.84	34.29	34.69	

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

⁽²⁾ All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

⁽¹⁾ All typical values are at V_{CC} = 3.3 V, T_A = 25°C. (2) Regulate clock frequency lower than 50 MHz. $t_{t(CLK)max}$ = 1/f x 50% x 60%.



TRANSMITTER SWITCHING CHARACTERISTICS (continued)

	PARAMETER	TEST CONDITIO	MIN	TYP ⁽¹⁾	MAX	UNIT		
t ₀	Output pulse position for bit 0		-0.25	0	0.25	·		
t ₁	Output pulse position for bit 1			3.32	3.57	3.82		
t ₂	Output pulse position for bit 2			6.89	7.14	7.39		
t ₃	Output pulse position for bit 3	f = 40 MHz, See Figure 12	10.46	10.71	10.96	ns		
t ₄	Output pulse position for bit 4		14.04	14.29	14.54			
t ₅	Output pulse position for bit 5			17.61	17.86	18.11		
t ₆	Output pulse position for bit 6			21.18	21.43	21.68		
t ₀	Output pulse position for bit 0			-0.20	0	0.20	·	
t ₁	Output pulse position for bit 1		2.00	2.20	2.40			
t ₂	Output pulse position for bit 2		4.20	4.40	4.60			
t ₃	Output pulse position for bit 3	f = 65 MHz, See Figure 12	6.39	6.59	6.79	ns		
t ₄	Output pulse position for bit 4		8.59	8.79	8.99			
t ₅	Output pulse position for bit 5		10.79	10.99	11.19			
t ₆	Output pulse position for bit 6		12.99	13.19	13.39			
t ₀	Output pulse position for bit 0		-0.15	0	0.15	·		
t ₁	Output pulse position for bit 1		1.53	1.68	1.83			
t ₂	Output pulse position for bit 2			3.21	3.36	3.51		
t ₃	Output pulse position for bit 3	f = 85 MHz, See Figure 12	4.89	5.04	5.19	ns		
t ₄	Output pulse position for bit 4		6.57	6.72	6.87			
t ₅	Output pulse position for bit 5			8.25	8.40	8.55	ı	
t ₆	Output pulse position for bit 6			9.93	10.08	10.23		
t ₀	Output pulse position for bit 0			-0.2	0	0.2		
t ₁	Output pulse position for bit 1		1.23	1.43	1.63	ns		
t ₂	Output pulse position for bit 2		2.66	2.86	3.06			
t ₃	Output pulse position for bit 3	f = 100 MHz, See Figure 12	4.09	4.29	4.49			
t ₄	Output pulse position for bit 4		5.51	5.71	5.91			
t ₅	Output pulse position for bit 5		6.94	7.14	7.34			
t ₆	Output pulse position for bit 6			8.37	8.57	8.77		
t _{su}	TAx/TBx Setup time to CLK IN	f OF MULT OF 100 MULT Coo	Figure 6	1				
t _h	TAx/TBx Hold time to CLK IN	f = 85 MHz or 100 MHz, See	rigure 6	0.25			ns	
			f = 10 MHz		1.0	2.98		
+	CLK IN to TCLK± Propagation delay time	See Figure 7 and Figure 8 ⁽²⁾	f = 25 MHz		1.38	3.21	ne	
τ _{pd} (TCC)	CER IN to TCER Fropagation delay time	See Figure 7 and Figure 6	f = 85 MHz		1.60	3.78	ns	
		f = 100 MHz			1.63	3.95		
t _{jit(C-C)}	TCLK± Clock cycle-to-cycle jitter	f = 85 MHz or 100 MHz				50	ps	
		f = 10 MHz						
		f = 25 MHz						
SSCG	Spread Spectrum Clock support; Modu-	f = 40 MHz		100		kHz		
3300	lation frequency with a linear profile (3)	f = 65 MHz	±2.5%/–5%			NI IZ		
		f = 85 MHz						
		f = 100 MHz				<u>. </u>		
t _{en(TPLL)}	Phase lock loop enable time	See Figure 9				10	ms	
t _{dis(T)}	Transmitter disable time	See Figure 11				100	ns	

⁽²⁾ Measure from CLK IN rising edge or falling edge to immediately crossing point of differential TCLK±, 50% duty cycle input clock is assumed

⁽³⁾ Care must be taken to ensure t_{su} and t_h are met so input data are sampling correctly. This SSCG parameter only shows the performance of tracking spread spectrum clock applied to CLK IN pin, and reflects the result on TCLK+ and TCLK- pins.



RECEIVER SWITCHING CHARACTERISTICS

	PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
	CMOS/LVTTL Bigg time	CLK OUT	See Figure 2		1.2	2.5	
t _r	CMOS/LVTTL Rise time		See Figure 3		2.0	3.5	ns
	CMOS/LVTTL Foll time	CLK OUT	Can Figure 2		1.2	2.5	ns
t _f	CMOS/LVTTL Fall time	RA or RB	See Figure 3		2.0	3.5	
t ₀	Input strobe position for bit 0			0.45	0.84	1.23	
t ₁	Input strobe position for bit 1			2.13	2.52	2.91	
t ₂	Input strobe position for bit 2			3.81	4.20	4.59	
t ₃	Input strobe position for bit 3		f = 85 MHz, See Figure 17	5.49	5.88	6.27	ns
t ₄	Input strobe position for bit 4			7.17	7.56	7.95	
t ₅	Input strobe position for bit 5			8.85	9.24	9.63	
t ₆	Input strobe position for bit 6			10.53	10.92	11.31	
t ₀	Input strobe position for bit 0			0.40	0.71	1.02	
t ₁	Input strobe position for bit 1 Input strobe position for bit 2 Input strobe position for bit 3 Input strobe position for bit 4			1.83	2.14	2.45	ns
t ₂				3.26	3.57	3.88	
t ₃			f = 100 MHz, See Figure 17	4.09	5.00	5.31	
t ₄				6.12	6.43	6.74	
t ₅	Input strobe position for bit 5			7.54	7.85	8.16	
t ₆	Input strobe position for bit 6			8.97	9.28	9.59	
	7.4(7.7)		f = 85 MHz, See Figure 18				
t _{SK}	RA/RB± Skew margin ⁽²⁾	f = 100 MHz, See Figure 18					ps
t _c	CLK OUT Typical period range			10	Т	100	ns
t _{wH}	CLK OUT Pulse duration, clock high	h		4.0	5	6.5	
t _{wL}	CLK OUT Pulse duration, clock low	,	f OF Mile Coo Figure 12	4.0	5	6.5	
t _{su}	Rax/RBx Setup time to CLK OUT		f = 85 MHz, See Figure 13	3.0			ns
t _h	Rax/RBx Hold time to CLK OUT			3.5			<u> </u>
t _{wH}	CLK OUT Pulse duration, clock high CLK OUT Pulse duration, clock low Rax/RBx Setup time to CLK OUT			3.0		5.0	
t _{wL}			f 400 MHz Cas Figure 40	3.0		5.0	
t _{su}			f = 100 MHz, See Figure 13	2.0			ns
t _h	Rax/RBx Hold time to CLK OUT			2.5			
t _{pd(RCC)}	RCLK± to CLK OUT Propagation de	elay time	At T _A = 25°C, V _{CC} = 3.3 V, See Figure 14		6	9	ns
t _{en(RPLL)}	Receiver phase lock loop enable tir	ne	See Figure 15			10	ms
t _{dis(R)}	Receiver disable time		See Figure 16			1	μs

All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. Receiver skew margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window - RSPos). This margin allows for LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and clock jitter (less than 150 ps).



PARAMETER MEASUREMENT INFORMATION

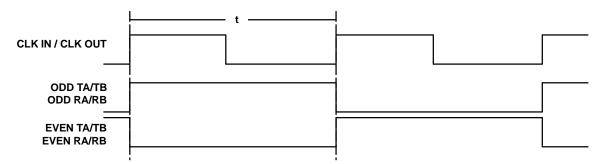


Figure 1. Worst Case Test Pattern

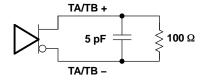


Figure 2. LVDS Output Load

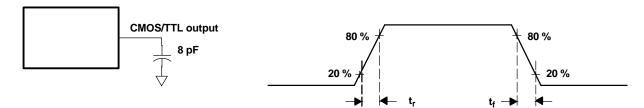


Figure 3. Receiver CMOS/LVTTL Output Load and Transition Times

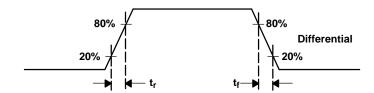


Figure 4. Transmitter LVDS Transition Times

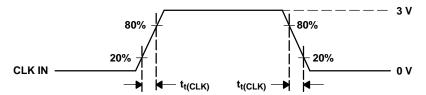


Figure 5. Transmitter Input Clock Transition Time



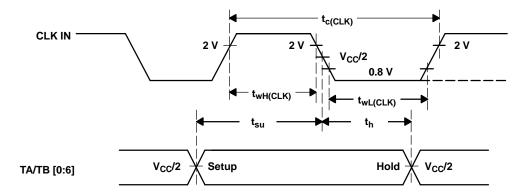


Figure 6. Transmitter Setup/Hold and High/Low Times (Falling Edge Strobe)

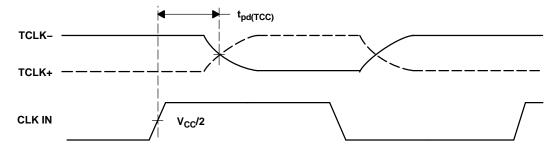


Figure 7. Transmitter Clock In to Clock Out Propagation Delay Time with R/F at V_{CC}

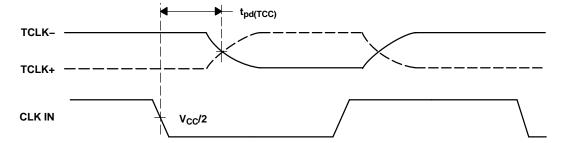


Figure 8. Transmitter Clock In to Clock Out Propagation Delay Time with R/F at GND

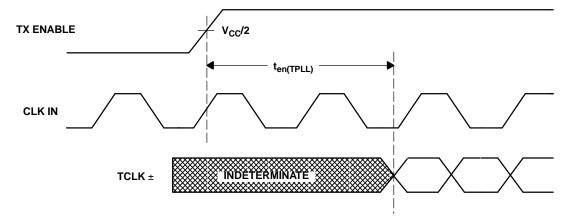


Figure 9. Transmitter Phase Lock Loop Enable Time



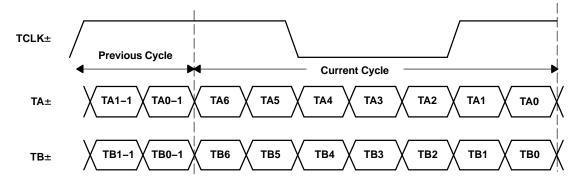


Figure 10. 14 Parallel TTL Data Inputs Mapped to LVDS Outputs

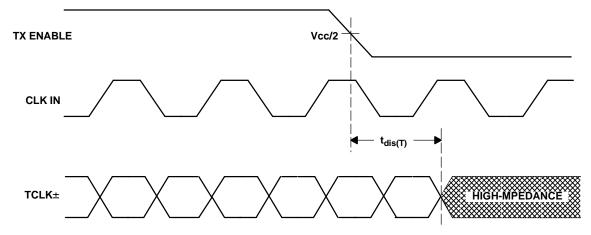


Figure 11. Transmitter Disable Time



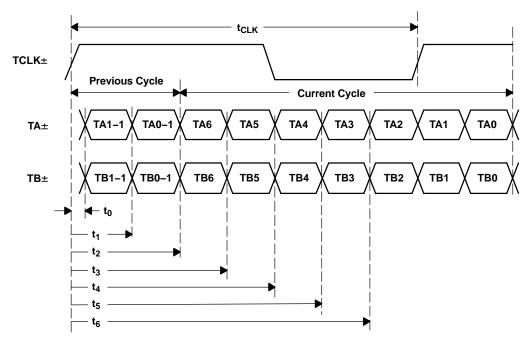


Figure 12. Transmitter LVDS Output Pulse Position Measurement

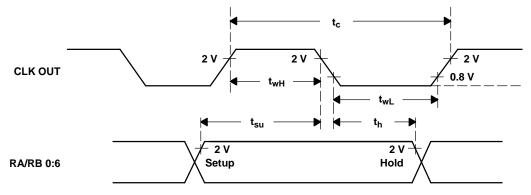


Figure 13. Receiver Setup/Hold and High/Low Times

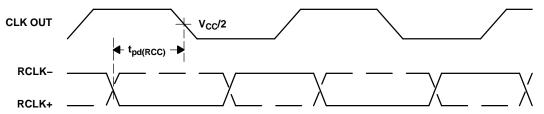


Figure 14. Receiver Clock In to Clock Out Propagation Delay Time



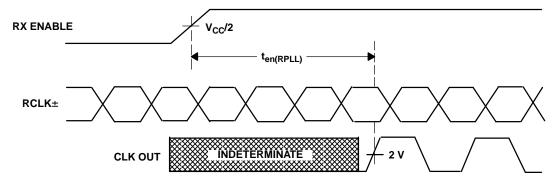


Figure 15. Receiver Phase Lock Loop Enable Time

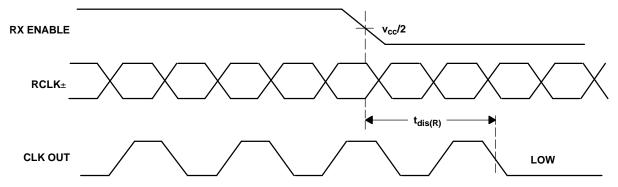


Figure 16. Receiver Disable Time



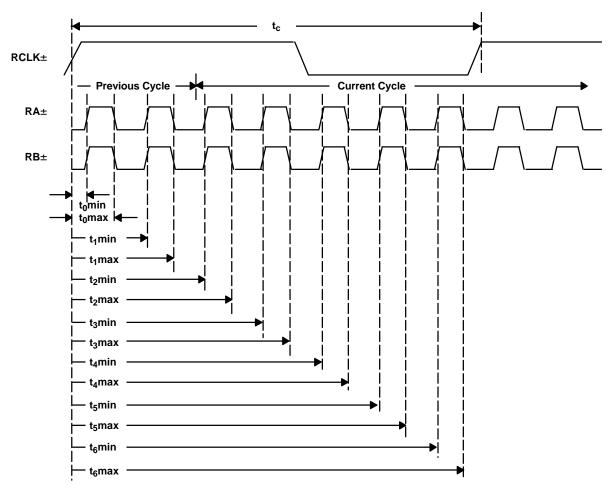
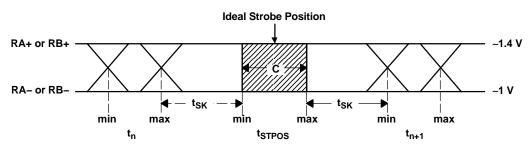


Figure 17. Receiver LVDS Input Strobe Position



- C Setup and hold time (internal data sampling window) defined by t_{STPOS}(receiver input strobe position) min and max
- (2) t_n Transmitter output pulse position (min and max)
- (3) t_{SK} = Cable skew (type, length) + source clock jitter (cycle to cycle) (5) + ISI (inter-symbol interference) (6)
- (4) Cable skew typically 10 ps to 40 ps per foot, media dependent
- (5) Cycle-to-cycle jitter is less than 150 ps at 85 MHz
- (6) ISI is dependent on interconnect length; may be zero

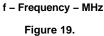
Figure 18. Receiver LVDS Input Skew Margin

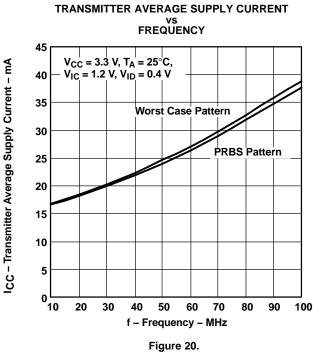
ICC - Receiver Average Supply Current - mA



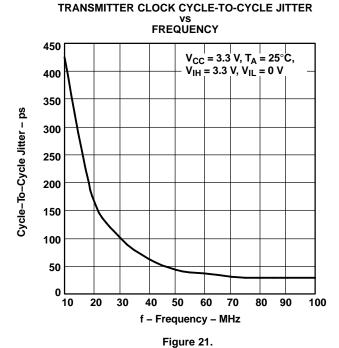
TYPICAL CHARACTERISTICS

RECEIVER AVERAGE SUPPLY CURRENT vs FREQUENCY V_{CC} = 3.3 V, T_A = 25°C, V_{IC} = 1.2 V, V_{ID} = 0.4 V Worst Case Pattern PRBS Pattern



TRANSMITTER CLOCK CYCLE-TO-CYCLE JITTER



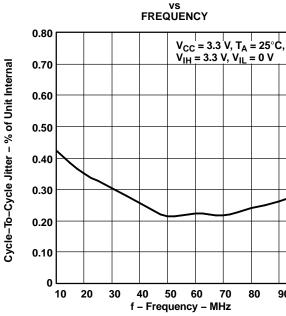


Figure 22.



APPLICATION INFORMATION

Power Source Sequence

There is no power-on sequence restriction to V_{CC} , LVDS V_{CC} , and PLL V_{CC} . In most applications, it is recommended to apply the same power source with the separate power planes and decoupling bypass capacitor groups. Use inductors to connect the different power planes.

Transmitter/Receiver Clock/Data Sequencing

There is no special requirement to the sequence of the input clock/data and enable signals. The input clock/data can be inserted after the enable signal is active. It is not necessary to cycle the enable signal when the clock/data is stopped and reapplied, like with the case of changing video modes within a graphics controller. When TX ENABLE pin is pulled low, the LVDS outputs of a SN75LVDT1422 transmitter are high-impedance, the PLL is shut down, and the transmitter is reset. When RX ENABLE is pulled low, the single-ended outputs of a SN75LVDT1422 receiver are at low status, the PLL is shut down, and the receiver is reset.

Spread Spectrum Clock Support

The transmitter of the SN75LVDT1422 accepts spread spectrum clocking signal type inputs. The outputs accurately track spread spectrum clock/data inputs with modulation frequencies of up to 100 kHz (max) with either center spread of ±2.5% or down spread -5% deviations.

Receiver Failsafe Feature

The receiver input failsafe bias circuitry ensures a stable output with known status while the receiver inputs are left floating.

When the receiver enable pin is active and a valid clock signal appears at the clock input, all of the data outputs are high if the data inputs are floating or idle. When the receiver enable pin is active and the clock input is floating, the last valid state is maintained on the data channels if the inputs are floating or idle. When the receiver enable pin is inactive, both data and clock outputs are kept low without considering the input status.

In an application with an unused data input, it is recommended to leave it open.

Receiver Failsafe Summary

RX ENABLE	DATA CHANNEL STATUS	CLOCK CHANNEL STATUS	FAILSAFE RESULT			
KA ENABLE	DATA CHANNEL STATUS	CLOCK CHANNEL STATUS	DATA	CLOCK		
High	Floating/Idle	Valid clock signal	High	Clock		
High	Floating/Idle	Floating/Idle	Last state	Low		
Low	Don't Care	Don't Care	Low	Low		

Transmitter Input, Receiver Output Pins

The single-ended I/O pins and control input pins are compatible with LVCMOS and LVTTL levels only. These pins are not 5-V tolerant.





21-Oct-2010

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN75LVDT1422PAG	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
SN75LVDT1422PAGG4	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
SN75LVDT1422PAGR	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
SN75LVDT1422PAGRG4	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





Α	0	Dimension designed to accommodate the component width
В	0	Dimension designed to accommodate the component length
		Dimension designed to accommodate the component thickness
٧	٧	Overall width of the carrier tape
ГР	1	Pitch between successive cavity centers

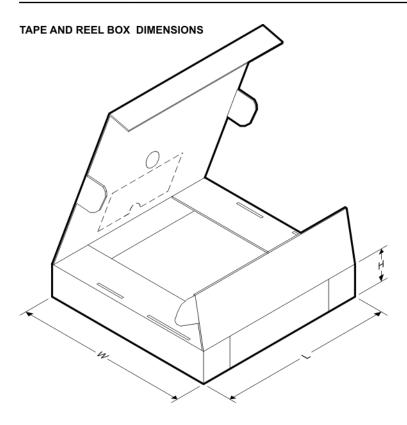
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVDT1422PAGR	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVDT1422PAGR	TQFP	PAG	64	1500	346.0	346.0	41.0

PAG (S-PQFP-G64)

PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-026

PAG (S-PQFP-G64)

PLASTIC QUAD FLATPACK



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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