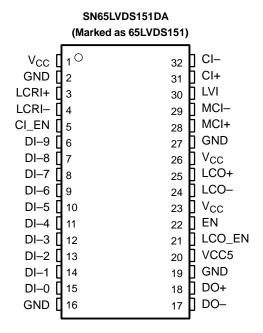


#### www.ti.com

## MuxIt™ SERIALIZER-TRANSMITTER

#### **FEATURES**

- A Member of the MuxIt<sup>™</sup> Serializer-Deserializer Building-Block Chip Family
- Supports Serialization of up to 10 Bits of Parallel Data Input at Rates up to 200 Mbps
- PLL Lock/Valid Input Provided to Enable Link Data Transfers
- Cascadable With Additional SN65LVDS151 MuxIt Serializer-Transmitters for Wider Parallel Input Data Channel Widths
- LVDS Compatible Differential Inputs and Outputs Meet or Exceed the Requirements of ANSI TIA/EIA-644-A
- LVDS Inputs and Outputs ESD Protection Exceeds 12 kV HBM
- LVTTL Compatible Inputs for Lock/Valid, Enables, and Parallel Data Inputs Are 5-V Tolerant
- Operates With 3.3 V Supply
- Packaged in 32-Pin DA Thin Shrink
   Small-Outline Package With 26 Mil Terminal
   Pitch



#### **DESCRIPTION**

MuxIt is a family of general-purpose, multiple-chip building blocks for implementing parallel data serializers and deserializers. The system allows for wide parallel data to be transmitted through a reduced number of transmission lines over distances greater than can be achieved with a single-ended (e.g., LVTTL or LVCMOS) data interface. The number of bits multiplexed per transmission line is user-selectable and allows for higher transmission efficiencies than with existing fixed ratio solutions. MuxIt utilizes the LVDS (TIA/EIA-644-A) low voltage differential signaling technology for communications between the data source and data destination.

The MuxIt family initially includes three devices supporting simplex communications: the SN65LVDS150 phase locked loop frequency multiplier, the SN65LVDS151 serializer-transmitter, and the SN65LVDS152 receiver-deserializer.

The SN65LVDS151 consists of a 10-bit parallel-in/serial-out shift register, three LVDS differential transmission line receivers, a pair of LVDS differential transmission line drivers, plus associated input buffers. It accepts up to 10 bits of user data on parallel data inputs (DI-0  $\rightarrow$  DI-9) and serializes (multiplexes) the data for transmission over an LVDS transmission line link. Two or more SN65LVDS151 units may be connected in series (cascaded) to accommodate wider parallel data paths for higher serialization values. Data is transmitted over the LVDS serial link at M times the input parallel data clock frequency. The multiplexing ratio M, or number of bits per data clock cycle, is programmed on the companion SN65LVDS150 MuxIt programmable PLL frequency multiplier with configuration pins (M1  $\rightarrow$  M5). The range of multiplexing ratio M supported by the SN65LVDS150 MuxIt programmable PLL frequency multiplier is between 4 and 40. Table 1 shows some of the combinations of LCRI and MCI supported by the SN65LVDS150 MuxIt programmable PLL frequency multiplier.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### **DESCRIPTION (CONTINUED)**

Data is parallel loaded into the SN65LVDS151 input latches on the first rising edge of the M-clock input (MCI) signal following a rising edge of the link clock reference input (LCRI). The data is read out serially from the SN65LVDS151 shift registers on the rising edges of the M-clock input (MCI). The lowest order bit of parallel input data, DI-0, is output from DO on the third rising edge of MCI following the rising edge of LCRI. The remaining bits of parallel input data, DI-1  $\rightarrow$  DI-(M-1) are clocked out sequentially, in ascending order, by subsequent MCI rising edges. The link clock output (LCO) signal rising edge is synchronized to the data output (DO) by an internal circuit clocked by MCI. The LCO signal rising edge follows the first rising edge of MCI after the rising edge of LCRI. Examples of operating waveforms for values of M = 4 and M = 10 are provided in Table 1.

Both the LCRI and MCI signals are intended to be sourced from the SN65LVDS150 MuxIt programmable frequency multiplier. They are carried over LVDS differential connections to minimize skew and jitter. The SN65LVDS151 includes LVDS differential line drivers for both the serialized data output (DO) stream and the link clock output (LCO). The cascade input (CI) is also an LVDS connection, and when it is used it is tied to the DO output of the preceding SN65LVDS151.

An internal power-on reset (POR) and an enable input (EN) control the operation of the SN65LVDS151. When  $V_{CC}$  is below 1.5 V, or when EN is low, the device is in a low-power disabled state, and the DO and LCO differential outputs are in a high-impedance state. When  $V_{CC}$  is above 3 V and EN is high, the device and the two differential outputs are enabled and operating to specifications. The link clock output enable input (LCO\_EN) is used to turn off the LCO output when it is not being used. Cascade input enable (CI\_EN) is used to turn off the CI input when it is not being used.

Serialized data bits are output from the DO output, starting in ascending order, from parallel input bit DI-0. The number of serialized data bits output per data clock cycle is determined by the multiplexing ratio M. For values of M less than or equal to 10, the cascade input (CI±) is not used, and only the first M parallel input bits (DI-0 thought DI-[M-1]) are used. For values of M greater than 10, all ten parallel input bits (DI-0 though DI-9) are used, and the cascade input is used to shift in the remaining data bits from additional SN65LVDS151 serializers. Table 2 shows which input data bits are used as a function of the multiplier M.

Table 1. Example Combinations of LCRI and MCI Supported by the SN65LVDS150 Muxit Programmable PLL Frequency Multiplier

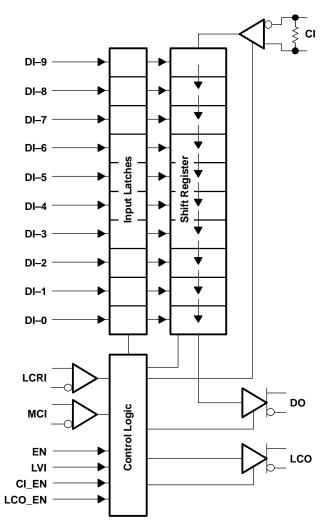
	LCR	LCRI, MHz		MHz
М	MINIMUM	MAXIMUM	MINIMUM	MAXIMUM
4	5	50	20	200
10	5	20	50	200
20	5	10	100	200
40	5	5	200	200



Table 2. Input Data Bits Used as a Function of the Mul	tiplier M
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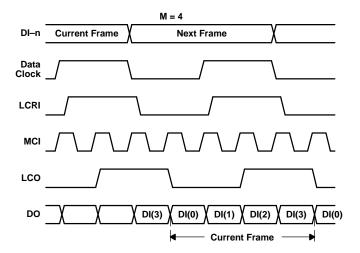
	M = 4	M = 5	M = 6	M = 7	M = 8	M = 9	M = 10	M >10
1 <sup>st</sup> bit output	DI-0							
2 <sup>nd</sup> bit output	DI-1							
3 <sup>rd</sup> bit output	DI-2							
4 <sup>th</sup> bit output	DI-3							
5 <sup>th</sup> bit output	Invalid	DI-4						
6 <sup>th</sup> bit output	Invalid	Invalid	DI-5	DI-5	DI-5	DI-5	DI-5	DI-5
7 <sup>th</sup> bit output	Invalid	Invalid	Invalid	DI-6	DI-6	DI-6	DI-6	DI-6
8 <sup>th</sup> bit output	Invalid	Invalid	Invalid	Invalid	DI-7	DI-7	DI-7	DI-7
9 <sup>th</sup> bit output	Invalid	Invalid	Invalid	Invalid	Invalid	DI-8	DI-8	DI-8
10 <sup>th</sup> bit output	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	DI-9	DI-9
11 <sup>th</sup> + bits output	Invalid	CI bits						

## **BLOCK DIAGRAM**



NOTE: The CI input includes a 110  $\Omega$  termination resistor.





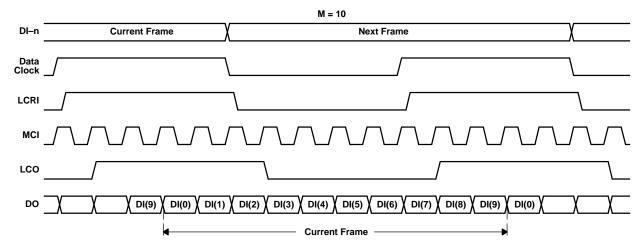
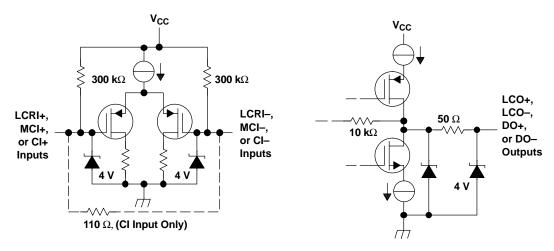
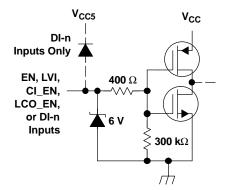


Figure 1. Operating Waveform Examples



#### **EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS**







#### **Terminal Functions**

TERMINAL		I/O TVDE		DESCRIPTION		
NAME	NO.	I/O	TYPE	DESCRIPTION		
CI+, CI-	31, 32	I	LVDS	Cascade input. This may be used to connect additional SN65LVDS151 units when the multiplexing ratio M value is greater than 10. This input has an internal $110-\Omega$ nominal termination resistor.		
CI_EN	5	I	LVTTL	Cascade input enable. Used to enable or disable the cascade input differential receiver. A high-level input enables the CI input, a low-level input disables the CI input.		
DO-, DO+	17, 18	0	LVDS	Data output. This is the data being transmitted to the destination end of the serial link, or being supplied to another SN65LVDS151 unit in cascade.		
EN	22	I	LVTTL	Enable. Controls device operation. A high-level input enables the device; a low-level input disables and resets the device. When initially enabled, all outputs are in a low-level condition.		
GND	2, 16, 19, 27		NA	Circuit ground		
LCO+, LCO-	25, 24	0	LVDS	Link clock output This is the data block synchronization clock being transmitted to the destination end of the serial link.		
LCO_EN	21	I	LVTTL	Link clock output enable. Used to disable the link clock output when it is not being used. A high-level input enables the LCO output; a low-level input disables the LCO output.		
LCRI+, LCR-	3, 4	I	LVDS	Link clock reference input. This is the clock for latching in the parallel data; it comes from the PLL frequency multiplier.		
LVI	30	I	LVTTL	Lock/valid input. This is a signal required for proper Muxlt system operation. It is directly connected to the LVO output of a SN65LVDS150. It is used to inhibit the operation of this device until after the PLL has stabilized. A low level input forces a reset of the internal latches and shift registers, and forces the DO and LCO outputs to a low level. A high level input enables operation.		
MCI+, MC-	28, 29	I	LVDS	M-clock input. This is the high frequency multiplied clock input from the local PLL frequency multiplier. It synchronizes the transmission of the link data		
DI-9-DI-0	6-15	I	LVTTL	Parallel data inputs. Data is latched into the device on the first rising edge of MCI following a rising edge of LCRI.		
V <sub>CC</sub>	1, 23, 26		NA	Supply voltage		
VCC5	20		NA	5-V $V_{CC}$ tolerance bias. Tied to 5 V nominal when the LVTTL inputs are being driven by a device powered from a 5-V supply, otherwise tied to local $V_{CC}$		

#### **ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
Supply voltage range, V <sub>CC</sub> <sup>(2)</sup>		–0.5 V to 4 V
	DI-0 through DI-9 inputs	-0.5 V to VCC5 +0.5 V
Voltage range	EN, CI_EN, LCO_EN, LVI inputs, VCC5	–0.5 V to 5.5 V
	Cl±, LCRI±, or MCl± Inputs, DO±, or LCO± outputs	-0.5 to 4 V
Floritanistic discharge human hady model(3)	MCI±, LCRI±, CI±, DO±, LCO±, and GND	±12 kV
Electrostatic discharge, human body model <sup>(3)</sup>	All pins	±2 kV
Charged-device model <sup>(4)</sup>	All pins	±500 V
Continuous power dissipation		See Dissipation Rating Table
Storage temperature range		−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case	e for 10 seconds	260°C

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- All voltage values, except differential I/O bus voltages, are with respect to network ground terminal. Tested in accordance with JEDEC Standard 22, Test Method A114-B. Tested in accordance with JEDEC Standard 22, Test Method C101.



#### **DISSIPATION RATING TABLE**

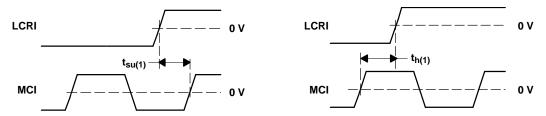
PACKAGE	T <sub>A</sub> ≤ 25°C	DERATING FACTOR	T <sub>A</sub> = 85°C
	POWER RATING	ABOVE T <sub>A</sub> = 25°C	POWER RATING
DA	1453 mW	11.6 mW/°C	756 mW

## RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage		3	3.3	3.6	V
$V_{IH}$	High-level input voltage	DIA DIA EN IVILIACI EN OLEM				V
$V_{IL}$	Low-level input voltage	DI-0 - DI-9, EN, LVI, LCO_EN, CI_EN			0.8	V
$ V_{ID} $	Magnitude of differential input voltage		0.1		0.6	V
$V_{IC}$	Common-mode input voltage	LCRI, MCI, CI	$\frac{ V_{\text{ID}} }{2}$		$2.4 - \frac{ V_{ D} }{2}$	V
					V <sub>CC</sub> -0.8	V
$T_A$	T <sub>A</sub> Operating free-air temperature				85	°C

#### **TIMING REQUIREMENTS**

	PARAMETERS	TEST CONDITIONS	MIN	MAX	UNIT	
t <sub>su(1)</sub>	LCRI <sup>↑</sup> setup time before MCI <sup>↑</sup>		0	0.5		ns
t <sub>h(1)</sub>	LCRI hold time after MCI↑		See Figure 2	0.3		ns
t <sub>su(2)</sub>	Data setup time, DI-0–DI-9 before MCI↑ after LC	0	0		ns	
t <sub>h(2)</sub>			See Figure 3	2		ns
	Ol antimations before MOI^	T <sub>A</sub> ≤ 25°C		0.8		
t <sub>su(3)</sub>	CI setup time before MCI↑	$T_A = 85^{\circ}C$	See Figure 4	1.1		ns
t <sub>h(3)</sub>	CI hold time after MCI↑			2.5		ns
	Olard made Con-	LCRI		20	200	
t <sub>c</sub>	Clock cycle time	MCI		5	50	ns
t <sub>w</sub>	High-level clock pulse width duration	MCI, LCRI		0.4 t <sub>c</sub>	0.6 t <sub>c</sub>	ns



**Figure 2. Clock Input Timing Requirements** 



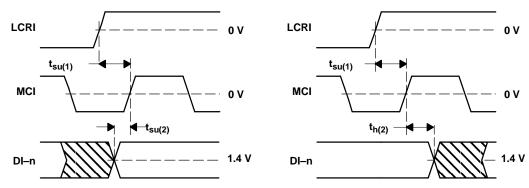
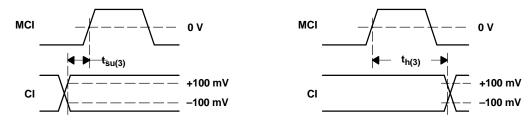


Figure 3. Data Input Timing Requirements



**Figure 4. Cascade Input Timing Requirements** 

## **ELECTRICAL CHARACTERISTICS**

over recommended operating conditions (unless otherwise noted)

	PARAM	IETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V <sub>ITH+</sub>	Positive-going differential input voltage threshold		Con Figure 5			100	mV
V <sub>ITH-</sub>	Negative-going differential input voltage threshold		See Figure 5	-100			mV
V <sub>OD(SS)</sub>	Steady-state differential outp	ut voltage magnitude	D 400 C V 400 mV	247	340	454	mV
$\Delta  V_{OD(SS)} $	Change in steady-state differ between logic states	rential output voltage magnitude	$R_L = 100 \Omega$ , $V_{ID} = \pm 100 \text{ mV}$ , See Figure 6 and Figure 7	-50		50	mV
V <sub>OC(SS)</sub>	Steady-stade common-mode	output voltage		1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state communications	mon-mode output voltage between logic	See Figure 8	-50		50	mV
V <sub>OC(PP)</sub>	Peak-to-peak change commo	on-mode output voltage			50	150	mV
			Enabled, $R_L = 100 \Omega$		22	30	
L Supply ourrent		Supply current			0.5	1	mA
Icc	очры синен		$f_{(MCI)} = 200$ MHz, $f_{(LCRI)} = 20$ MHz, $R_L = 100$ $\Omega$ , DI-n= 1010101010		35	65	1101
		(I <sub>I+</sub> - I <sub>I-</sub> ) (CI input)	V <sub>ID</sub> = 0.4 V, V <sub>IC</sub> = 2.2 V or 0.2 V	3		4.4	mA
I <sub>ID</sub>	Differential input current	(I <sub>I</sub> + - I <sub>I</sub> -) (LCRI, MCI inputs)	$V_{IC} = 0.05 \text{ V to } 2.35 \text{ V},$ $V_{ID} = \pm 0.1 \text{ V}$	-2		2	μΑ
		LODI MOL:	V <sub>I</sub> = 0 V	-2		-20	
	la a constant	LCRI, MCI inputs	V <sub>I</sub> = 2.4 V	-1.2			μA
կ	Input current	Chinaut	V <sub>I</sub> = 0 V	-4		-40	
		CI input	V <sub>I</sub> = 2.4 V	-2.4			μA
	D	LCRI, MCI inputs	V 0V V 00V			20	
I <sub>I(OFF)</sub>	Power-off output current	CI input	$V_{CC} = 0 \text{ V}, V_{I} = 3.6 \text{ V}$			40	μA
I <sub>IH</sub>	High-level input current	EN, LVI, DI-n, LCO_EN	V <sub>IH</sub> = 2 V			20	μΑ
I <sub>IL</sub>	Low-level input current	EN, LVI, DI-n, LCO_EN	V <sub>IL</sub> = 0.8 V			10	μΑ
	Ob and almostic automate and	PO 100	V <sub>O+</sub> or V <sub>O-</sub> = 0 V	-10		10	A
I <sub>OS</sub>	Short-circuit output current	DO, LCO	V <sub>OD</sub> = 0 V	-10		10	mA

(1) All typical values are at  $T_A$  = 25°C and with  $V_{CC}$  = 3.3 V.



## **ELECTRICAL CHARACTERISTICS (continued)**

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I <sub>OZ</sub> High-impedance output current		$V_O = 0 \text{ V or } V_{CC}$	-5		5	μA	
I <sub>O(OFF)</sub>	I <sub>O(OFF)</sub> Power-off output current		$V_{CC} = 1.5 \text{ V}$ , $V_{I} = 3.6 \text{ V}$	-5		5	μA
Cı	Input capacitance	LCRI, MCI inputs	$V_{ID} = (0.4\sin(4E6\pi t) + 0.5) V$		3		pF

#### **SWITCHING CHARACTERISTICS**

over recommended operating conditions (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Decreasion delevitime MCI <sup>↑</sup> to DO <sup>↑</sup>	$T_A \le 25^{\circ}C$		3	5	5.8	
t <sub>d(1)</sub>	Propagation delay time, MCI↑ to DO↑	T <sub>A</sub> = 85°C		3	5	6.1	ns
	Propagation delay time MCI <sup>↑</sup> to DO	T <sub>A</sub> ≤ 25°C	$R_L = 100 \Omega$ , $C_L = 10 pF$ , See	3	5	5.8	20
t <sub>d(2)</sub>	Propagation delay time, MCI↑ to DO↓	T <sub>A</sub> = 85°C	Figure 9	3	5	6.1	ns
	Propagation delay time MCI <sup>↑</sup> to I CO <sup>↑</sup>	$T_A \le 25^{\circ}C$		3	5	5.8	
t <sub>d(3)</sub>	Propagation delay time, MCI↑ to LCO↑	$T_A = 85$ °C		3	5	6.1	ns
t <sub>r</sub>	Differential output signal rise time			0.3	0.8	1.5	ns
t <sub>f</sub>	Differential output signal fall time		$R_L = 100 \Omega$ , $C_L = 10 pF$ , See	0.3	8.0	1.5	ns
t <sub>sk(p)</sub>	Pulse skew ( t <sub>PHL</sub> - t <sub>PLH</sub>  ), DO		Figure 10	-250	0	250	ps
t <sub>sk(pp)</sub>	Part-to-part output skew, DO				0	2.3	ns
$t_{sk(\omega)}$	Multiple-frequency skew, LCO↑ to DO↑ or DO↓		See Figure 11	-250	0	250	ps
t <sub>PZL</sub>					3	20	ns
t <sub>PLZ</sub>	t <sub>PLZ</sub> Propagation delay time, low-level to high-impedance		EN input to DO, LCO output, See Figure 12		3	10	ns
t <sub>PHZ</sub>	Propagation delay time, high-level to high-impeda	nce	200 Satpat, 200 Figure 12		4	10	ns

## PARAMETER MEASUREMENT INFORMATION

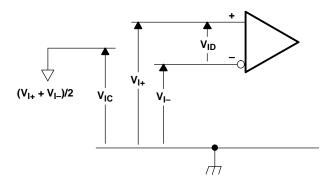


Figure 5. Receiver Voltage Definitions



Table 3. Receiver Minimum and Maximum Input Threshold Test Voltages

	LIED AGES	RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON- MODE INPUT VOLTAGE
V <sub>I+</sub>	V <sub>I</sub> _	$V_{ID}$	V <sub>IC</sub>
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	–100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	–100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	–100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	−600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	−600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	−600 mV	0.3 V

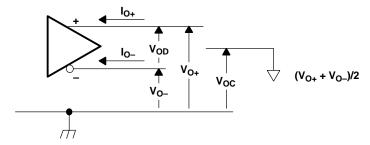


Figure 6. Driver Voltage and Current Definitions

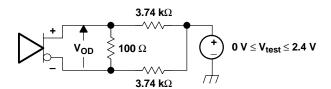
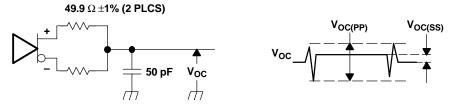


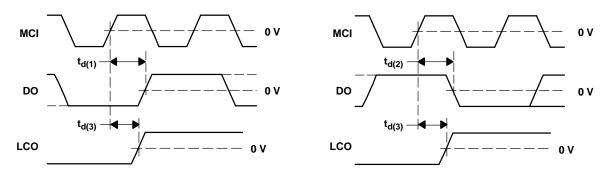
Figure 7. V<sub>OD</sub> Test Circuit



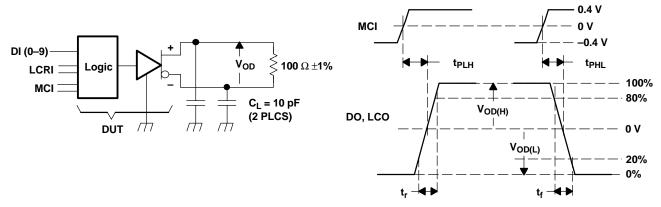
A. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \le 1$  ns, pulse repetition rate (PRR) = 0.5 Mpps, Pulse width = 500  $\pm$  10 ns.  $C_L$  includes instrumentation and fixture capacitance within 0,06 m of the D.U.T. The measurement of  $V_{OC(PP)}$  is made on test equipment with a -3 dB bandwidth of at least 5 GHz.

Figure 8. Test Circuit and Definitions for the Driver Common-Mode Output Voltage





**Figure 9. Output Timing Waveforms** 



A. All input pulses are supplied by generators having the following characteristics:  $t_r$  or  $t_f \le 1$  ns, MCI pulse repetition rate (PRR) = 50 Mpps, MCI Pulse width = 10 ± 0.2 ns, LCRI pulse repetition rate (PRR) = 5 Mpps, LCRI pulse width = 100 ±20 ns.  $C_1$  includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 10. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

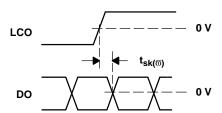


Figure 11. LCO to DO Multiple-Frequency Skew Waveforms



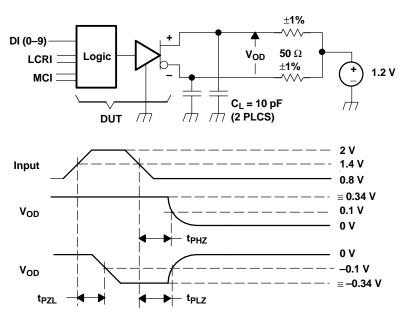
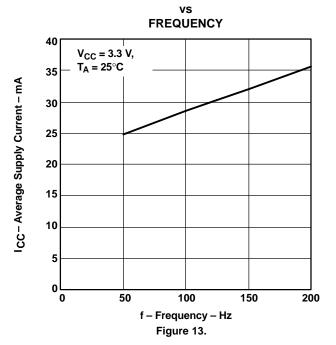


Figure 12. Enable/Disable Time Waveforms

# TYPICAL CHARACTERISTICS AVERAGE SUPPLY CURRENT



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