SN75LVDS31D (Marked as 75LVDS31)

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- Meets or Exceeds the Requirements of ANSI TIA/EIA-644 Standard
- Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100-Ω Load
- Signaling Rates up to 155 Mbps
- Operates From a Single 3.3-V Supply
- Driver at High Impedance When Disabled or With V<sub>CC</sub> = 0
- Low-Voltage TTL (LVTTL) Logic Input Levels
- Characterized For Operation From 0°C to 70°C

SN75LVDS31PW (Marked as DS31)											
(TOP VIEW)											
1A [ 1Y [	1	U 16 15	] V <sub>CC</sub> ] 4A								
1Z [	3	14	<b>4</b> Y								
G [ 2Z [	4 5	13 12	] 4Z ] G								
2Y [	6	11	] 3Z								
2A [ GND [	7 8	10 9	] 3Y ] 3A								

SN75LVDS9638D (Marked as DF638 or 7L9638) SN75LVDS9638DGK (Marked as AXK) (TOP VIEW)

	(			, ,
Vcc [	1	υ	8	] ] 1Y
V <sub>CC</sub> [ 1A [	2		7	] 1Z
2A [	3		6	] 2Y
GND [	4		5	] 2Z

#### description

The SN75LVDS31 and SN75LVDS9638 are differential line drivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as TIA/EIA-422B) to reduce

the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the four current-mode drivers will deliver a minimum differential output voltage magnitude of 247 mV into a  $100-\Omega$  load when enabled.

The intended application of these devices and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100  $\Omega$ . The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN75LVDS31 and SN75LVDS9638 are characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

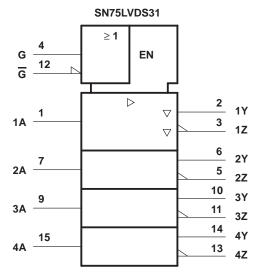
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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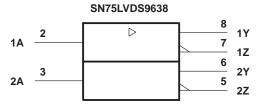
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### logic symbol<sup>†</sup>



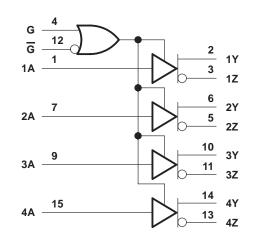
<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic symbol<sup>†</sup>

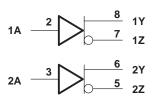


<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'LVDS31 logic diagram (positive logic)



'LVDS9638 logic diagram (positive logic)





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### **Function Tables**

	SN75LVDS31										
INPUT	ENA	BLES	OUTE	PUTS							
A	G	G	Y	Z							
Н	Н	Х	Н	L							
L	н	Х	L	н							
н	Х	L	Н	L							
L	Х	L	L	н							
Х	L	н	Z	Z							
Open	н	Х	L	н							
Open	Х	L	L	Н							

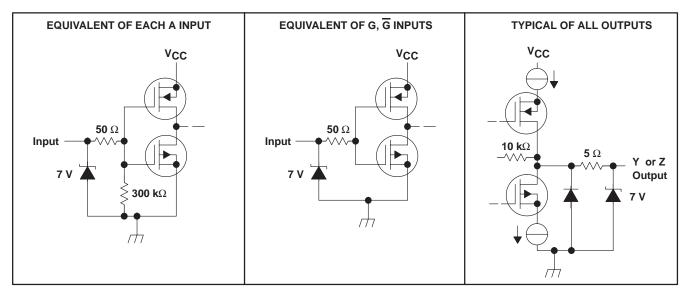
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

#### SN75LVDS9638

Ουτι	PUTS
Y	Z
Н	L
L	Н
L	Н
	Y H

H = high level, L = low level

### equivalent input and output schematic diagrams





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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC</sub> (see Note 1)	–0.5 V to 4 V
Input voltage range: Inputs	
Y or Z	–0.5 V to 4 V
Continuous total power dissipation	. See Dissipation Rating Table
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C
Storage temperature range, T <sub>stg</sub> Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages, except differential I/O bus voltages, are with respect to the network ground terminal.

DISSIPATION RATING TABLE											
PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR <sup>‡</sup> ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING								
D (8)	725 mW	5.8 mW/°C	464 mW								
D (16)	950 mW	7.6 mW/°C	608 mW								
PW	774 mW	6.2 mW/°C	496 mW								
DGK	425 mW	3.4 mW/°C	272 mW								

<sup>‡</sup> This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

#### recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC</sub>	3	3.3	3.6	V
High-level input voltage, VIH	2			V
Low-level input voltage, VIL			0.8	V
Operating free-air temperature, T <sub>A</sub>	0		70	°C



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### electrical characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONI	DITIONS	SN SN7		UNIT		
				MIN	TYP†	MAX		
VOD	Differential output voltage magnitud			247	340	454	mV	
ΔV <sub>OD</sub>	Change in differential output voltage between logic states	e magnitude	R <sub>L</sub> = 100 Ω,	See Figure 2	-50		50	mV
$\Delta VOC(SS)$	Change in steady-state common-mo between logic states	ode output voltage			1.125	1.2	1.375	V
VOC(SS)	Steady-state common-mode output	voltage	See Figure 3		-50		50	mV
VOC(PP)	Peak-to-peak common-mode outpu	t voltage				50	150	mV
	Supply current		$V_{I} = 0.8 V \text{ or } 2 V,$ No load	Enabled,		9	20	mA
Icc		SN75LVDS31	V <sub>I</sub> = 0.8 or 2 V, Enabled	R <sub>L</sub> = 100 Ω,		25	35	mA
	cepp. central		$V_{I} = 0 \text{ or } V_{CC},$	Disabled		0.25	1	mA
		SN75LVDS9638		No load		4.7	8	mA
		3N75LVD39030	$V_{I} = 0.8 V \text{ or } 2 V$	R <sub>L</sub> = 100 Ω		9	13	mA
Ιн	High-level input current		V <sub>IH</sub> = 2			4	20	μΑ
IIL	Low-level input current		V <sub>IL</sub> = 0.8 V			0.1	10	μΑ
	Short circuit output ourroat		$V_{O(Y)}$ or $V_{O(Z)} =$	0		-4	-24	mA
los	OS Short-circuit output current		$V_{OD} = 0$				±12	mA
IOZ	High-impedance output current		$V_0 = 0 \text{ or } 2.4 \text{ V}$				±1	μA
IO(OFF)	Power-off output current		$V_{CC} = 0,$	V <sub>O</sub> = 2.4 V			±1	μΑ
Cl	Input capacitance					3		pF

<sup>†</sup> All typical values are at  $T_A = 25^{\circ}C$  and with  $V_{CC} = 3.3$  V.

### switching characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	SN SN7	UNIT		
			MIN	TYP†	MAX	
<sup>t</sup> pLH	Propagation delay time, low-to-high-level output				6	ns
<sup>t</sup> pHL	Propagation delay time, high-to-low-level output				6	ns
tr	Differential output signal rise time (20% to 80%)			0.5	1.2	ns
tf	Differential output signal fall time (80% to 20%)	$R_L = 100 \Omega$ , $C_L = 10 pF$ , See Figure 2		0.5	1.2	ns
tsk(p)	Pulse skew ( t <sub>PHL</sub> – t <sub>PLH</sub>  ) <sup>‡</sup>				0.6	ns
tsk(o)	Channel-to-channel output skew§				0.6	ns
t <sub>sk(pp)</sub>	Part-to-part skew¶				1	ps
<sup>t</sup> pZH	Propagation delay time, high-impedance-to-high-level output				25	ns
<sup>t</sup> pZL	Propagation delay time, high-impedance-to-low-level output				25	ns
<sup>t</sup> pHZ	Propagation delay time, high-level-to-high-impedance output	See Figure 4			25	ns
<sup>t</sup> pLZ	Propagation delay time, low-level-to-high-impedance output				25	ns

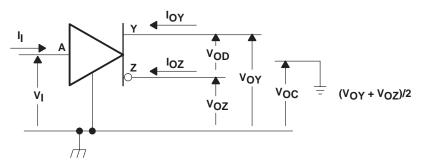
<sup>†</sup> All typical values are at  $T_A = 25^{\circ}C$  and with  $V_{CC} = 3.3 \text{ V}$ . <sup>‡</sup>  $t_{sk(p)}$  is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output. <sup>§</sup>  $t_{sk(o)}$  is the magnitude of the time difference between the outputs of a single device with all of their inputs connected together.

It sk(p) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, same temperature, and have identical packages and test circuits.

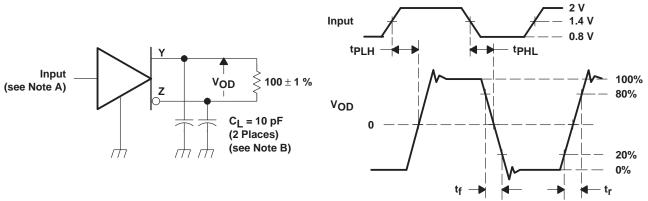


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### PARAMETER MEASUREMENT INFORMATION



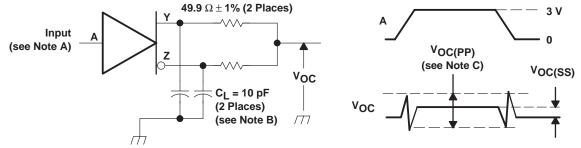




NOTES: A. All input pulses are supplied by a generator having the following characteristics:  $t_f \text{ or } t_f \le 1 \text{ ns}$ , pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.

B. CL includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

#### Figure 2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

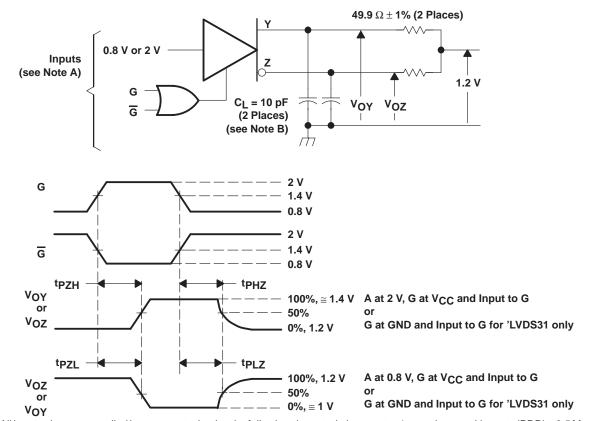


- NOTES: A. All input pulses are supplied by a generator having the following characteristics:  $t_f$  or  $t_f \le 1$  ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.
  - B. CL includes instrumentation and fixture capacitance within 6 mm of the D.U.T.
  - C. The measurement of VOC(PP) is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

#### Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



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## PARAMETER MEASUREMENT INFORMATION

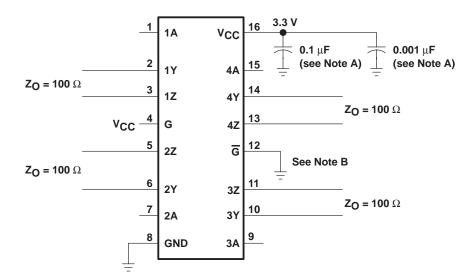
NOTES: A. All input pulses are supplied by a generator having the following characteristics:  $t_f$  or  $t_f < 1$  ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns.

B.  $C_L$  includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

#### Figure 4. Enable and Disable Time Circuit and Definitions



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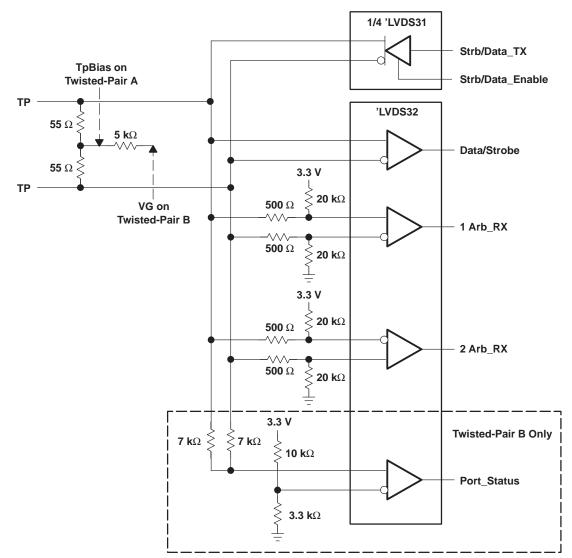
### APPLICATIONS INFORMATION

- NOTES: A. Place a 0.1  $\mu$ F and a 0.001  $\mu$ F Z5U ceramic, mica or polystyrene dielectric, 0805 size, chip capacitor between V<sub>CC</sub> and the ground plane. The capacitors should be located as close as possible to the device terminals.
  - B. Unused enable inputs should be tied to V<sub>CC</sub> or GND as appropriate.

#### **Figure 5. Typical Application Circuit Schematic**



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**APPLICATIONS INFORMATION** 

NOTES: A. Resistors are leadless thick-film (0603) 5% tolerance.

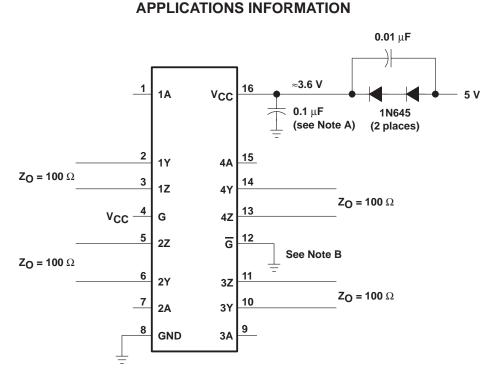
B. Decoupling capacitance is not shown but recommended.

- C. V<sub>CC</sub> is 3 V to 3.6 V.
- D. The differential output voltage of the 'LVDS31 can exceed that specified by IEEE1394.

Figure 6. 100 Mbps IEEE1394 Transceiver



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NOTE A: Place a 0.1 µF Z5U ceramic, mica or polystyrene dielectric, 0805 size, chip capacitor between V<sub>CC</sub> and the ground plane. The capacitor should be located as close as possible to the device terminals.

Figure 7. Operation With a 5-V Supply

### related information

IBIS modeling is available for this device. Please contact the local TI sales office or the TI Web site at *www.ti.com* for more information.

For more application guidelines, please see the following documents:

- Low-Voltage Differential Signalling Design Notes (TI literature number SLLA014)
- Interface Circuits for TIA/EIA-644 (LVDS) (TI literature number SLLA038)
- Reducing EMI With LVDS (TI literature number SLLA030)
- Slew Rate Control of LVDS Circuits (TI literature number SLLA034)
- Using an LVDS Receiver With RS-422 Data (TI literature number SLLA031)
- Evaluating the LVDS EVM (TI literature number SLLA033)

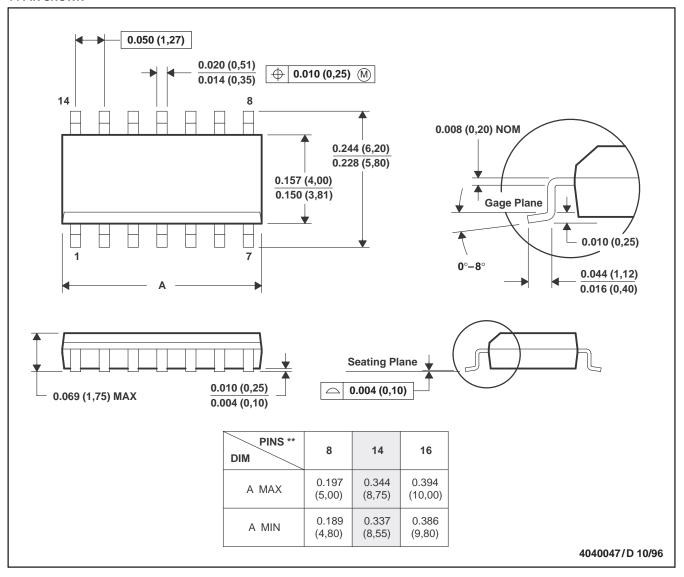


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### **MECHANICAL INFORMATION**

### PLASTIC SMALL-OUTLINE PACKAGE

### D (R-PDSO-G\*\*) 14 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-012

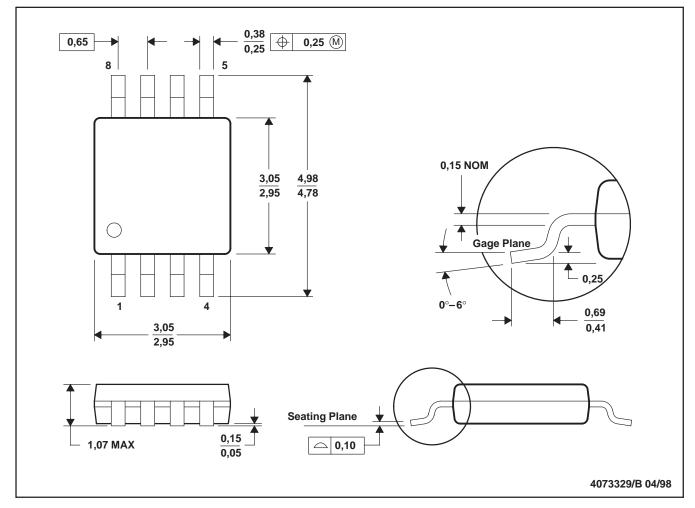


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**MECHANICAL INFORMATION** 

#### DGK (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO-187

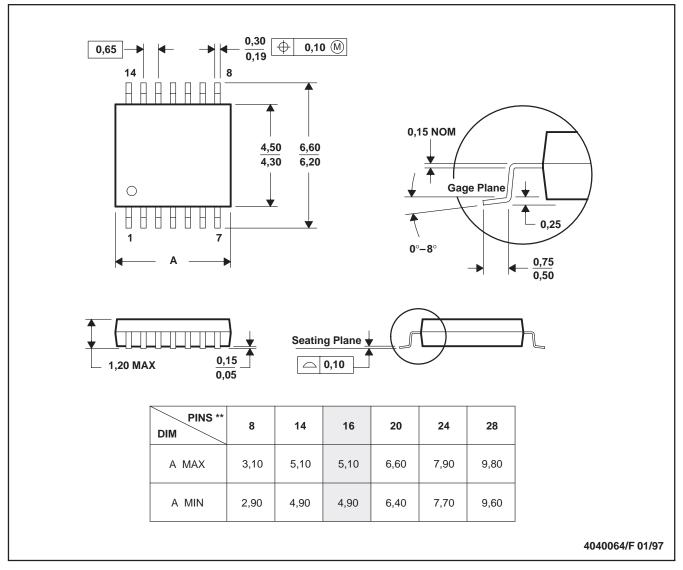


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### MECHANICAL INFORMATION

#### PLASTIC SMALL-OUTLINE PACKAGE

PW (R-PDSO-G\*\*) 14 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153



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#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN75LVDS31D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LVDS31DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LVDS31DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LVDS31DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LVDS31PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LVDS31PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LVDS9638D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LVDS9638DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LVDS9638DGK	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LVDS9638DGKG4	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## PACKAGE OPTION ADDENDUM



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### OTHER QUALIFIED VERSIONS OF SN75LVDS31 :

Military: SN55LVDS31

NOTE: Qualified Version Definitions:

• Military - QML certified for Military and Defense Applications

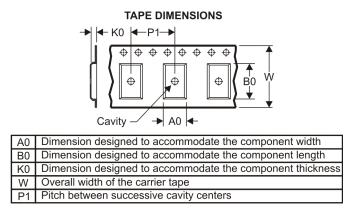
# PACKAGE MATERIALS INFORMATION

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### TAPE AND REEL INFORMATION





### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*	All dimensions are nominal												
	Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	SN75LVDS31DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TEXAS INSTRUMENTS

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# PACKAGE MATERIALS INFORMATION

29-Jul-2009



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVDS31DR	SOIC	D	16	2500	333.2	345.9	28.6

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