

1.8-V HIGH-SPEED DIFFERENTIAL LINE RECEIVER

Check for Samples: SN65LVDS4

FEATURES

- · Designed for Signaling Rates up to:
 - 500-Mbps Receiver

The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second)

- Operates From a 1.8-V or 2.5-V Core Supply
- Available in 1.5-mm × 2-mm QFN Package
- Bus-Terminal ESD Exceeds 2 kV (HBM)
- Low-Voltage Differential Signaling With Typical Output Voltages of 350 mV Into a 100-Ω Load
- Propagation Delay Times
 - 2.1 ns Typical Receiver
- Power Dissipation at 250 MHz
 - 40 mW Typical
- Requires External Failsafe
- Differential Input Voltage Threshold Less Than 50 mV
- Can Provide Output Voltage Logic Level (3.3-V LVTTL, 2.5-V LVCMOS, 1.8-V LVCMOS) Based on External VDD Pin, Thus Eliminating External Level Translation

APPLICATIONS

- Clock Distribution
- Wireless Base Stations
- Newtwork Routers

DESCRIPTION

The SN65LVDS4 is a single, low-voltage, differential line receiver in a small-outline QFN package.

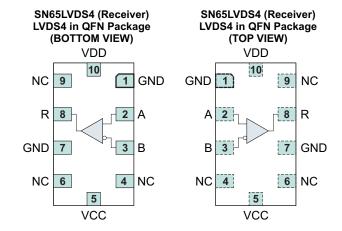


Table 1. Pin Description Table

PIN		I/O	DESCRIPTION	
NAME	NO.	1/0	DESCRIPTION	
Α	2	1	LVDS input, positive	
В	3	1	LVDS input, negative	
GND	1, 7	-	Ground	
NC	4, 6, 9	_	No connect	
R	8	0	1.8/2.5 LVCMOS/3.3 LVTTL output	
VCC	5	_	Core supply voltage	
VDD	10	-	Output drive voltage	

AVAILABLE OPTIONS

PART NUMBER	INTEGRATED TERMINATION	PACKAGE	PACKAGE MARKING
SN65LVDS4RSE	No	QFN	QXB

The SN65LVDS4 is characterized for operation from -40°C to 85°C.

Table 2. FUNCTION TABLE

INPUTS	OUTPUT ⁽¹⁾
$V_{ID} = V_A - V_B$	R
V _{ID} ≥ 50 mV	Н
V _{ID} ≤ -50 mV	L

(1) H = high level, L = low level, ? = indeterminate



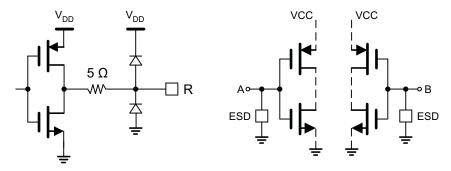
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

RECEIVER EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

DAD	AMETER	Values			Values		Huita
PARAMETER		MIN	MAX	Units			
Supply voltage range, V _{CC} ⁽²⁾		-0.5	4	V			
Receiver output voltage logic level and driver input voltage logic level supply, V_{DD}		-0.5	4	V			
Input voltage range, V _I	(A or B)	-0.5	V _{CC} + 0.3	V			
Output voltage, V _O	(R)	-0.5	$V_{DD} + 0.3$	V			
Differential input voltage magnitude, $ V_{ID} $			1 V				
Receiver output current, I _O		-12	12	mA			
Human-body model electrostatic disch	arge, HBM ESD ⁽³⁾						
	All pins		2000	V			
	Bus pins (A, B, Y, Z)		2000	V			
Field-induced-charge device model electrostatic discharge, FCDM ESD ⁽⁴⁾			500	V			
Continuous total power dissipation, P _D		See th	ne Thermal Information	n Table			
Storage Temperature Range (non ope	rating)	-65	150	°C			

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

Test method based upon JEDEC Standard 22, Test Method A114-A. Bus pins stressed with respect to GND and V_{CC} separately.

Test method based upon EIA-JEDEC JESD22-C101C.



THERMAL INFORMATION

		SN65LVDS4	
	THERMAL METRIC ⁽¹⁾	RSE	UNIT
		10 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	171.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance ⁽³⁾	60.7	°C/W
θ_{JB}	Junction-to-board thermal resistance (4)	71.4	°C/W
Ψлт	Junction-to-top characterization parameter ⁽⁵⁾	0.8	°C/W
ΨЈВ	Junction-to-board characterization parameter ⁽⁶⁾	64.7	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance ⁽⁷⁾	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	TEST CONDITION	MIN	NOM	MAX	UNIT
V _{CC1.8}	Core supply voltage		1.62	1.8	1.98	V
V _{CC2.5}	Core supply voltage		2.25	2.5	2.75	V
V _{DD1.8}	Output drive voltage		1.62	1.8	1.98	V
V _{DD2.5}	Output drive voltage		2.25	2.5	2.75	V
$V_{DD3.3}$	Output drive voltage		3	3.3	3.6	V
T _A	Operating free-air temperature		-40		85	°C
$ V_{ID} $	Magnitude of differential input voltage		0.15		0.6	V
f _{op}	Operating frequency range		10		250	MHz
VIN _{MAX}	Input voltage (any combination of input or common-mode voltage) ⁽¹⁾ See VIN _{MAX} .		0		V_{CC}	٧

⁽¹⁾ Any combination of input or common-mode voltage should not be below 0 V or above V_{CC}.



RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions, V_{CC} = 2.5 V, V_{ID} = 150 mV-600 mV, V_{CM} = $V_{ID}/2$ to $V_{CC} - V_{ID}/2$ V, 10 pF load (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN ⁽¹⁾	TYP ⁽²⁾	MAX	UNIT
V _{ITH+}	Positive-going differential input voltage threshold	See Figure 4 V			50	mV
V _{ITH} _	Negative-going differential input voltage threshold	See Figure 1, V _{CC1.8} , V _{CC2.5}	-50			mv
		$V_{DD} = 3.3V$, $I_{OH} = -8$ mA	V _{DD} - 0.2	5		
V_{OH}	High-level output voltage	$V_{DD} = 2.5V$, $I_{OH} = -6$ mA	V _{DD} - 0.2	5		V
		$V_{DD} = 1.8 \text{ V}, I_{OH} = -4 \text{ mA}$	V _{DD} - 0.2	5		
		$V_{DD} = 3.3 \text{ V}, I_{OL} = 8 \text{ mA}$			0.25	
V_{OL}	Low-level output voltage	$V_{DD} = 2.5 \text{ V}, I_{OL} = 6 \text{ mA}$			0.25	V
		$V_{DD} = 1.8 \text{ V}, I_{OL} = 4 \text{ mA}$			0.25	
D	Statio nawar	No load, steady state, $V_{DD} = 3.3 \text{ V}, V_{ID} +$		22	28	mW
P _{static}	Static power	No load, steady state, $V_{DD} = 2.5 \text{ V}$, V_{ID} +		20	25	IIIVV
C _I	Input capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5 V$		4		pF
Co	Output capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5 V$		4		pF

⁽¹⁾ The algebraic convention, in which the least positive (most negative) limit is designated as a minimum, is used in this data sheet.

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions, V_{CC} = 1.8 V, V_{ID} = 150 mV-600 mV, V_{CM} = $V_{ID}/2$ to $V_{CC} - V_{ID}/2$ V, 10 pF load (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN ⁽¹⁾	TYP ⁽²⁾	MAX	UNIT
V _{ITH+}	Positive-going differential input voltage threshold	Con Figure 4 V			50	\/
V _{ITH} _	Negative-going differential input voltage threshold	See Figure 1, V _{CC1.8} , V _{CC2.5}	-50			mV
		$V_{DD} = 3.3V$, $I_{OH} = -8$ mA	V _{DD} - 0.2	5		
V_{OH}	High-level output voltage	$V_{DD} = 2.5V, I_{OH} = -6 \text{ mA}$	V _{DD} - 0.2	5		V
		$V_{DD} = 1.8 \text{ V}, I_{OH} = -4 \text{ mA}$	V _{DD} - 0.2	5		ı
		$V_{DD} = 3.3 \text{ V}, I_{OL} = 8 \text{ mA}$			0.25	
V_{OL}	Low-level output voltage	$V_{DD} = 2.5 \text{ V}, I_{OL} = 6 \text{ mA}$			0.25	V
		$V_{DD} = 1.8 \text{ V}, I_{OL} = 4 \text{ mA}$			0.25	ı
		No load, steady state, $V_{DD} = 3.3 \text{ V}$, V_{ID} +		18	21	
P _{static}	Static power	No load, steady state, $V_{DD} = 2.5 \text{ V}$, V_{ID} +		16	19	mW
		No load, steady state, $V_{DD} = 1.8 \text{ V}$, V_{ID} +		13	16	ı
Cı	Input capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5 V$		4		pF
Co	Output capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5 V$		4		pF

⁽¹⁾ The algebraic convention, in which the least positive (most negative) limit is designated as a minimum, is used in this data sheet.

²⁾ All typical values are at 25°C.

⁽²⁾ All typical values are at 25°C.



RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions, V_{CC} = 2.5 V, V_{ID} = 150 mV-600 mV, V_{CM} = $V_{ID}/2$ to $V_{CC} - V_{ID}/2$ V, 10 pF load (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output				2.5	3.3	ns
t _{PHL}	Propagation delay time, high-to-low-level output				2.5	3.3	ns
t _{sk(p)}	Pulse skew $(t_{pHL} - t_{pLH})^{(2)}$					240	ps
	Output signal rise time	C _L = 10 pF, See Figure 3	$V_{DD} = 3.3 \text{ V}$			550	20
ι _r	t _r Output signal rise time	occ riguic o	$V_{DD} = 2.5 \text{ V}$			600	ps
	Output signal fall time		$V_{DD} = 3.3 \text{ V}$			550	
t _f	Output signal fall time		$V_{DD} = 2.5 \text{ V}$			600	ps
t _{jit}	Residual jitter added	Carrier frequency = 122.8 amplitude = 500 mVpp sine bandwidth for rms jitter = 2 = 2.5 V	e wave, integration		370		fs

⁽¹⁾ All typical values are at 25°C.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions, V_{CC} = 1.8 V, V_{ID} = 150 mV-600 mV, V_{CM} = $V_{ID}/2$ to $V_{CC} - V_{ID}/2$ V, 10 pF load (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN T	(1) YP	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output				3.2	3.8	ns
t _{PHL}	Propagation delay time, high-to-low-level output				3.2	3.8	ns
t _{sk(p)}	Pulse skew (t _{pHL} - t _{pLH}) ⁽²⁾					240	ps
		_	V _{DD} = 3.3 V			550	
t _r	Output signal rise time	V _{DI}	V _{DD} = 2.5 V			600	ps
			V _{DD} = 1.8 V			750	
			V _{DD} = 3.3 V			550	
t _f	Output signal fall time		V _{DD} = 2.5 V			600	ps
			V _{DD} = 1.8 V			750	
t _{jit}	Residual jitter added				370		fs

⁽²⁾ $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

 ⁽¹⁾ All typical values are at 25°C.
 (2) t_{sk(p)} is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.



PARAMETER MEASUREMENT INFORMATION

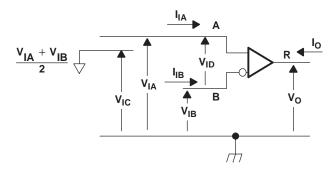
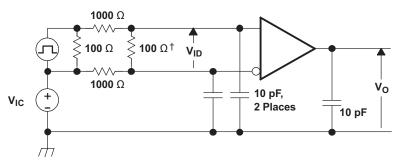
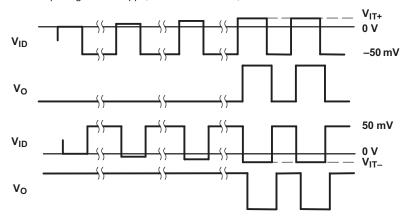


Figure 1. Receiver Voltage and Current Definitions



[†] Remove for testing LVDT device.

NOTE: Input signal of 3 Mpps, duration of 167 ns, and transition time of <1 ns.



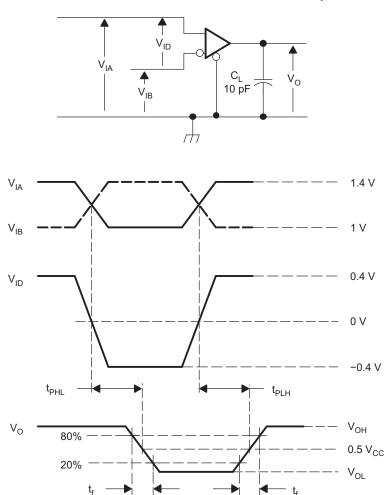
NOTE: Input signal of 3 Mpps, duration of 167 ns, and transition time of <1 ns.

30481-01

Figure 2. $V_{\text{IT+}}$ and $V_{\text{IT-}}$ Input Voltage Threshold Test Circuit and Definitions



PARAMETER MEASUREMENT INFORMATION (continued)



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 3. Receiver Timing Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

VICM = 1.2 V, VID = 300 mV, C_L = 10 pF, input rise time and fall time = 1 ns, input frequency = 250 MHz, 50% duty cycle, T_A = 25°C, unless otherwise noted

-0.5

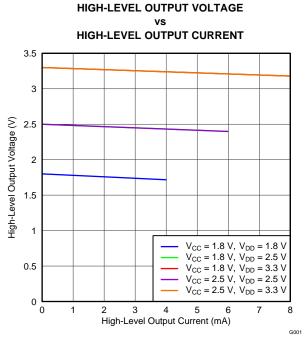


Figure 4.

LOW-LEVEL OUTPUT VOLTAGE

vs

NSTRUMENTS

8

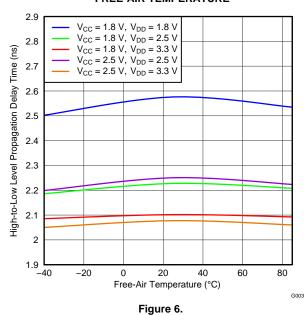
G002

Figure 5.

Low-Level Output Current (mA)

3

HIGH- TO LOW-LEVEL PROPAGATION DELAY TIME VS FREE-AIR TEMPERATURE



LOW- TO HIGH-LEVEL PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

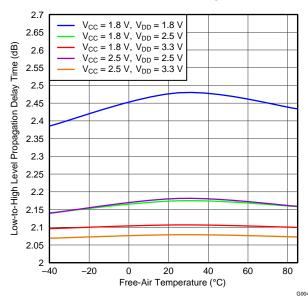
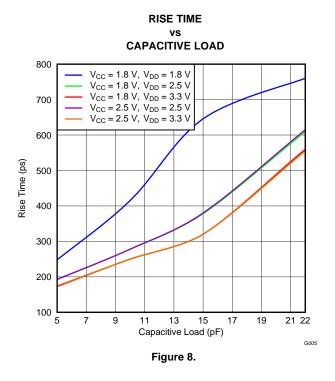


Figure 7.



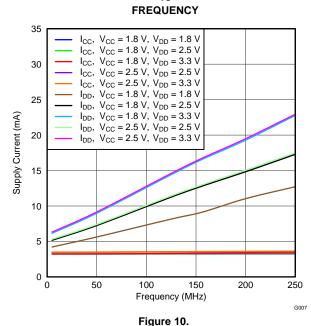
TYPICAL CHARACTERISTICS (continued)

VICM = 1.2 V, VID = 300 mV, C_L = 10 pF, input rise time and fall time = 1 ns, input frequency = 250 MHz, 50% duty cycle, T_A = 25°C, unless otherwise noted



FALL TIME vs **CAPACITIVE LOAD** 800 $V_{CC} = 1.8 \text{ V}, V_{DD} = 1.8 \text{ V}$ $V_{CC} = 1.8 \text{ V}, V_{DD} = 2.5 \text{ V}$ $V_{CC} = 1.8 \text{ V}, V_{DD} = 3.3 \text{ V}$ 700 $V_{CC} = 2.5 \text{ V}, \ V_{DD} = 2.5 \text{ V}$ $V_{CC} = 2.5 \text{ V}, \ V_{DD} = 3.3 \text{ V}$ 600 Fall Time (ps) 500 400 300 200 100 13 15 19 21 22 Capacitive Load (pF) G006 Figure 9.

SUPPLY CURRENT



SUPPLY CURRENT vs TEMPERATURE

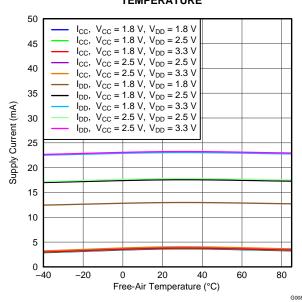


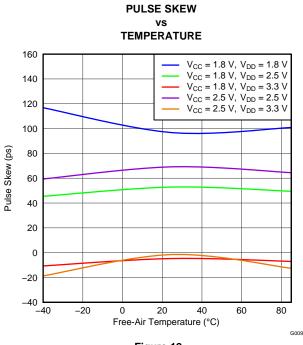
Figure 11.

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TYPICAL CHARACTERISTICS (continued)

VICM = 1.2 V, VID = 300 mV, $C_L = 10 \text{ pF}$, input rise time and fall time = 1 ns, input frequency = 250 MHz, 50% duty cycle, $T_A = 25^{\circ}C$, unless otherwise noted

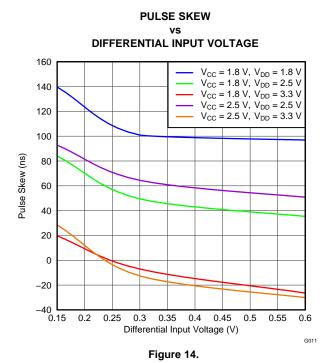


VS **COMMON-MODE VOLTAGE** 180 $V_{CC} = 1.8 \text{ V}, \ V_{DD} = 1.8 \text{ V}$ $V_{CC} = 1.8 \text{ V}, V_{DD} = 2.5 \text{ V}$ 160 $V_{CC} = 1.8 \text{ V}, V_{DD} = 3.3 \text{ V}$ $V_{CC} = 2.5 \text{ V}, V_{DD} = 2.5 \text{ V}$ 140 $V_{CC} = 2.5 \text{ V}, V_{DD} = 3.3 \text{ V}$ 120 100 Pulse Skew (ps) 80 60 40 20 0 -20**ــا** 0.15 0.45 0.75 1.05 1.65 Common-Mode Input Voltage (V) G010

PULSE SKEW

Figure 12.

Figure 13.



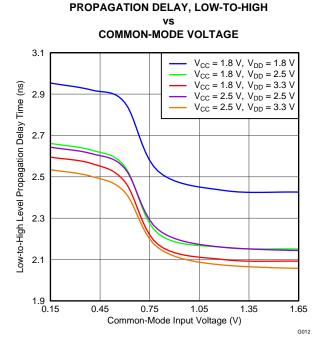


Figure 15.



TYPICAL CHARACTERISTICS (continued)

VICM = 1.2 V, VID = 300 mV, $C_L = 10 \text{ pF}$, input rise time and fall time = 1 ns, input frequency = 250 MHz, 50% duty cycle, $T_A = 25^{\circ}C$, unless otherwise noted

PROPAGATION DELAY, LOW-TO-HIGH **DIFFERENTIAL INPUT VOLTAGE** 2.7 $V_{CC} = 1.8 \text{ V}, V_{DD} = 1.8 \text{ V}$ $V_{CC} = 1.8 \text{ V}, V_{DD} = 2.5 \text{ V}$ 2.6 $V_{CC} = 1.8 \text{ V}, V_{DD} = 3.3 \text{ V}$ Low-to-High Level Propagation Delay Time (ns) $V_{CC} = 2.5 \text{ V}, V_{DD} = 2.5 \text{ V}$ $V_{CC} = 2.5 \text{ V}, V_{DD} = 3.3 \text{ V}$ 2.5 2.4 2.3 2.2 2.1 2 1.9 -0.2 0.25 0.3 0.35 0.4 0.45 0.55 0.6 Differential Input Voltage (V) G013

Figure 16.

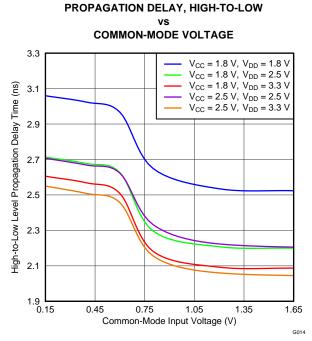
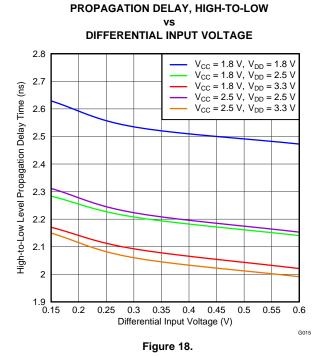
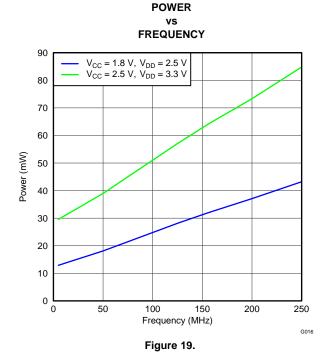


Figure 17.

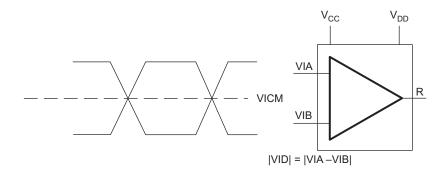




TEXAS INSTRUMENTS

APPLICATION INFORMATION

VIN_{MAX}



 $V_{CC2.5}$ (Note: Worst-Case VCC = 2.5 – 10% = 2.25 V)

VIA (V)	VIB (V)	VID (mV)	VICM (V)
1.25	1.2	50	1.225
1.2	1.25	50	1.225
2.2	2.25	50	2.225
2.25	2.2	50	2.225
0.05	0	50	0.025
0	0.05	50	0.025

 $V_{CC1.8}$ (Note: Worst-Case VCC = 1.8 – 10% =1.62 V)

VIA (V)	VIB (V)	VID (mV)	VICM (V)
1.25	1.2	50	1.225
1.2	1.25	50	1.225
1.57	1.62	50	1.595
1.62	1.57	50	1.595
0.05	0	50	0.025
0	0.05	50	0.025

 $V_{\text{CC2.5}}$ (Note: Worst-Case VCC = 2.5 – 10% = 2.25 V)

VIA (V)	VIB (V)	VID (mV)	VICM (V)
1.5	0.9	600	1.2
0.9	1.5	600	1.2
1.65	2.25	600	1.95
2.25	1.65	600	1.95
0.6	0	600	0.3
0	0.6	600	0.3

V_{CC1.8} (Note: Worst-Case VCC = 1.8 – 10% =1.62 V)

VIA (V)	VIB (V)	VID (mV)	VICM (V)
1.5	0.9	600	1.2
0.9	1.5	600	1.2
1.02	1.62	600	1.32
1.62	1.02	600	1.32
0.6	0	600	0.3
0	0.6	600	0.3

Figure 20. Maximum Input Voltage Combination Allowed

POWER SUPPLY

There are two power supplies in SN65LVDS4, VCC which is the core power supply and VDD which is the output drive power supply. For proper device operation it is recommended that VCC should be powered up first and then VDD or VCC applied at the same time as VDD (VCC and VDD tied together). It is also recommended that VCC should be equal to or less than VDD as shown in Table 3.

Table 3. Power Supply Acceptable Combinations

VCC (V)	VDD (V)	Recommended
1.8	1.8	yes
1.8	2.5	yes
1.8	3.3	yes
2.5	1.8	no
2.5	2.5	yes
2.5	3.3	yes



FAILSAFE

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –50 mV and 50 mV and within its recommended input common-mode voltage range.

Open circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, it is recommended to have an external failsafe solution as shown in Figure 21. In the external failsafe solution, the A side is pulled to V_{CC} via a weak pullup resistor and the B side is pulled down via a weak pulldown resistor. This creates a voltage offset and prevents the receiver from switching based on noise.

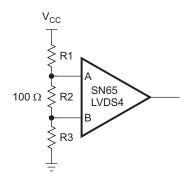


Figure 21. Open-Circuit Failsafe of the LVDS Receiver

R1 and R3 Calculation With VCC = 1.8 V

Assume that an external failsafe bias of 25 mV is desired

Bias current in this case is = 25 mV/100 Ω = 250 μ A

Next, determine the total resistance from VCC to ground = 1.8 V/250 μ A = 7.2 $k\Omega$

Keeping the common mode bias of 1.25 V to the receiver, the value of R3 = 1.25 V/250 μ A = 5 k Ω

Thus, R1 = $2.2 \text{ k}\Omega$

R1 and R3 Calculation With VCC = 2.5 V

Assume that an external failsafe bias of 25 mV is desired

Bias current in this case is = 25 mV/100 Ω = 250 μ A

Next, determine the total resistance from VCC to ground = 2.5 V/250 μ A = 10 k Ω

Keeping the common mode bias of 1.25 V to the receiver, the value of R3 = 1.25 V/250 μ A = 5 k Ω

Thus, R1 = $5 k\Omega$



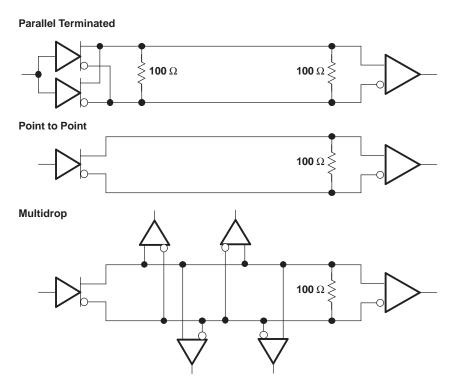


Figure 22. Typical Application Circuits



PACKAGE OPTION ADDENDUM

1-Aug-2011

PACKAGING INFORMATION

www.ti.com

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN65LVDS4RSER	ACTIVE	UQFN	RSE	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN65LVDS4RSET	ACTIVE	UQFN	RSE	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS4RSER	UQFN	RSE	10	3000	180.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1
SN65LVDS4RSET	UQFN	RSE	10	250	180.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1

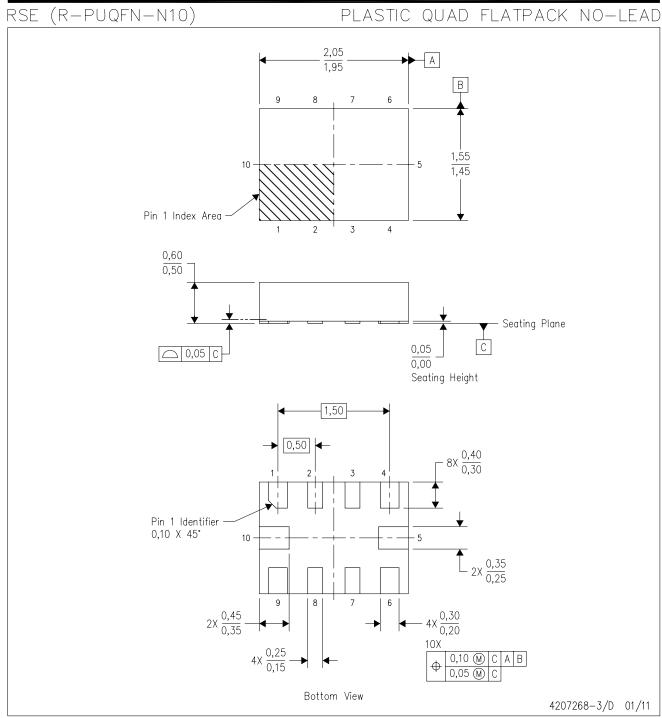
PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS4RSER	UQFN	RSE	10	3000	202.0	201.0	28.0
SN65LVDS4RSET	UQFN	RSE	10	250	202.0	201.0	28.0



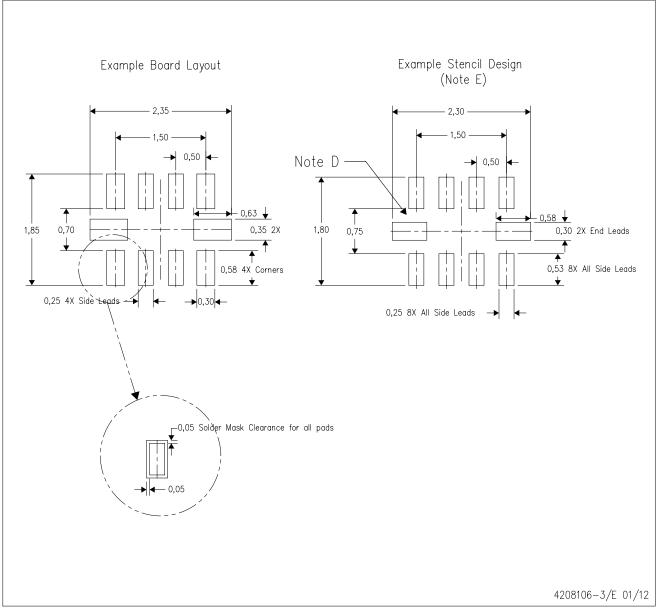
NOTES: All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
 C. QFN (Quad Flatpack No-Lead) package configuration.
 D. This package complies to JEDEC MO-288 variation UEFD.



RSE (R-PUQFN-N10)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



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