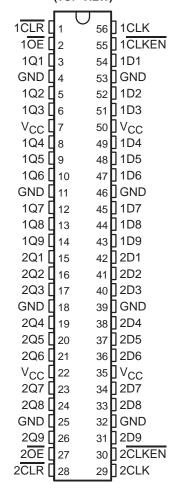
- Members of the Texas Instruments
   Widebus™ Family
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- High-Impedance State During Power Up and Power Down
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C
- Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Lavout
- High-Drive Outputs (-32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

#### description

These 18-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The 'ABT16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable (CLKEN) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high disables the clock buffer, latching the outputs. Taking the clear (CLR) input low causes the Q outputs to go low independently of the clock.

SN54ABT16823 . . . WD PACKAGE SN74ABT16823 . . . DGG OR DL PACKAGE (TOP VIEW)



A buffered output-enable ( $\overline{OE}$ ) input can be used to place the nine outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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## SN54ABT16823, SN74ABT16823 18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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## description (continued)

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

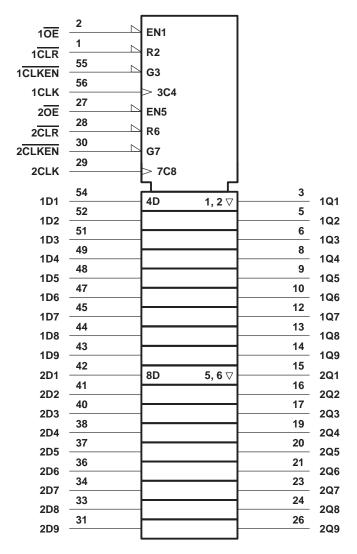
The SN54ABT16823 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to  $125^{\circ}$ C. The SN74ABT16823 is characterized for operation from  $-40^{\circ}$ C to  $85^{\circ}$ C.

FUNCTION TABLE (each 9-bit flip-flop)

		•		. ,	
		INPUTS			OUTPUT
OE	CLR	CLKEN	CLK	D	Q
L	L	Х	Χ	Х	L
L	Н	L	$\uparrow$	Н	Н
L	Н	L	$\uparrow$	L	L
L	Н	L	L	X	$Q_0$
L	Н	Н	Χ	Χ	Q <sub>0</sub> Q <sub>0</sub>
Н	Χ	Χ	Χ	Χ	Z

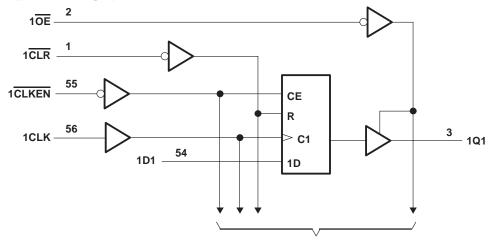


## logic symbol†

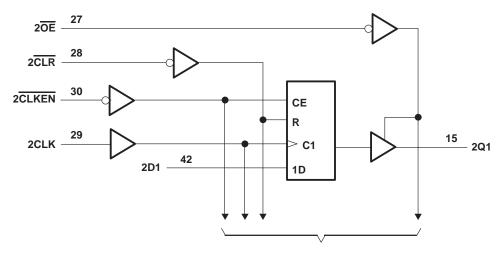


<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



To Eight Other Channels



**To Eight Other Channels** 

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V <sub>O</sub>	-0.5 V to 5.5 V
Current into any output in the low state, IO: SN54ABT16823	96 mA
SN74ABT16823	128 mA
Input clamp current, $I_{ K }(V_{ C } < 0)$	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T <sub>stq</sub>	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions (see Note 3)

			SN54AB1	Γ16823	SN74AB1	Γ16823	UNIT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V	
VIH	High-level input voltage	2		2		V	
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V	
VI	Input voltage	0	VCC	0	Vcc	V	
IOH	High-level output current			-24		-32	mA
loL	Low-level output current			48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		200		200		μs/V
T <sub>A</sub>	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

## SN54ABT16823, SN74ABT16823 18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS217C - JUNE 1992 - REVISED JANUARY 1997

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST	ONDITIONS	Т	A = 25°C	;	SN54AB	Γ16823	SN74AB1	16823	UNIT
PARAMETER	lesic	CNDITIONS	MIN	TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNII
VIK	$V_{CC} = 4.5 \text{ V},$	I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$	2.5			2.5		2.5		
VOH	$V_{CC} = 5 \text{ V}, \qquad I_{OH} = -3 \text{ mA}$		3			3		3		V
VOH	V <sub>CC</sub> = 4.5 V	$I_{OH} = -24 \text{ mA}$	2			2				V
	VCC = 4.5 V	$I_{OH} = -32 \text{ mA}$	2*					2		
VOL	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA			0.55		0.55			<b>\</b>
VOL	VCC = 4.5 V			0.55*				0.55	٧	
V <sub>hys</sub>				100						mV
Ц	$V_{CC} = 0 \text{ to } 5.5$ $V_{I} = V_{CC} \text{ or } G$				±1		±1		±1	μΑ
lozpu	$V_{CC} = 0 \text{ to } 2.1$ $V_{O} = 0.5 \text{ V to } 2$			±50		±50		±50	μΑ	
lozpd	$V_{CC} = 2.1 \text{ V to } 2.0 \text{ V}_{O} = 0.5 \text{ V to } 2.0 \text{ V}_{O} = 0.0  $			±50		±50		±50	μΑ	
lozh	V <sub>CC</sub> = 2.1 V to V <sub>O</sub> = 2.7 V, OE				10**		50		10	μΑ
lozL	$V_{CC} = 2.1 \text{ V} \text{ to}$ $V_{O} = 0.5 \text{ V}, \text{ OE}$	5.5 V, ≥ 2 V			-10**		<del>-</del> 50		-10	μА
l <sub>off</sub>	$V_{CC} = 0$ ,	$V_I$ or $V_O \le 4.5 \text{ V}$			±100				±100	μΑ
ICEX Outputs high	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 5.5 V			50		50		50	μΑ
IO <sup>‡</sup>	$V_{CC} = 5.5 \text{ V},$	$V_0 = 2.5 \text{ V}$	-50	-100	-200	-50	-200	-50	-200	mA
Outputs high					0.5		0.5		0.5	
I <sub>CC</sub> Outputs low	$V_{CC} = 5.5 \text{ V}, \text{ I}_{CC}$ $V_{I} = V_{CC} \text{ or GI}$				80		80		80	mA
Outputs disabled					0.5		0.5		0.5	
ΔICC§	V <sub>CC</sub> = 5.5 V, C Other inputs at	one input at 3.4 V, V <sub>CC</sub> or GND			1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.	5 V		3.5						pF
Co	$V_0 = 2.5 \text{ V or } 0$	).5 V		7.5						pF

<sup>\*</sup> On products compliant to MIL-PRF-38535, this parameter does not apply.



<sup>\*\*</sup> These limits apply only to the SN74ABT16823.

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>‡</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

# timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V <sub>CC</sub> =	= 5 V, 25°C	SN54AB1	Г16823	SN74AB1	Г16823	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
fclock	Clock frequency		0	150	0	150	0	150	MHz
	Pulse duration	CLR low	3.3		3.3		3.3		no
t <sub>W</sub>	ruise duration	CLK high or low	3.3		3.3		3.3		ns
		CLR inactive	1.6		2		1.6		
t <sub>su</sub>	Setup time before CLK↑	Data	1.7		1.7		1.7		ns
		CLKEN low	2.8		2.8		2.8		
<b>.</b>	Hold time after CLK↑	Data	1.2		1.2		1.2		
th	HOIG TIME AITER CLK	CLKEN low	0.6		0.6		0.6		ns

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

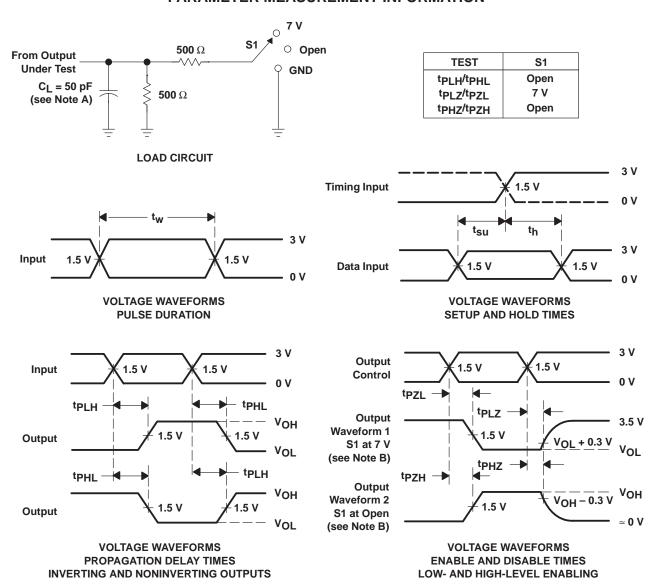
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>(</sub>	CC = 5 \ 4 = 25°C	/, ;	MIN	MAX	UNIT
f <sub>max</sub>			150			150		MHz
t <sub>PLH</sub>	CLK	Q	1.6	3.9	5.5	1.6	7.7	ns
t <sub>PHL</sub>	OLK	ď	2.1	3.9	5.4	2.1	6.4	113
<sup>t</sup> PHL	CLR	Q	1.9	4.1	5.3	1.9	6.3	ns
<sup>t</sup> PZH	ŌĒ	Q	1	3.1	4.2	1	5.1	20
t <sub>PZL</sub>	OE	ζ	1.5	3.5	4.6	1.5	5.7	ns
<sup>t</sup> PHZ	ŌĒ	Q	2.2	4.3	6	2.2	6.8	ne
<sup>t</sup> PLZ	OL .		1.6	4.3	6.4	1.6	9.9	ns

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

			SN74ABT16823					
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>(</sub>	CC = 5 V A = 25°C	<i>'</i> ,	MIN	MAX	UNIT
			MIN	TYP	MAX			
fmax			150			150		MHz
t <sub>PLH</sub>	CLK	Q	1.6	3.9	5.5	1.6	6.8	ns
<sup>t</sup> PHL		α	2.1	3.9	5.4	2.1	6	113
t <sub>PHL</sub>	CLR	Q	1.9	4.1	5.3	1.9	6.1	ns
<sup>t</sup> PZH	ŌĒ	Q	1	3.1	4.2	1	4.9	ns
t <sub>PZL</sub>	OE	ά	1.5	3.5	4.6	1.5	5.5	115
<sup>t</sup> PHZ	ŌĒ	Q	2.2	4.3	5.6	2.2	6.1	ne
t <sub>PLZ</sub>	OL .	ď	1.6	4.3	6.4	1.6	8.7	ns



#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_Q = 50 \ \Omega$ ,  $t_f \leq$  2.5 ns.  $t_f \leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms





5-Sep-2011

#### **PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-9584201QXA	ACTIVE	CFP	WD	56	1	TBD	Call TI	Call TI	
74ABT16823DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74ABT16823DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16823DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16823DGVR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16823DGVRE4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16823DGVRG4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16823DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16823DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16823DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT16823DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54ABT16823WD	ACTIVE	CFP	WD	56	1	TBD	A42	N / A for Pkg Type	

<sup>&</sup>lt;sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



### PACKAGE OPTION ADDENDUM

5-Sep-2011

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF SN54ABT16823, SN74ABT16823:

Catalog: SN74ABT16823

Military: SN54ABT16823

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

Military - QML certified for Military and Defense Applications



### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16823DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ABT16823DGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1
SN74ABT16823DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1





\*All dimensions are nominal

7 til dillionolorio aro nominal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16823DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74ABT16823DGVR	TVSOP	DGV	56	2000	346.0	346.0	41.0
SN74ABT16823DLR	SSOP	DL	56	1000	346.0	346.0	49.0

### WD (R-GDFP-F\*\*)

#### **CERAMIC DUAL FLATPACK**

#### **48 LEADS SHOWN**



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only
- E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA

GDFP1-F56 and JEDEC MO-146AB

## DGV (R-PDSO-G\*\*)

#### **24 PINS SHOWN**

#### **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194

### DL (R-PDSO-G\*\*)

#### **48 PINS SHOWN**

#### PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

#### **48 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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