SN54ALS273, SN74ALS273 OCTAL D-TYPE FLIP-FLOPS WITH CLEAR SDAS218A – APRIL 1982 – REVISED DECEMBER 1994

- Contain Eight Flip-Flops With Single-Rail Outputs
- Buffered Clock and Direct-Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications Include: Buffer/Storage Registers Shift Registers Pattern Generators
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

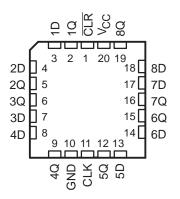
These octal positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct-clear (CLR) input.

Information at the data (D) inputs meeting the setup-time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input signal has no effect at the output.

The SN54ALS273 is characterized for operation over the full military temperature range of -55° C to 125°C. The SN74ALS273 is characterized for operation from 0°C to 70°C.

SN54ALS273 J PACKAGE SN74ALS273 DW OR N PACKAGE (TOP VIEW)						
	1 U	20] v _{cc}			
1Q [2	19	8Q			
1D 🛛	3	18	8D			
2D 🛛	4	17]7D			
2Q [5	16] 7Q			
3Q [6	15] 6Q			
3D [7	14] 6D			
4D 🛛	8	13	5D			
4Q [9	12] 5Q			
GND [10	11] CLK			

SN54ALS273 . . . FK PACKAGE (TOP VIEW)



FUNCTION TABLE	
(each flin-flon)	

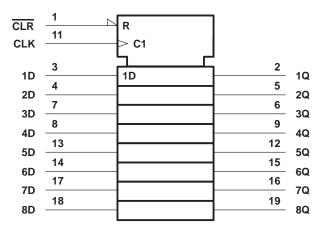
	INPUTS		OUTPUT
CLR	CLK	D	Q
L	Х	Х	L
н	\uparrow	Н	н
н	\uparrow	L	L
н	H or L	Х	Q ₀

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

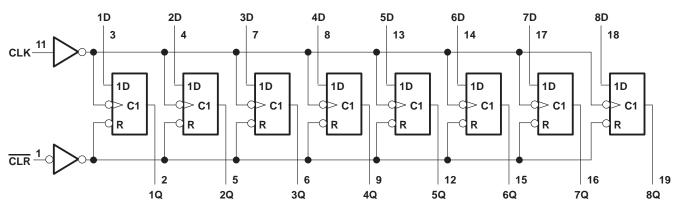
SN54ALS273, SN74ALS273 **OCTAL D-TYPE FLIP-FLOPS** WITH CLEAR

SDAS218A - APRIL 1982 - REVISED DECEMBER 1994

logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, V _{CC}	
Input voltage, V _I	
Operating free-air temperature range, T _A : SN54ALS273	
SN74ALS273	0°C to 70°C
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



recommended operating conditions

			SN	54ALS2	73	SN	74ALS2	73	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage		2			2			V
VIL	Low-level input voltage				0.7			0.8	V
ЮН	High-level output current				-1			-2.6	mA
IOL	Low-level output current				12			24	mA
fclock	Clock frequency		0		30	0		35	MHz
		CLR low	10			10			
tw	Pulse duration	CLK high	16.5			14			ns
		CLK low	16.5			14			
+		Data	10			10			ns
t _{su}	Setup time before CLK↑	CLR inactive state	15			15			115
t _h	Hold time, data after $CLK\uparrow$		0			0			ns
TA	Operating free-air temperature		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST O	SN	54ALS2	73	SN	73	UNIT		
FARAMETER	TEST CO	TEST CONDITIONS			MAX	MIN	TYP†	MAX	UNIT
VIK	V _{CC} = 4.5 V,	lj = -18 mA			-1.5			-1.5	V
	V_{CC} = 4.5 V to 5.5 V,	$I_{OH} = -0.4 \text{ mA}$	V _{CC} -2			V _{CC} -2			
VOH	V _{CC} = 4.5 V	$I_{OH} = -1 \text{ mA}$	2.4	3.3					V
	VCC = 4.5 V	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2		
Ve		I _{OL} = 12 mA		0.25	0.4		0.25	0.4	V
VOL	$V_{CC} = 4.5 V$	I _{OL} = 24 mA					0.35	0.5	v
lı	V _{CC} = 5.5 V,	V _I = 7 V			0.1			0.1	mA
ΙΗ	V _{CC} = 5.5 V,	VI = 2.7 V			20			20	μA
١	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.2			-0.2	mA
10 [‡]	V _{CC} = 5.5 V,	V _O = 2.25 V	-20		-112	-30		-112	mA
ІССН	V _{CC} = 5.5 V			11	20		11	20	mA
ICCL	V _{CC} = 5.5 V			19	29		19	29	mA

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. [‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.



SN54ALS273, SN74ALS273 OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

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switching characteristics (see Figure 1)

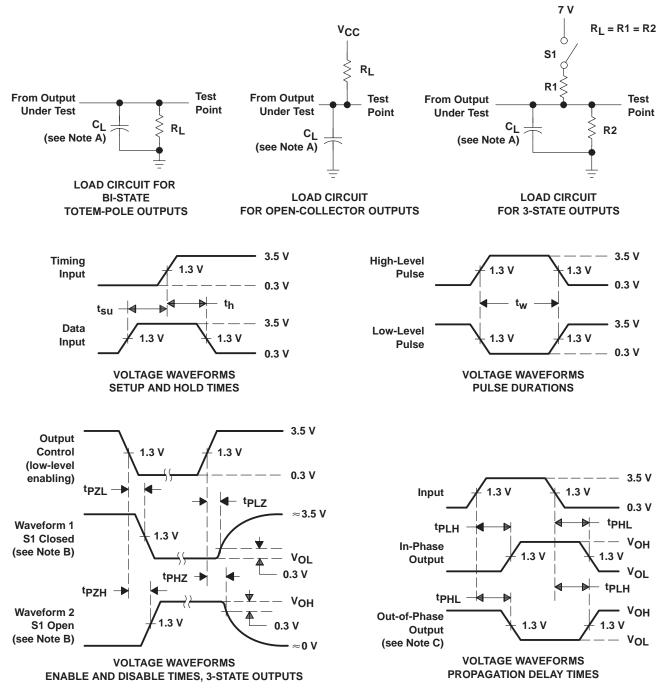
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _C CL RL TA	UNIT			
			SN54A	LS273	SN74ALS273		
			MIN	MAX	MIN	MAX	
fmax			30		35		MHz
^t PHL	CLR	Any Q	4	24	4	18	ns
tPLH	CLK	Δην.Ο	2	20	2	12	ns
^t PHL	CER	Any Q	3	17	3	15	115

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS273, SN74ALS273 OCTAL D-TYPE FLIP-FLOPS WITH CLEAR SDAS218A – APRIL 1982 – REVISED DECEMBER 1994

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR \leq 1 MHz, t_{f} = t_{f} = 2 ns, duty cycle = 50\%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms





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5-Sep-2011

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
84136012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
8413601RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	
8413601SA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	
SN54ALS273J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SN74ALS273DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS273DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS273DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS273DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS273DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS273DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS273N	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS273N3	OBSOLETE	PDIP	Ν	20		TBD	Call TI	Call TI	
SN74ALS273NE4	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS273NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS273NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS273NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54ALS273FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54ALS273J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SNJ54ALS273W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect. NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.



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5-Sep-2011

PREVIEW: Device has been announced but is not in production. Samples may or may not be available. **OBSOLETE:** TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and package die adhesive used between the die adhesive used between the die adhesive used between the die adhesive used betw

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54ALS273, SN74ALS273 :

• Catalog: SN74ALS273

• Military: SN54ALS273

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

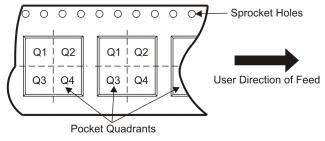
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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	-	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS273DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74ALS273NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1



PACKAGE MATERIALS INFORMATION

5-Aug-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS273DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74ALS273NSR	SO	NS	20	2000	346.0	346.0	41.0

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20



LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N**) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AC.



LAND PATTERN DATA



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0-10 Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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