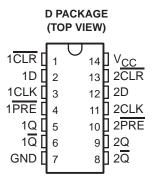
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- Controlled Baseline
 - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree[†]
- † Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- 4.5-V to 5.5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 10.5 ns at 5 V
- Inputs Are TTL-Voltage Compatible



description/ordering information

The SN74ACT74-EP is a dual positive-edge-triggered D-type flip-flop.

A low level at the preset (PRE) or clear (CLR) input sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at D can be changed without affecting the levels at the outputs.

ORDERING INFORMATION

TA	PACKAG	SE‡	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	SOIC - D	Tape and reel	SN74ACT74MDREP	SACT74MEP

[‡] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each flip-flop)

	INP	OUTI	PUTS		
PRE	CLR	CLK	D	Q	Q
L	Н	Х	Χ	Н	L
Н	L	X	Χ	L	Н
L	L	X	Χ	Н§	н§
Н	Н	\uparrow	Н	Н	L
Н	Н	\uparrow	L	L	Н
Н	Н	L	Χ	Q_0	\overline{Q}_0

[§] This configuration is nonstable; that is, it does not persist when either PRE or CLR returns to its inactive (high) level.



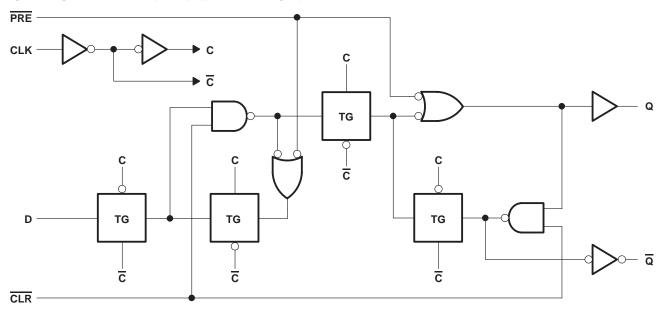
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SN74ACT74-EP DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

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logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	
Output voltage range, V _O (see Note 1)	0.5 V to V _{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	±200 mA
Package thermal impedance, θ_{JA} (see Note 2)	86°C/W
Storage temperature range, T _{stq} (see Note 3)	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. The package thermal impedance is calculated in accordance with JESD 51-7.
 - 3. Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.



SN74ACT74-EP DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
VI	Input voltage	0	VCC	V
VO	Output voltage	0	VCC	V
ЮН	High-level output current		-24	mA
loL	Low-level output current		24	mA
Δt/Δν	Input transition rise or fall rate		8	ns/V
TA	Operating free-air temperature	-55	125	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEST COMPITIONS	,,	T	A = 25°C	;	BAIN!	BAAV		
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	UNIT	
	1 50 A	4.5 V	4.4	4.49		4.4			
.,,	I _{OH} = -50 μA	5.5 V	5.4	5.49		5.4			
VOH	04.004	4.5 V	3.86			3.7		V	
	$I_{OH} = -24 \text{ mA}$	5.5 V	4.86			4.7			
	4.5 V			0.001	0.1		0.1		
.,	I _{OL} = 50 μA	5.5 V		0.001	0.1		0.1	V	
VOL		4.5 V			0.36		0.5		
	I _{OL} = 24 mA	5.5 V			0.36		0.5		
I _I	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μΑ	
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		40	μΑ	
ΔlCC [†]	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V		0.6			1.6	mA	
Ci	$V_I = V_{CC}$ or GND	5 V		3				pF	

[†] This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or VCC.

timing characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

				25°C		BAAY	
			MIN	MAX	MIN	MAX	UNIT
fclock	Clock frequency			145		85	MHz
	Delega describes	PRE or CLR low	5		7		
t _W	Pulse duration	CLK	5		7		ns
		Data	3		4	4	
t _{su}	Setup time, data before CLK↑ PRE or CLF		0		0.5		ns
th	Hold time, data after CLK↑		1		1		ns



SN74ACT74-EP DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

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switching characteristics over recommended operating free-air temperature (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	T,	_Δ = 25°C	;	BAINI		
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNIT
f _{max}			145	210		85		MHz
^t PLH	PRE or CLR	0	1	5.5	9.5	1	11.5	
^t PHL	PRE OF CLR	Q or Q	1	6	10	1	12.5	ns
^t PLH	CLK	0.010	1	7.5	11	1	14	20
^t PHL	OLK .	Q or Q	1	6	10	1	12	ns

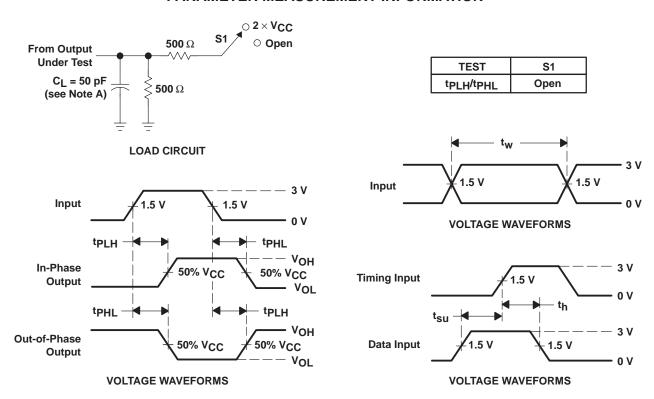
operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	C _L = 50 pF, f = 1 MHz	45	pF



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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_Q = 50~\Omega$, $t_f \leq 2.5~\text{ns}$, $t_f \leq 2.5~\text{ns}$.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms





i.com 18-Sep-2008

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins F	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74ACT74MDREP	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04725-01XE	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74ACT74-EP:

Catalog: SN74ACT74Military: SN54ACT74

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications



TAPE AND REEL INFORMATION





_		
	A0	Dimension designed to accommodate the component width
Γ	B0	Dimension designed to accommodate the component length
		Dimension designed to accommodate the component thickness
	W	Overall width of the carrier tape
Γ	P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT74MDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1





*All dimensions are nominal

ĺ	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
	SN74ACT74MDREP	SOIC	D	14	2500	333.2	345.9	28.6

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