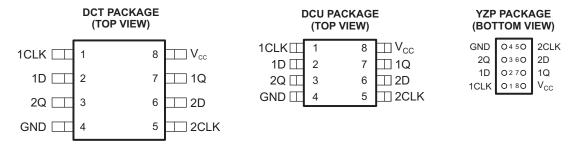
SCES536C-DECEMBER 2003-REVISED JANUARY 2007

FEATURES

- Available in the Texas Instruments
 NanoFree™ Package
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial Power-Down-Mode Operation
- Sub-1-V Operable

- Max t_{nd} of 1.9 ns at 1.8 V
- Low Power Consumption, 10-μA Max I_{CC}
- ±8-mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This single positive-edge-triggered D-type flip-flop is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

When data at the data (D) input meets the setup time requirement, the data is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽²⁾
	NanoFree [™] – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUC2G79YZPR	UR_
-40°C to 85°C	SSOP - DCT	Reel of 3000	SN74AUC2G79DCTR	U79
	VSSOP - DCU	Reel of 3000	SN74AUC2G79DCUR	U79_

⁽¹⁾ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

⁽²⁾ DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site. DCU: The actual top-side marking has one additional character that designates the assembly/test site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

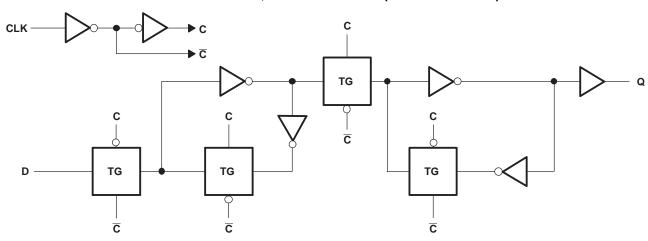
NanoFree is a trademark of Texas Instruments.



FUNCTION TABLE

INPU	JTS	OUTPUT
CLK	D	Q
1	Н	Н
\uparrow	L	L
L	X	Q_0

LOGIC DIAGRAM, EACH FLIP-FLOP (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
V _{CC}	Supply voltage range		-0.5	3.6	V	
VI	Input voltage range ⁽²⁾		-0.5	3.6	V	
Vo	Voltage range applied to any output in the h	nigh-impedance or power-off state ⁽²⁾	-0.5	3.6	V	
Vo	Output voltage range ⁽²⁾		-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < 0		-50	mA	
I _{OK}	Output clamp current	utput clamp current $V_O < 0$		-50	mA	
Io	Continuous output current			±20	mA	
	Continuous current through V _{CC} or GND			±100	mA	
		DCT package		220		
θ_{JA}	Package thermal impedance (3)	DCU package		227	°C/W	
		YZP package		102		
T _{stg}	Storage temperature range		-65	150	°C	

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

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Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		0.8	2.7	V
		V _{CC} = 0.8 V	V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		
		V _{CC} = 0.8 V		0	
V _{IL} Lov	Low-level input voltage	V _{CC} = 1.1 V to 1.95 V		$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	
V_{I}	Input voltage		0	3.6	V
V_{O}	Output voltage		0	V_{CC}	V
		V _{CC} = 0.8 V		-0.7	
		V _{CC} = 1.1 V		-ვ	
I_{OH}	High-level output current	V _{CC} = 1.4 V		-5	mA
		V _{CC} = 1.65 V		-8	
		V _{CC} = 2.3 V		-9	
		V _{CC} = 0.8 V		0.7	
		V _{CC} = 1.1 V		3	
I_{OL}	Low-level output current	V _{CC} = 1.4 V		5	mA
		V _{CC} = 1.65 V		8	
		V _{CC} = 2.3 V		9	
		$V_{CC} = 0.8 \text{ V to } 1.65 \text{ V}^{(2)}$		20	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.65 \text{ V to } 2.3 \text{ V}^{(3)}$		20	ns/V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}^{(3)}$		20	
T _A	Operating free-air temperature		-40	85	°C

 ⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.
 (2) The data was taken at C_L = 15 pF, R_L = 2 kΩ (see Figure 1).
 (3) The data was taken at C_L = 30 pF, R_L = 500 Ω (see Figure 1).

SN74AUC2G79 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES536C-DECEMBER 2003-REVISED JANUARY 2007



Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	MIN TYP ⁽¹⁾	MAX	UNIT
	$I_{OH} = -100 \mu A$	0.8 V to 2.7 V	V _{CC} - 0.1		
	$I_{OH} = -0.7 \text{ mA}$	0.8 V	0.55		
V	$I_{OH} = -3 \text{ mA}$	1.1 V	0.8		V
V _{OH}	$I_{OH} = -5 \text{ mA}$	1.4 V	1		V
	$I_{OH} = -8 \text{ mA}$	1.65 V	1.2		
	$I_{OH} = -9 \text{ mA}$	2.3 V	1.8		
	I _{OL} = 100 μA	0.8 V to 2.7 V		0.2	
	I _{OL} = 0.7 mA	0.8 V	0.25		
V	I _{OL} = 3 mA	1.1 V		0.3	V
V _{OL}	I _{OL} = 5 mA	1.4 V		0.4	V
	I _{OL} = 8 mA	1.65 V		0.45	
	I _{OL} = 9 mA	2.3 V		0.6	
I _I D or CLK inputs	$V_I = V_{CC}$ or GND	0 to 2.7 V		±5	μΑ
I _{off}	V_1 or $V_0 = 2.7 \text{ V}$	0		±10	μΑ
I _{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	0.8 V to 2.7 V		10	μΑ
Ci	$V_I = V_{CC}$ or GND	2.5 V	2.5		pF

⁽¹⁾ All typical values are at $T_A = 25$ °C.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC} = 0.8 V	V _{CC} = ± 0.	1.2 V 1 V	V _{CC} = ± 0.	1.5 V 1 V	V _{CC} = ± 0.7	1.8 V 15 V	V _{CC} = ± 0.		UNIT
		TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	50		200		225		250		275	MHz
t _w	Pulse duration, CLK high or low	2.4	1		1		1		1		ns
t _{su}	Setup time before CLK↑	1.6	0.9		0.6		0.6		0.5		ns
t _h	Hold time, data after CLK↑	0	0		0		0.1		0.1		ns

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM TO (INPUT) (OUTPUT)		V _{CC} = 0.8 V	V _{CC} = ± 0.		V _{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V			V _{CC} = 2.5 V ± 0.2 V		UNIT
	(INPOT)	(001701)	TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
f _{max}			50	200		225		250			275		MHz
t _{pd}	CLK	Q	5	1	3.9	0.8	2.5	0.3	1	1.9	0.3	1.3	ns

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _C	V _{CC} = 1.8 V ± 0.15 V			V _{CC} = 2.5 V ± 0.2 V	
	(INFOI)	(001F01)	MIN	TYP	MAX	MIN	MAX	
f _{max}			250			275		ns
t _{pd}	CLK	Q	0.8	1.5	2.4	0.6	1.8	ns



SN74AUC2G79 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES536C-DECEMBER 2003-REVISED JANUARY 2007

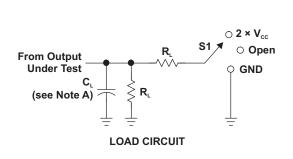
Operating Characteristics

 $T_A = 25^{\circ}C$

PARAMETER		TEST	$V_{CC} = 0.8 \text{ V}$	V _{CC} = 1.2 V	V _{CC} = 1.5 V	V _{CC} = 1.8 V	V _{CC} = 2.5 V	UNIT	
			CONDITIONS	TYP	TYP	TYP	TYP	TYP	
		Data		16	16.2	18	19.8	29.2	
C_{pd}	C _{pd} Power dissipation capacitance	CLK	f = 10 MHz	1.1	1.1	1.2	1.5	2.7	pF
Capacitance	oapaonanoo	Total		17.1	17.3	19.2	21.3	31.9	

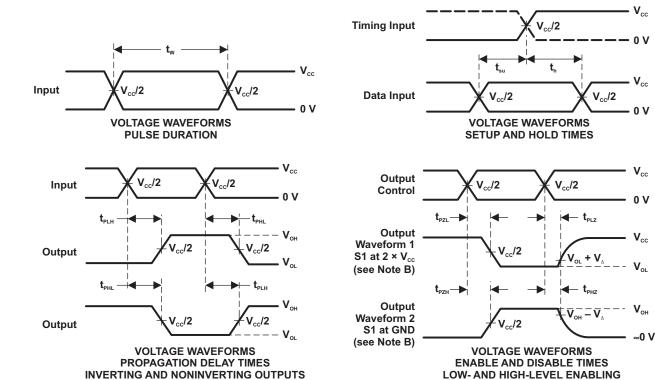


PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{PLH} /t _{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V _{cc}
$t_{_{PHZ}}/t_{_{PZH}}$	GND

V _{cc}	C _∟	R _∟	V _Δ
0.8 V	15 pF	2 k Ω	0.1 V
1.2 V ± 0.1 V	15 pF	2 k Ω	0.1 V
1.5 V ± 0.1 V	15 pF	2 k Ω	0.1 V
1.8 V ± 0.15 V	15 pF	2 k Ω	0.15 V
$2.5~V~\pm~0.2~V$	15 pF	2 k Ω	0.15 V
1.8 V ± 0.15 V	30 pF	1 k Ω	0.15 V
2.5 V ± 0.2 V	30 pF	500 Ω	0.15 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_o = 50 Ω , slew rate \geq 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. $t_{\text{\tiny PLZ}}$ and $t_{\text{\tiny PHZ}}$ are the same as $t_{\text{\tiny dis}}$
- F. $t_{\mbox{\tiny PZL}}$ and $t_{\mbox{\tiny PZH}}$ are the same as $t_{\mbox{\tiny en}}.$
- G. $t_{Pl\,H}$ and t_{PHl} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms





com 15-Sep-2008

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AUC2G79DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G79DCTRE4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G79DCTRG4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G79DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G79DCURE4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G79DCURG4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G79YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC2G79DCUR	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G79YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC2G79DCUR	US8	DCU	8	3000	202.0	201.0	28.0
SN74AUC2G79YZPR	DSBGA	YZP	8	3000	220.0	220.0	34.0

DCT (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. Falls within JEDEC MO-187 variation DA.

DCT (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



NOTES:

- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-187 variation CA.



DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



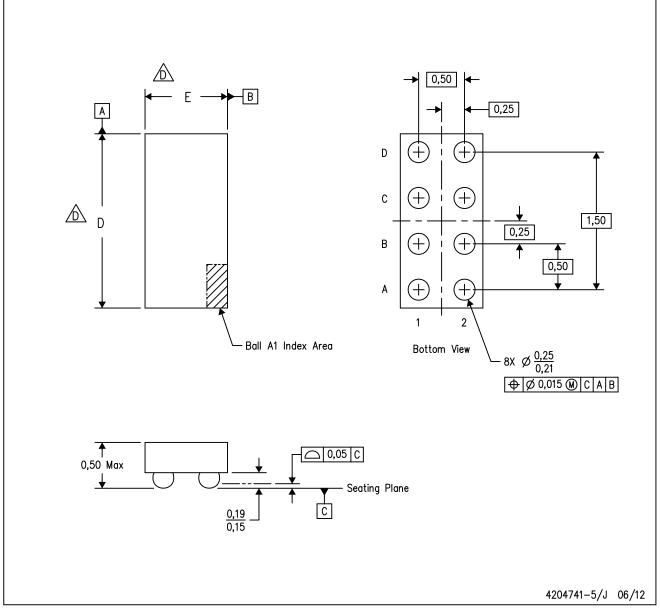
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



NOTES: All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- This drawing is subject to change without notice.
- Ç. NanoFree™ package configuration.
- ⚠ The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative. E. This package is a Pb-free solder ball design. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

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