

SCES038F-JULY 1995-REVISED APRIL 2005

FEATURE	S
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- Member of the Texas Instruments Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

DESCRIPTION

This 18-bit bus-interface flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16823 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The SN74ALVCH16823 can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable (CLKEN) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking CLKEN high disables the clock buffer, thus latching the outputs. Taking the clear (CLR) input low causes the Q outputs to go low independently of the clock.

(TOP VIEW)										
1CLR	$_{1}$ U	56]1CLK							
	2	55	1 1 CLKEN							
1Q1 [3	54	1D1							
GND [4	53] GND							
1Q2 [5	52	1D2							
1Q3 [6	51]1D3							
V _{CC}	7	50]V _{CC}							
1Q4 [8	49]1D4							
1Q5 🛛	9	48]1D5							
1Q6 🛛	10	47	1D6							
GND [11	46] GND							
1Q7 [12	45	1D7							
1Q8	13	44	1D8							
1Q9 [14	43	1D9							
2Q1 [15	42	2D1							
2Q2 [16	41	2D2							
2Q3 [17	40	2D3							
GND [18	39	GND							
2Q4 [19	38	2D4							
2Q5 [20	37	2D5							
2Q6 _	21	36	2D6							
Vcc	22	35	V _{CC}							
2Q7 [23	34	2D7							
2Q8 [24	33	2D8							
GND [25	32	GND							
2Q9	26	31	2D9							
20E	27	30	2CLKEN							
2CLR	28	29	2CLK							

DGG OR DL PACKAGE

A buffered output-enable (\overline{OE}) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (OE) input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16823 is characterized for operation from -40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet. Widebus, EPIC are trademarks of Texas Instruments.

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FUNCTION TABLE (each 9-bit flip-flop)

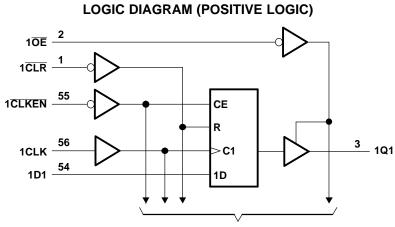
	INPUTS							
OE	CLR	CLKEN	CLK	D	Q			
L	L	Х	Х	Х	L			
L	Н	L	\uparrow	Н	Н			
L	Н	L	\uparrow	L	L			
L	Н	L	L	Х	Q ₀			
L	н	Н	Х	Х	Q ₀			
Н	Х	Х	Х	Х	Z			

	•			
10E	2			
1CLR	1	R2		
1CLKEN	55	G3		
1CLK	56	——————————————————————————————————————		
2OE	27	EN5		
2CLR	28	R6		
2CLKEN	30	G7		
2CLK	29			
LOLIX	54			3
1D1	52	4D	1, 2 ⊽ –	5
1D2				
1D3	51 49			6
1D4			_	8
1D5	48		_	9
1D6	47		_	10
1D7	45		_	12
1D8	44			13
1D9	43			14
2D1	42		5,6 ▽ -	15
2D2	41			16
2D3	40			17
2D4	38			19
2D5	37			20
2D6	36			21
2D7	34			23
2D8	33			24
2D9	31			26

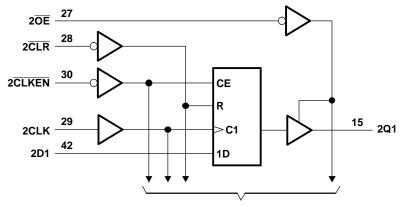
LOGIC SYMBOL⁽¹⁾

(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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To Eight Other Channels



To Eight Other Channels

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range	Supply voltage range			V
VI	Input voltage range ⁽²⁾		-0.5	4.6	V
Vo	Output voltage range ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current V _O < 0			-50	mA
I _O	Continuous output current	Continuous output current			
	Continuous current through V_{CC} or GND			±100	mA
0	Decline the stand interval (4)	DGG package		81	°C/W
θ_{JA}	Package thermal impedance ⁽⁴⁾	DL package		74	
T _{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) This value is limited to 4.6 V maximum.

(4) The package thermal impedance is calculated in accordance with JESD 51.

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Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		1.65	3.6	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		
V _{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
V _{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
VI	Input voltage		0	V _{CC}	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 1.65 V		-4	
	The large stand and a sum of	V _{CC} = 2.3 V	-12 -12		mA
I _{OH}	High-level output current	$V_{CC} = 2.7 V$			
	$\label{eq:constraint} \begin{split} V_{\text{IL}} & \text{Low-level input voltage} & \begin{array}{c} V_{\text{CC}} = 1.65 \text{ V to } 1.95 \text{ V} \\ \overline{V_{\text{CC}}} = 2.3 \text{ V to } 2.7 \text{ V} \\ \overline{V_{\text{CC}}} = 2.3 \text{ V to } 2.7 \text{ V} \\ \overline{V_{\text{CC}}} = 2.7 \text{ V to } 3.6 \text{ V} \\ \end{array} \\ \hline \\ \hline \\ V_{\text{O}} & \text{Output voltage} & \end{array} \\ \hline \\ \hline \\ OH & \begin{array}{c} W_{\text{OL}} = 1.65 \text{ V} \\ \overline{V_{\text{CC}}} = 2.3 \text{ V} \\ \overline{V_{\text{CC}}} = 2.3 \text{ V} \\ \overline{V_{\text{CC}}} = 2.3 \text{ V} \\ \overline{V_{\text{CC}}} = 2.7 \text{ V} \\ \overline{V_{\text{CC}}} = 3 \text{ V} \\ \end{array} \\ \hline \\ \hline \\ V_{\text{CC}} = 3 \text{ V} \\ \hline \\ \overline{V_{\text{CC}}} = 2.3 \text{ V} \\ \overline{V_{\text{CC}}} = 2.3 \text{ V} \\ \hline \\ \overline{V_{\text{CC}}} = 2.7 \text{ V} \\ \hline \\ \overline{V_{\text{CC}}} = 2.3 \text{ V} \\ \hline \\ \overline{V_{\text{CC}}} = 2.3 \text{ V} \\ \hline \\ \overline{V_{\text{CC}}} = 2.3 \text{ V} \\ \hline \\ \overline{V_{\text{CC}}} = 2.7 \text{ V} \\ \hline \\ \overline{V_{\text{CC}}} = 2.7 \text{ V} \\ \hline \\ \overline{V_{\text{CC}}} = 2.3 \text{ V} \\ \hline \\ \overline{V_{\text{CC}}} = 3 \text{ V} \\ \hline \\ \overline{V_{\text{CC}}} = 3 \text{ V} \\ \hline \end{array} \\ \hline \end{array} $		-24		
		V _{CC} = 1.65 V		4	
		$V_{CC} = 2.3 V$		12	
I _{OL}	Low-level output current	V _{CC} = 2.7 V	12		mA
		$V_{CC} = 3 V$		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T _A	Operating free-air temperature		-40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	MIN TYP ⁽¹⁾	MAX	UNIT		
	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} - 0.2				
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2				
	I _{OH} = -6 mA	2.3 V	2				
V _{OH}		2.3 V	1.7		V		
	I _{OH} = -12 mA	2.7 V	2.2				
		3 V	2.4				
	I _{OH} = -24 mA	3 V	2				
	I _{OL} = 100 μA	1.65 V to 3.6 V		0.2			
	I _{OL} = 4 mA	1.65 V		0.45			
N/	I _{OL} = 6 mA	2.3 V		0.4	V		
	40	2.3 V		0.7			
	$I_{OL} = 12 \text{ mA}$	2.7 V		0.4			
	I _{OL} = 24 mA	3 V		0.55			
l _l	$V_{I} = V_{CC}$ or GND	3.6 V		±5	μA		
	V _I = 0.58 V	1.65 V	25				
	V _I = 1.07 V	1.65 V	-25				
	V _I = 0.7 V	2.3 V	45				
I _{I(hold)}	V _I = 1.7 V	2.3 V	-45		μA		
	V _I = 0.8 V	3 V	75				
	V ₁ = 2 V	3 V	-75				
	V ₁ = 0 to 3.6 V ⁽²⁾	3.6 V		±500			
I _{oz}	$V_0 = V_{CC}$ or GND	3.6 V		±10	μA		
I _{CC}	$V_{I} = V_{CC} \text{ or } GND, \qquad I_{O} = 0$	3.6 V		40	μA		
Δl _{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V		750	μA		
Control inputs	V = V or CND	2.2.1/	4.5	4.5 6.5			
C _i Data inputs	$V_{I} = V_{CC} \text{ or } GND$	3.3 V	6.5				
C _o Outputs	$V_{O} = V_{CC}$ or GND	3.3 V	7		pF		

(1) (2)

All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

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Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

			V _{CC} =	V _{CC} = 1.8 V		2.5 V 2 V	V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency			(1)		150		150		150	MHz
t _w Pulse duration	CLR low	(1)		3.3		3.3		3.3			
	Pulse duration	CLK high or low	(1)		3.3		3.3		3.3		ns
	0.4.4	CLR inactive	(1)		0.7		0.7		0.8		
		Data low before CLK [↑]	(1)		1.6		1.6		1.3		ns
t _{su}	Setup time	Daa high before CLK↑	(1)		1.1		1.1		1		
		CLKEN low before CLK [↑]	(1)		1.9		1.9		1.5		
		Data low after CLK1	(1)		0.5		0.5		0.5		
t _h	Hold time	Data high after CLK↑	(1)		0.1		0.1		0.8		ns
		CLKEN low after CLK [↑]	(1)		0.3		0.3		0.4		

(1) This information was not available at the time of publication.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} =	1.8 V	V _{CC} = ± 0.2	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} = 3 ± 0.3	3.3 V 3 V	UNIT
	(INFUT)	(001201)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			(1)		150		150		150		MHz
+	CLK	Q		(1)	1	5.8		5.2	1	4.5	20
Lpd	CLR	Q		(1)	1	5.4		5.2	1.2	4.6	ns
t _{en}	OE	Q		(1)	1	6		5.7	1	4.8	ns
t _{dis}	OE	Q		(1)	1.1	5.4		4.7	1.3	4.5	ns

(1) This information was not available at the time of publication.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted), V_{CC} = 3.3 ± 0.3 V, C_L = 30 pF, R_L = 500 Ω

PARAMETER	FROM	то	V _{CC} = 3.3 V ±	UNIT		
FARAMETER	(INPUT) (OUTPUT)		MIN	MAX	UNIT	
f _{max} ⁽¹⁾			250		MHz	
+	CLK	Q	1	3.5	2	
۲pd	CLR	Q	1.2	4.1	ns	
t _{en}	ŌĒ	Q	1	3.8	ns	
t _{dis}	ŌĒ	Q	1.3	4.5	ns	
t _{sk(o)} ⁽¹⁾				0.5	ns	

(1) Values are characterized but not production tested.

Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT
<u> </u>	Power dissipation	Outputs enabled		(1)	27	30	" Г
Cpd	capacitance	Outputs disabled	$C_{L} = 50 \text{ pF}, \text{ f} = 10 \text{ MHz}$	(1)	16	18	р⊢

(1) This information was not available at the time of publication.

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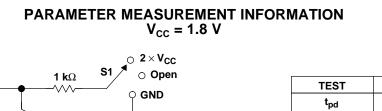
From Output

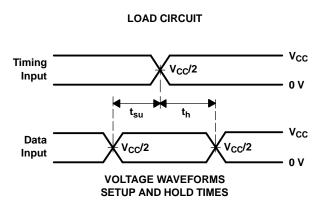
Under Test

 $C_L = 30 \, pF$

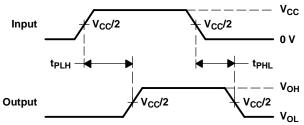
(see Note A)





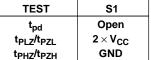


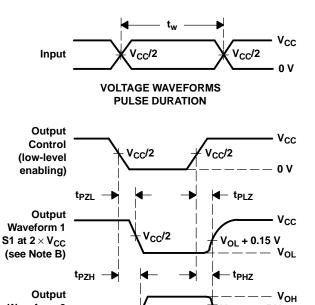
1 kΩ



VOLTAGE WAVEFORMS

PROPAGATION DELAY TIMES







Vcc/2

V_{OH} – 0.15 V

0 V

ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.

Waveform 2

(see Note B)

S1 at GND

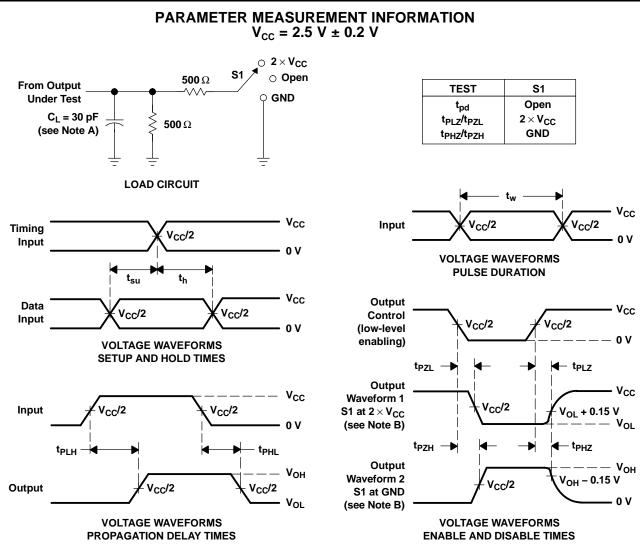
- Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_r \leq 2 ns, t_f \leq 2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. $t_{PLH} \, \text{and} \, t_{PHL}$ are the same as $t_{pd}.$

Figure 1. Load Circuit and Voltage Waveforms

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SN74ALVCH16823 18-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS

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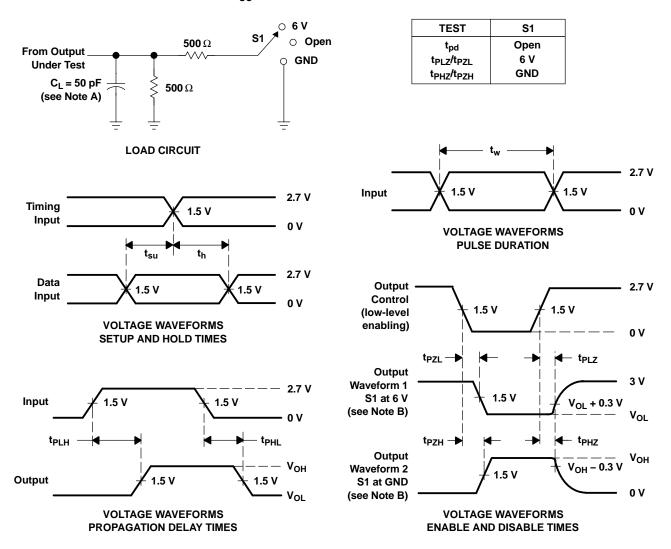
- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION V_{cc} = 2.7 V AND 3.3 V ± 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_r \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

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19-Apr-2010

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ALVCH16823DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16823DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16823DGVRE4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16823DGVRG4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16823DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16823DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16823DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16823DGVR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16823DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16823DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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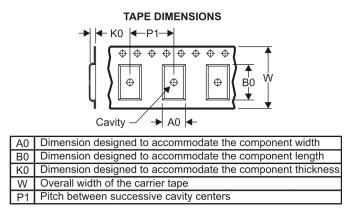
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH16823DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ALVCH16823DGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1
SN74ALVCH16823DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

19-Apr-2010



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH16823DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74ALVCH16823DGVR	TVSOP	DGV	56	2000	346.0	346.0	41.0
SN74ALVCH16823DLR	SSOP	DL	56	1000	346.0	346.0	49.0

MECHANICAL DATA

PLASTIC SMALL-OUTLINE

MPDS006C - FEBRUARY 1996 - REVISED AUGUST 2000

DGV (R-PDSO-G**)

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins MO-153

14/16/20/56 Pins – MO-194



MECHANICAL DATA

MSSO001C - JANUARY 1995 - REVISED DECEMBER 2001

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

DL (R-PDSO-G**)



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118



MECHANICAL DATA

MTSS003D - JANUARY 1995 - REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



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