

FEATURES

- Member of the Texas Instruments Widebus™ Family
- **EPIC™** (Enhanced-Performance Implanted **CMOS) Submicron Process**
- ESD Protection Exceeds 2000 V Per MIL-STD-883. Method 3015: Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

DESCRIPTION

This 20-bit flip-flop is designed specifically for 1.65-V to 3.6-V V_{CC} operation.

The 20 flip-flops of the SN74ALVCH16721 are edge-triggered D-type flip-flops with gualified clock storage. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs if the clock-enable (CLKEN) input is low. If CLKEN is high, no data is stored.

A buffered output-enable (\overline{OE}) input places the 20 outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components. OE does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

<u> OE</u>	1	56]сгк
Q1 [2	55	D1
Q2 [3	54] D2
GND [4	53	GND
Q3 [5	52] D3
Q4 [6	51] D4
V _{CC} [7	50]v _{cc}
Q5 [8	49] D5
Q6 [9	48	D6
Q7 [10	47] D7
GND 🛛	11	46] GND
Q8 [12	45] D8
Q9 [13	44] D9
Q10 🛛	14	43	D10
Q11 [15	42	D11
Q12 🛛	16	41	D12
Q13 [17	40	D13
GND 🛛	18	39] GND
Q14 🛛	19	38	D14
Q15 🛛	20	37	D15
Q16 🛛	21	36	D16
V _{CC}	22	35	V _{cc}
Q17 [23	34	D17
Q18	24	33	D18
GND	25	32	GND
Q19 🛛	26	31	D19
Q20 [27	30	D20
NC 🛛	28	29	CLKEN

DGG, DGV, OR DL PACKAGE

(TOP VIEW)

NC - No internal connection

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16721 is characterized for operation from -40°C to 85°C.



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SCES052E-JULY 1995-REVISED AUGUST 2004



FUNCTION TABLE (each flip-flop)

	OUTPUT			
OE	CLKEN	CLK	D	Q
L	Н	Х	Х	Q ₀
L	L	\uparrow	Н	н
L	L	\uparrow	L	L
L	L	L or H	Х	Q ₀
н	Х	х	Х	z

LOGIC DIAGRAM (POSITIVE LOGIC)



To 19 Other Channels



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	4.6	V
VI	Input voltage range ⁽²⁾	-0.5	4.6	V	
Vo	Output voltage range ⁽²⁾⁽³⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{ок}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current	•		±50	mA
	Continuous current through each V_{CC} or GND			±100	mA
		DGG package		81	
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGV package		86	°C/W
		DL package		74	
T _{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) This value is limited to 4.6 V maximum.

(4) The package thermal impedance is calculated in accordance with JESD 51.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		1.65	3.6	V
		V _{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		
VIH	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		V _{CC} = 1.65 V to 1.95 V		$0.35\times V_{CC}$	
V _{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
		V _{CC} = 2.7 V to 3.6 V		0.8	1
VI	Input voltage		0	V _{CC}	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 1.65 V		-4	
.	Lich lovel output ourrent	V _{CC} = 2.3 V		-12	
юн	High-level output current	$V_{CC} = 2.7 V$		-12	
		$V_{CC} = 3 V$		-24	
		V _{CC} = 1.65 V		4	
.		$V_{CC} = 2.3 V$		12	m ^
'OL	Low-level output current	$V_{CC} = 2.7 V$		12	I IIA
		$V_{CC} = 3 V$		24	
Δt/Δv	Input transition rise or fall rate			10	ns/V
T _A	Operating free-air temperature		-40	85	°C

 All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾ MAX	UNIT
		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} - 0.2		
		I _{OH} = -4 mA	1.65 V	1.2		
		I _{OH} = -6 mA	2.3 V	2		
V _{OH}			2.3 V	1.7		V
		I _{OH} = -12 mA	2.7 V	2.2		
			3 V	2.4		
		I _{OH} = -24 mA	3 V	2		
		I _{OL} = 100 μA	1.65 V to 3.6 V		0.2	
		I _{OL} = 4 mA	1.65 V		0.45	
		I _{OL} = 6 mA	2.3 V		0.4	
VOL		1 12 12	2.3 V		0.7	v
		$I_{OL} = 12 \text{ IIIA}$	2.7 V		0.4	
		I _{OL} = 24 mA	3 V		0.55	
I _I		$V_1 = V_{CC}$ or GND	3.6 V		±5	μΑ
		V ₁ = 0.58 V	1.65 V	25		
		V ₁ = 1.07 V	1.65 V	-25		
		V ₁ = 0.7 V	2.3 V	45		
I _{I(hold)}		V ₁ = 1.7 V	2.3 V	-45		μA
		V ₁ = 0.8 V	3 V	75		
		V ₁ = 2 V	3 V	-75		
		$V_1 = 0 \text{ to } 3.6 \text{ V}^{(2)}$	3.6 V		±500	
I _{OZ}		$V_0 = V_{CC}$ or GND	3.6 V		±10	μA
I _{CC}		$V_{I} = V_{CC} \text{ or } GND, \qquad I_{O} = 0$	3.6 V		40	μA
ΔI_{CC}		One input at V_{CC} - 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V		750	μA
6	Control inputs	V = V or GND	221/		3.5	рЕ
Ui	Data inputs		3.3 V		6	рг
Co	Outputs	$V_0 = V_{CC}$ or GND	3.3 V		7	pF

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(1)

All typical values are at V_{CC} = 3.3 V, T_A = 25°C. This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to (2) another.

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

			V _{CC} =	1.8 V	V _{CC} = ± 0.	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} = ± 0.	3.3 V 3 V	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency			(1)		150		150		150	MHz
t _w	Pulse duration, CLK high or low				3.3		3.3		3.3		ns
+	Sotup time	Data before CLK↑	(1)		4		3.6		3.1		20
^L su	Setup time	CLKEN before CLK1	(1)		3.4		3.1		2.7		115
th	Lold time	Data after CLK↑	(1)		0		0		0		20
u i		CLKEN after CLK1	(1)		0		0		0		115

(1) This information was not available at the time of publication.



SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO (OUTBUT)	V _{CC} = 1.8 V		V_{CC} = 2.5 V \pm 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
	(INFOT)	(001-01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			(1)		150		150		150		MHz
t _{pd}	CLK	Q		(1)	1	5.6	1	5.1	1	4.3	ns
t _{en}	OE	Q		(1)	1	6.1	1	5.8	1	4.8	ns
t _{dis}	ŌĒ	Q		(1)	1	5.5	1	4.7	1	4.4	ns

(1) This information was not available at the time of publication.

OPERATING CHARACTERISTICS

 $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V		
		TEST CONDITIONS	TYP	TYP	TYP		
6	Power dissipation	Outputs enabled	C = 50 pc f = 10 MHz	(1)	55	59	۶E
C _{pd}	capacitance	Outputs disabled	$C_{L} = 50 \text{ pr}, 1 = 10 \text{ MHz}$	(1)	46	49	рг

(1) This information was not available at the time of publication.



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PARAMETER MEASUREMENT INFORMATION

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z₀ = 50 Ω , t_r \leq 2 ns, t_f \leq 2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PIZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .



TEXAS INSTRUMENTS www.ti.com

SN74ALVCH16721 3.3-V 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS

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NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z₀ = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms



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NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_r \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 3. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Baakaga	Bookago	Dine	Dookog	Eco Blon ⁽²⁾	Lood/Boll Einicl	MEL Book Tomp (3)
Orderable Device	Status V	Туре	Drawing	FINS	Qty	e Eco Plan V		i wise reak temp '
74ALVCH16721DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16721DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16721DGVRE4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16721DGVRG4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16721DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16721DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16721GRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16721DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16721DGVR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16721DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16721DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE OPTION ADDENDUM

27-Sep-2007

to Customer on an annual basis.

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All dimensions are nominal												
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH16721DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ALVCH16721DGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1
SN74ALVCH16721DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1



PACKAGE MATERIALS INFORMATION

11-Mar-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH16721DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74ALVCH16721DGVR	TVSOP	DGV	56	2000	346.0	346.0	41.0
SN74ALVCH16721DLR	SSOP	DL	56	1000	346.0	346.0	49.0

MECHANICAL DATA

MSSO001C - JANUARY 1995 - REVISED DECEMBER 2001

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

DL (R-PDSO-G**)



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118



MECHANICAL DATA

MTSS003D - JANUARY 1995 - REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



MECHANICAL DATA

PLASTIC SMALL-OUTLINE

MPDS006C - FEBRUARY 1996 - REVISED AUGUST 2000

DGV (R-PDSO-G**)

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins MO-153

14/16/20/56 Pins – MO-194



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