SN74LS377, SN74LS378, SN74LS379 OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH ENABLE SDLS167 – OCTOBER 1976 – REVISED MARCH 1988

- 'LS377 and 'LS378 Contain Eight and Six Flip-Flops, Respectively, with Single-Rail Outputs
- 'LS379 Contains Four Flip-Flops with Double-Rail Outputs
- Individual Data Input to Each Flip-Flop
- Applications Include: Buffer/Storage Registers Shift Registers Pattern Generators

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with an enable input. The 'LS377, 'LS378, and 'LS379 devices are similar to 'LS273, 'LS174, and 'LS175, respectively, but feature a common enable instead of a common clear.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the enable input \overline{G} is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the \overline{G} input.

These flip-flops are guaranteed to respond to clock frequencies ranging from 0 to 30 MHz while maximum clock frequency is typically 40 megahertz. Typical power dissipation is 10 milliwatts per flip-flop.

FUNCT	ION	TABLE
(EACH	FLIF	-FLOP)

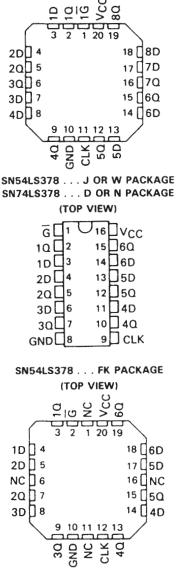
	INPUT	OUT	PUTS	
Ĝ	CLOCK	DATA	Q	ā
н	X	х	Q ₀	ā ₀
L	t	н	н	L
L	†	L	L.	н
х	L	х	Q0	$\overline{\mathbf{Q}}_{0}$

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



SN54LS377 J P. SN74LS377 DW OR (TOP VIEW)	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	VCC 80 80 70 70 60 60 50 50 50 CLK
SN54LS377 FK F	ACKAGE
(TOP VIEW)	

SN54LS377, SN54LS378, SN54LS379,



NC - No internal connection

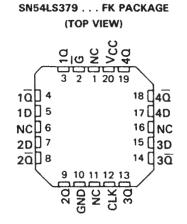
Copyright © 1988, Texas Instruments Incorporated

SN54LS377, SN54LS378, SN54LS379, SN74LS377, SN74LS378, SN74LS379 OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH ENABLE

SDLS167 – OCTOBER 1976 – REVISED MARCH 1988

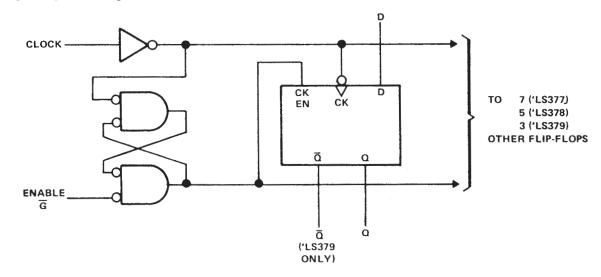
SN54LS379 . . . J OR W PACKAGE SN74LS379 . . . D OR N PACKAGE (TOP VIEW)

1 2 3 4 5 6 7	U16 15 14 13 12 11 10	Vcc 40 40 40 30 30 30 30
7 8	10 9	Цза Дсгк

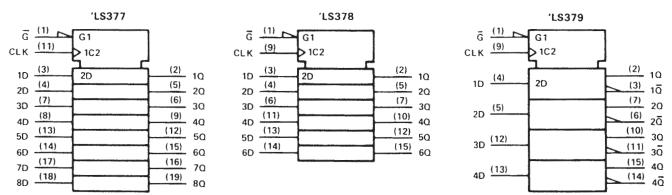


NC - No internal connection

logic diagram (positive logic)



logic symbols[†]

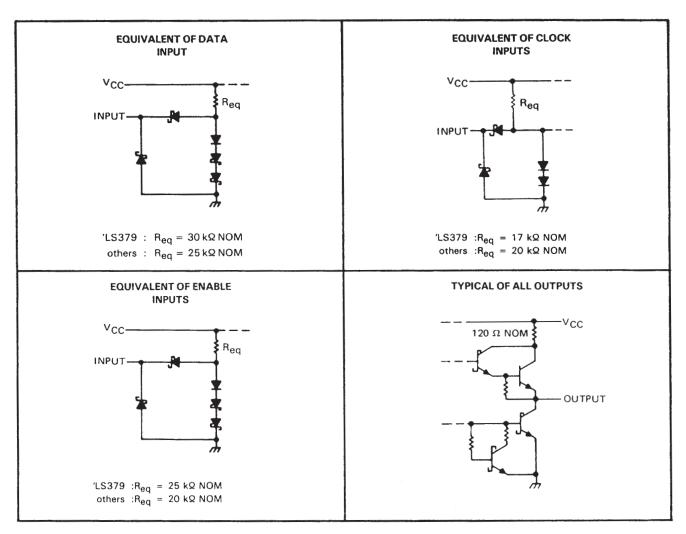


[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.



SN54LS377, SN54LS378, SN54LS379, SN74LS377, SN74LS378, SN74LS379 OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH ENABLE SDLS167 - OCTOBER 1976 - REVISED MARCH 1988

schematics of inputs and outputs



absolute maximum rating over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)	1
Input voltage	
Operating free-air temperature range: SN54LS'	2
SN74LS'	2
Storage temperature range \ldots	2

NOTE 1: Voltage values are with respect to network ground terminal.



SN54LS377, SN54LS378, SN54LS379, SN74LS377, SN74LS378, SN74LS379 OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH ENABLE

SDLS167 - OCTOBER 1976 - REVISED MARCH 1988

recommended operating conditions

			SN54LS	5'		SN74LS	5'	
		MIN	NOM	MAX	MIN	NOM	IOM MAX	UNIT
Supply voltage, VCC	4.5	5	5,5	4.75	5	5,25	V	
High-level output current, IOH			-400			-400	μA	
Low-level output current, IOL			4			8	mA	
Clock frequency, fclock	0		30	0		30	MHz	
Width of clock pulse, tw		20			20			ns
	Data input	201			201			
Setup time, t _{su}	Enable active-state	251			251			ns
Enable inactive-state		10†			101			1
Hold time, th	Data and enable	51			51	<u>}</u>		ns
Operating free-air temperature, TA		-55		125	0		70	°c

[†]The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	те	T CONDITIONS	t		SN54LS	1		SN74LS	¥	
		16	ST CONDITIONS		MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage				2			2			V
VIL	Low-level input voltage						0.7			0.8	V
VIK	Input clamp voltage	VCC = MIN,	11 = -18 mA				-1.5			-1.5	V
v _{он}	High-level output voltage	V _{CC} = MIN, VIL = VIL max,	V _{IH} = 2 V, I _{OH} = -400 μA		2.5	3.5		2.7	3.5		v
VOL	Low-level output voltage	V _{CC} = MIN, VIL = VIL max	V _{IH} = 2 V,	$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$		0.25	0.4		0.25 0.35	0.4	v
t _i	Input current at maximum input voltage	V _{CC} = MAX,	V _I = 7 V				0.1			0,1	mA
Чн	High-level input current	V _{CC} = MAX,	V1 = 2.7 V				20			20	μA
μL	Low-level input current	V _{CC} = MAX,	VI = 0.4 V				-0.4			-0.4	mA
los	Short-circuit output current§	V _{CC} = MAX			-20		-100	-20		-100	mA
				'LS377		17	28		17	28	mA
ICC	Supply current	V _{CC} = MAX,	See Note 2	'LS378		13	22		13	22	mA
				'LS379		9	15		9	15	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$.

§ Note more than one input should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open and ground applied to all data and enable inputs, ICC is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, $V_{CC} = 5 V$, $T_A = 25^{\circ}C$

PARAMETER	TEST CONDITIONS	MIN	түр	MAX	UNIT
f _{max} Maximum clock frequency	CL = 15 pF,	30	40		MHz
tPLH Propagation delay time, low-to-high-level output from clock	RL = 2 kΩ		17	27	ns
tPHL Propagation delay time, high-to-low-level output from clock	See Note 3		18	27	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.





25-Jan-2012

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-8992501EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	
5962-8992501FA	ACTIVE	CFP	W	16	1	TBD	Call TI	Call TI	
5962-8992501FA	ACTIVE	CFP	W	16	1	TBD	Call TI	Call TI	
JM38510/32504B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/32504B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/32504BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
JM38510/32504BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
JM38510/32504BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	
JM38510/32504BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	
M38510/32504B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/32504B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/32504BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
M38510/32504BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
M38510/32504BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	
M38510/32504BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	
SN54LS377J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SN54LS377J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SN54LS378J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN54LS378J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN54LS379J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN54LS379J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SN74LS377DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS377DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS377DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS377DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS377DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



25-Jan-2012

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LS377DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS377DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS377DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS377DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS377DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS377DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS377DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS377N	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS377N	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS377N3	OBSOLETE	PDIP	Ν	20		TBD	Call TI	Call TI	
SN74LS377N3	OBSOLETE	PDIP	Ν	20		TBD	Call TI	Call TI	
SN74LS377NE4	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS377NE4	ACTIVE	PDIP	Ν	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS377NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS377NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS377NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS377NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS377NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS377NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS378D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



25-Jan-2012

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LS378D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS378DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS378DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS378DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS378DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS378DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS378DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS378DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS378DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS378DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS378DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS378N	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS378N	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS378N3	OBSOLETE	E PDIP	Ν	16		TBD	Call TI	Call TI	
SN74LS378N3	OBSOLETE	E PDIP	Ν	16		TBD	Call TI	Call TI	
SN74LS378NE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS378NE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS379D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	
SN74LS379D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	
SN74LS379J	OBSOLETE	E CDIP	J	16		TBD	Call TI	Call TI	
SN74LS379J	OBSOLETE	E CDIP	J	16		TBD	Call TI	Call TI	
SN74LS379N	OBSOLETE	E PDIP	Ν	16		TBD	Call TI	Call TI	
SN74LS379N	OBSOLETE	PDIP	Ν	16		TBD	Call TI	Call TI	



25-Jan-2012

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SNJ54LS377FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS377FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS377J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SNJ54LS377J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	
SNJ54LS377W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	
SNJ54LS377W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	
SNJ54LS378FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	
SNJ54LS378FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	
SNJ54LS378J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54LS378J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54LS378W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
SNJ54LS378W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
SNJ54LS379FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS379FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS379J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54LS379J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	
SNJ54LS379W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	
SNJ54LS379W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)



25-Jan-2012

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54LS377, SN54LS378, SN54LS379, SN74LS377, SN74LS378, SN74LS379 :

• Catalog: SN74LS377, SN74LS378, SN74LS379

• Military: SN54LS377, SN54LS378, SN54LS379

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

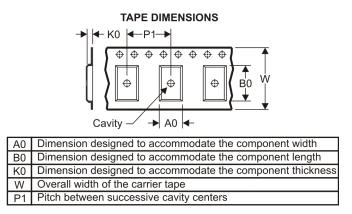
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS377DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LS377NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74LS378DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

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PACKAGE MATERIALS INFORMATION

29-Jul-2009



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS377DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74LS377NSR	SO	NS	20	2000	346.0	346.0	41.0
SN74LS378DR	SOIC	D	16	2500	333.2	345.9	28.6

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20



LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N**) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-013 variation AC.



LAND PATTERN DATA



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0°-10° Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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