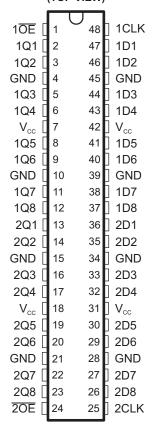
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FEATURES

- State-of-the-Art Advanced BiCMOS
 Technology (ABT) Widebus™ Design for 2.5-V
 and 3.3-V Operation and Low Static Power
 Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V V_{CC})
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- High Drive (-24/24 mA at 2.5-V V_{CC} and -32/64 mA at 3.3-V)
- Power Off Disables Outputs, Permitting Live Insertion
- High-Impedance State During Power Up and Power Down Prevents Driver Conflict
- Uses Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating
- Auto3-State Eliminates Bus Current Loading When Output Exceeds V_{CC} + 0.5 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection
 - Exceeds 2000 V Per MIL-STD-883, Method 3015
 - Exceeds 200 V Using Machine Model
 - Exceeds 1000 V Using Charged-Device Model, Robotic Method
- Flow-Through Architecture Facilitates Printed Circuit Board Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package

SN54ALVTH16374...WD PACKAGE SN74ALVTH16374...DGG, DGV, OR DL PACKAGE (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The 'ALVTH16374 devices are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for 2.5-V or 3.3-V V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the flip-flops store the logic levels set up at the data (D) inputs.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ALVTH16374 is characterized for operation over the full military temperature range of -55°C to 125°C.

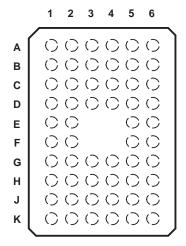
The SN74ALVTH16374 is characterized for operation from -40°C to 85°C.

ORDERING INFORMATION

T _A	P	ACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	TSSOP – DGG	Reel of 2000	74ALVTH16374GRE4	
	1330F - DGG	Reel of 2000	SN74ALVTH16374GR	
	TVCOD DCV	Dark of 2000	74ALVTH16374VRE4	
400C to 050C	TVSOP – DGV	Reel of 2000	SN74ALVTH16374VR	
–40°C to 85°C		Tub	74ALVTH16374DL	
	CCOD DI	Tube of 25	SN74ALVTH16374DLG4	
	SSOP – DL	Dark of 4000	SN74ALVTH16374DLR	
		Reel of 1000	SN74ALVTH16374DLRG4	

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ZQL PACKAGE (TOP VIEW)



TERMINAL ASSIGNMENTS(1)

	1	2	3	4	5	6
Α	1 OE	NC	NC	NC	NC	1CLK
В	1Q2	1Q1	GND	GND	1D1	1D2
С	1Q4	1Q3	V_{CC}	V_{CC}	1D3	1D4
D	1Q6	1Q5	GND	GND	1D5	1D6
E	1Q8	1Q7			1D7	1D8
F	2Q1	2Q2			2D2	2D1
G	2Q3	2Q4	GND	GND	2D4	2D3
Н	2Q5	2Q6	V _{CC}	V _{CC}	2D6	2D5
J	2Q7	2Q8	GND	GND	2D8	2D7
K	2 OE	NC	NC	NC	NC	2CLK

(1) NC - No internal connection

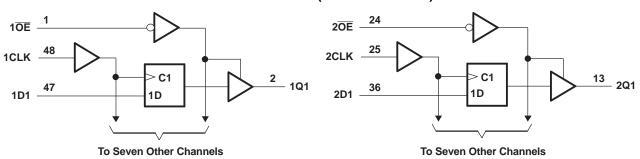
FUNCTION TABLE (each 8-bit section)

	INPUTS		OUTPUT
OE	CLK	D	Q
L	1	Н	Н
L	\uparrow	L	L
L	H or L	Χ	Q_0
Н	Χ	Χ	Z

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LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG, DL, and WD packages.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	4.6	V
V_{I}	Input voltage range ⁽²⁾		-0.5	7	V
Vo	Voltage range applied to any output in the high-impedar	nce or power-off state ⁽²⁾	-0.5	7	V
Vo	Voltage range applied to any output in the high state ⁽²⁾		-0.5	7	V
	Output assument in the lass state	SN54ALVTH16374 ⁽³⁾		96	Λ
IO	Output current in the low state	SN74ALVTH16374		128	mA
	Output accompation that himb atoms	SN54ALVTH16374 ⁽³⁾		-48	Λ
IO	Output current in the high state	SN74ALVTH16374		-64	mA
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
		DGG package		89	
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGV package		93	°C/W
		DL package		94	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

³⁾ Product preview

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51.

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Recommended Operating Conditions(1)

 $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

			SN54A	LVTH16	374 ⁽²⁾	SN74AL	VTH16	374	UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	UNII
V _{CC}	Supply voltage		2.3		2.7	2.3		2.7	V
V _{IH}	High-level input voltage		1.7			1.7			V
V _{IL}	Low-level input voltage				0.7			0.7	V
VI	Input voltage		0	V _{CC}	5.5	0	V _{CC}	5.5	V
I _{OH}	High-level output current				-6			-8	mA
	Low-level output current				6			8	A
I _{OL}	Low-level output current; current duty cycle	≤ 50%; f ≥ 1 kHz			18			24	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled			10			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200			200			μs/V
T _A	Operating free-air temperature		-55		125	-40		85	°C

⁽¹⁾ All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Recommended Operating Conditions(1)

 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

			SN54AL	_VTH163	374 ⁽²⁾	SN74A	LVTH16	374	UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	UNII
V _{CC}	Supply voltage		3		3.6	3		3.6	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				8.0			8.0	V
V_{I}	Input voltage		0	V_{CC}	5.5	0	V_{CC}	5.5	V
I _{OH}	High-level output current				-24			-32	mA
	Low-level output current				24			32	mΛ
I _{OL}	Low-level output current; current duty cyc	cle ≤ 50%; f ≥ 1 kHz			48			64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200			200			μs/V
T _A	Operating free-air temperature		-55		125	-40		85	°C

⁽¹⁾ All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

⁽²⁾ Product preview

⁽²⁾ Product preview





Electrical Characteristics

over operating free-air temperature range V_{CC} = 2.5 V \pm 0.2 V (unless otherwise noted)

	DADAMETED	TEST OF	ONDITIONS	SN54ALVTI	H16374 ⁽¹⁾	SN74AL	VTH16374	
	PARAMETER	IESI CO	ONDITIONS	MIN TY	'P ⁽²⁾ MA	X MIN	TYP ⁽²⁾ MAX	UNIT
V_{IK}		$V_{CC} = 2.3 \text{ V},$	$I_1 = -18 \text{ mA}$		-1	.2	-1.2	V
		$V_{CC} = 2.3 \text{ V to } 2.7$	$^{\prime}$ V, $I_{OH} = -100 \mu A$	V _{CC} - 0.2		V _{CC} - 0.2		
V _{OH}		V _{CC} = 2.3 V	$I_{OH} = -6 \text{ mA}$	1.8				V
		$V_{CC} = 2.3 \text{ V}$	$I_{OH} = -8 \text{ mA}$			1.8		
		$V_{CC} = 2.3 \text{ V to } 2.7$	' V, I _{OL} = 100 μA		C	.2	0.2	
			I _{OL} = 6 mA		C	.4		
V_{OL}		V 22V	I _{OL} = 8 mA				0.4	V
		V _{CC} = 2.3 V	I _{OL} = 18 mA		C	.5		
			I _{OL} = 24 mA				0.5	
	Control innuts	V _{CC} = 2.7 V,	$V_I = V_{CC}$ or GND		:	±1	±1	
	Control inputs	$V_{CC} = 0 \text{ or } 2.7 \text{ V},$	V _I = 5.5 V			10	10	
I_{\parallel}			V _I = 5.5 V			10	10	μΑ
	Data inputs	$V_{CC} = 2.7 \text{ V}$	$V_I = V_{CC}$			1	1	
			V _I = 0			-5	-5	
I _{off}		$V_{CC} = 0,$ $V_{I} \text{ or } V_{O} = 0 \text{ to } 4.5$	5 V				±100	μΑ
I _{BHL}	(3)	$V_{CC} = 2.3 \text{ V},$	V _I = 0.7 V		115		115	μΑ
I _{BHH}	(4)	$V_{CC} = 2.3 \text{ V},$	V _I = 1.7 V		-10		-10	μΑ
I _{BHL}	O ⁽⁵⁾	V _{CC} = 2.7 V,	$V_I = 0$ to V_{CC}	300		300		μΑ
I _{BHH}	O ⁽⁶⁾	V _{CC} = 2.7 V,	V _I = 0 to V _{CC}	-300		-300		μΑ
I _{EX} ⁽⁷	7)	$V_{CC} = 2.3 \text{ V},$	V _O = 5.5 V		1:	25	125	μΑ
I _{OZ(F}	PU/PD) ⁽⁸⁾	$V_{CC} \le 1.2 \text{ V}, V_{O} = V_{I} = \text{GND or } V_{CC},$	0.5 V to V _{CC} , OE = don't care		±1	00	±100	μΑ
I _{OZH}		$V_{CC} = 2.7 \text{ V}, V_{O} = V_{I} = 0.7 \text{ V} \text{ or } 1.7 \text{ V}$	2.3 V, /			5	5	μΑ
I _{OZL}		$V_{CC} = 2.7 \text{ V}, V_{O} = V_{I} = 0.7 \text{ V} \text{ or } 1.7 \text{ V}$				-5	-5	μΑ
		V _{CC} = 2.7 V,	Outputs high		0.04	.1	0.1	
I_{CC}		$I_0 = 0$.	Outputs low		2.3 4	5	4.5	mA
		$V_I = V_{CC}$ or GND	Outputs disabled		0.04	.1	0.1	
C_{i}		$V_{CC} = 2.5 V,$	V _I = 2.5 V or 0		3.5			pF
Co		$V_{CC} = 2.5 \text{ V},$	$V_0 = 2.5 \text{ V or } 0$		6			pF

All typical values are at V_{CC} = 2.5 V, T_A = 25°C. The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

The bus-hold circuit can source at least the minimum high sustaining current at VIH min. IBHH should be measured after raising VIN to V_{CC} and then lowering it to V_{IH} min.

 ⁽⁵⁾ An external driver must source at least I_{BHLO} to switch this node from low to high.
 (6) An external driver must sink at least I_{BHHO} to switch this node from high to low.
 (7) Current into an output in the high state when V_O > V_{CC}

⁽⁸⁾ High-impedance state during power up or power down



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Electrical Characteristics

over recommended operating free-air temperature range V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted)

	DADAMETED	TEST COL	UDITIONS	SN54ALV	/TH1637	4 ⁽¹⁾	SN74	ALVTH16	374	UNIT
	PARAMETER	TEST CO	NUTTIONS	MIN	TYP ⁽²⁾	MAX	MIN	TYP ⁽²⁾	MAX	UNIT
V_{IK}		$V_{CC} = 3 V$,	$I_1 = -18 \text{ mA}$			-1.2			-1.2	V
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V},$	$I_{OH} = -100 \mu A$	V _{CC} - 0.2			V _{CC} - 0.2			
V_{OH}		V 2.V	$I_{OH} = -24 \text{ mA}$	2						V
		$V_{CC} = 3 V$	$I_{OH} = -32 \text{ mA}$				2			
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V},$	I _{OL} = 100 μA			0.2			0.2	
			I _{OL} = 16 mA						0.4	
.,			$I_{OL} = 24 \text{ mA}$			0.5				V
V_{OL}		$V_{CC} = 3 V$	I _{OL} = 32 mA						0.5	V
			I _{OL} = 48 mA			0.55				
			I _{OL} = 64 mA						0.55	
	On attack in most a	$V_{CC} = 3.6 \text{ V}, V_{I} = V_{C}$	C or GND			±1			±1	
	Control inputs	$V_{CC} = 0 \text{ or } 3.6 \text{ V}, \text{ V}_{I} = 0.00 \text{ V}$	= 5.5 V			10			10	
I			$V_1 = 5.5 \text{ V}$			10			10	μΑ
	Data inputs	$V_{CC} = 3.6 \text{ V}$	$V_I = V_{CC}$			1			1	
			$V_I = 0$			-5			-5	
I _{off}	1	$V_{CC} = 0$, V_I or $V_O = 0$	to 4.5 V						±100	μΑ
I _{BHL} (3)		$V_1 = 0.8 \text{ V}$	75			75			μΑ
I _{BHH}	(4)	V _{CC} = 3 V,	V _I = 2 V	-75			-75			μΑ
I _{BHLC}) ⁽⁵⁾	V _{CC} = 3.6 V,	$V_I = 0$ to V_{CC}	500			500			μΑ
I _{BHH}	O ⁽⁶⁾	V _{CC} = 3.6 V,	$V_I = 0$ to V_{CC}	-500			-500			μΑ
I _{EX} (7		$V_{CC} = 3 V$,	V _O = 5.5 V			125			125	μΑ
I _{OZ(P}	U/PD) ⁽⁸⁾	$V_{CC} \le 1.2 \text{ V}, V_O = 0.5$ $V_I = \text{GND or } V_{CC}, \overline{\text{OE}}$	5 V to V _{CC} , = don't care			±100			±100	μΑ
I _{OZH}		$V_{CC} = 3.6 \text{ V}, V_{O} = 3 \text{ V}$ $V_{I} = 0.8 \text{ V or } 27 \text{ V}$	V,			5			5	μΑ
I _{OZL}		$V_{CC} = 3.6 \text{ V}, V_{O} = 0.8 \text{ V}$ $V_{I} = 0.8 \text{ V}$ or 2 V	5 V,			-5			-5	μΑ
		V _{CC} = 3.6 V,	Outputs high		0.07	0.1		0.07	0.1	
I_{CC}		$I_0 = 0$	Outputs low		3.2	5		3.2	5	mA
		$V_I = V_{CC}$ or GND	Outputs disabled		0.07	0.1			0.1	
Δl _{CC}	(9)	$V_{CC} = 3 \text{ V to } 3.6 \text{ V},$ One input at $V_{CC} = 0.$ Other inputs at $V_{CC} = 0.$				0.4			0.4	mA
C _i		V _{CC} = 3.3 V,	V _I = 3.3 V or 0		3.5			3.5		pF
Co		$V_{CC} = 3.3 \text{ V},$	V _O = 3.3 V or 0		6			6		pF

- (1) Product preview
- All typical values are at $V_{CC} = 2.5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.
- (3) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to $V_{\text{IL}}\ \text{max}.$
- The bus-hold circuit can source at least the minimum high sustaining current at VIH min. IBHH should be measured after raising VIN to $V_{\rm CC}$ and then lowering it to $V_{\rm IH}$ min. An external driver must source at least $I_{\rm BHLO}$ to switch this node from low to high.
- An external driver must sink at least I_{BHHO} to switch this node from high to low. Current into an output in the high state when $V_O > V_{CC}$

- (8) High-impedance state during power up or power down
 (9) This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.





Timing Requirements

over recommended operating free-air temperature range V_{CC} = 2.5 V \pm 0.2 V (unless otherwise noted) (see Figure 1)

			SN54ALVTH	16374 ⁽¹⁾	SN74ALVTH1	16374	UNIT
			MIN	MAX	MIN	MAX	UNII
f _{clock}	Clock frequency			150		150	MHz
t _w	Pulse duration, CLK high or low		1.5		1.5		ns
	Setup time, data before CLK↑	Data high	1.1		1		20
t _{su}	Setup time, data before CEN	Data low	1.4		1.3		ns
	Hold time, data after CLK↑	Data high	0.6	·	0.5		22
t _h	Hold tille, data after CER	Data low	0.9		0.8		ns

⁽¹⁾ Product preview

Timing Requirements

over recommended operating free-air temperature range V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 2)

			SN54ALVTH	16374 ⁽¹⁾	SN74ALVTI	H16374	
			MIN	MAX	MIN	MAX	UNIT
f _{clock}	Clock frequency			25		250	MHz
t _w	Pulse duration, CLK high or low		1.5		1.5		ns
	Catura time a data batana CLIVA	Data high	1.1		1		
t _{su}	Setup time, data before CLK↑	Data low	1.6		1.5		ns
	Hold time data after CLKA	Data high	0.6		0.5		
t _h	Hold time, data after CLK↑	Data low	1.1		1		ns

⁽¹⁾ Product preview

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Switching Characteristics

over recommended operating free-air temperature range, C_L = 30 pF, V_{CC} = 2.5 V \pm 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	SN54ALVTH16	6374 ⁽¹⁾	SN74ALVTH	16374	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	UNII
f _{max}			150		150		MHz
t _{PLH}	CLK	Q	1.4	3.9	1.5	3.8	no
t _{PHL}	CLK	Q	1.4	3.9	1.5	3.8	ns
t _{PZH}	- OE	0	1	4.2	1	4.1	
t _{PZL}	OE OE	Q	1	3.8	1	3.7	ns
t _{PHZ}	- OE	0	1.7	4.3	1.8	4.2	no
t _{PLZ}	OE .	Q	1	3.5	1	3.4	ns

⁽¹⁾ Product preview

Switching Characteristics

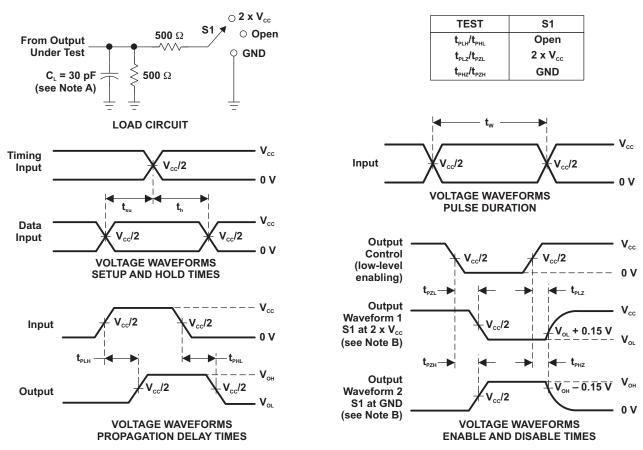
over recommended operating free-air temperature range, C_L = 50 pF, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 2)

DADAMETED	FROM	то	SN54ALVTH1	6374 ⁽¹⁾	SN74ALVTH	16374	LINUT
PARAMETER	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	UNIT
f _{max}			250		250		MHz
t _{PLH}	CLK	0	1	3.4	1	3.2	no
t _{PHL}	CLK	Q	1	3.3	1	3.2	ns
t _{PZH}	ŌĒ	0	1	3.9	1	3.8	
t _{PZL}	OE	Q	1	3.4	1	3.3	ns
t _{PHZ}	ŌĒ	0	1	4.7	1	4.6	
t _{PLZ}	OE .	Q	1	4.4	1	4.2	ns

(1) Product preview



PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.5 V \pm 0.2 V



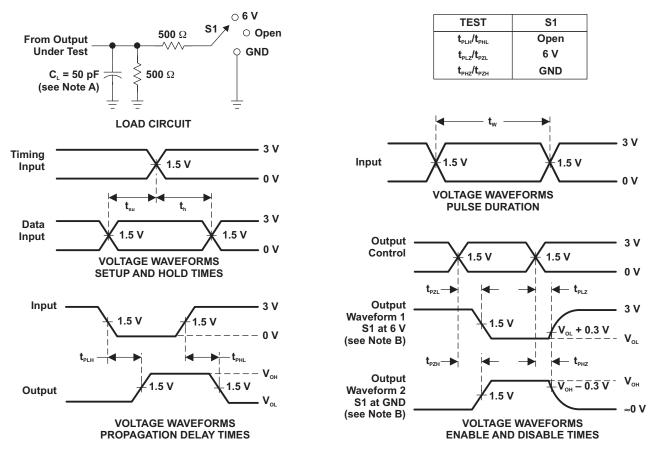
NOTES: A. C, includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_o = 50 Ω , $t_o \leq$ 2 ns, $t_o \leq$ 2 ns.
- D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION V_{CC} = 3.3 V ± 0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_o = 50 Ω , $t_i \leq$ 2.5 ns. $t_i \leq$ 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms



3-May-2012

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
74ALVTH16374DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74ALVTH16374DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74ALVTH16374GRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74ALVTH16374GRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74ALVTH16374VRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74ALVTH16374VRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74ALVTH16374ZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	
SN74ALVTH16374DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALVTH16374DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALVTH16374GR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALVTH16374KR	LIFEBUY	BGA MICROSTAR JUNIOR	GQL	56	1000	TBD	SNPB	Level-1-240C-UNLIM	
SN74ALVTH16374VR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.



PACKAGE OPTION ADDENDUM

3-May-2012

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

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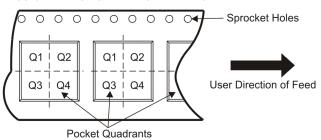
TAPE AND REEL INFORMATION



TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ALVTH16374ZQLR	BGA MI CROSTA R JUNI OR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.45	8.0	16.0	Q1
SN74ALVTH16374DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74ALVTH16374GR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74ALVTH16374KR	BGA MI CROSTA R JUNI OR	GQL	56	1000	330.0	16.4	4.8	7.3	1.45	8.0	16.0	Q1
SN74ALVTH16374VR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

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*All dimensions are nomina

All differsions are nominal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ALVTH16374ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	333.2	345.9	28.6
SN74ALVTH16374DLR	SSOP	DL	48	1000	346.0	346.0	49.0
SN74ALVTH16374GR	TSSOP	DGG	48	2000	346.0	346.0	41.0
SN74ALVTH16374KR	BGA MICROSTAR JUNIOR	GQL	56	1000	333.2	345.9	28.6
SN74ALVTH16374VR	TVSOP	DGV	48	2000	346.0	346.0	33.0

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is Pb-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

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DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.



DL (R-PDSO-G**)

48 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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