

FEATURES

- Member of the Texas Instruments Widebus™ Family
- EPIC<sup>™</sup> (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot) > 2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

## DESCRIPTION

This 16-bit edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V  $V_{\rm CC}$  operation.

The SN74LVC16374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to V<sub>CC</sub> through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVC16374 is characterized for operation from –40°C to 85°C.



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# SN74LVC16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

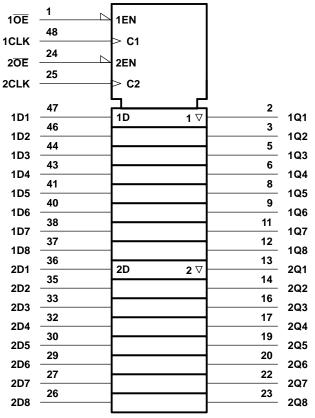
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#### FUNCTION TABLE (EACH FLIP-FLOP)

	INPUTS	OUTPUT	
OE	CLK	D	Q
L	$\uparrow$	Н	Н
L	$\uparrow$	L	L
L	H or L	Х	Q <sub>0</sub>
н	Х	Х	Z

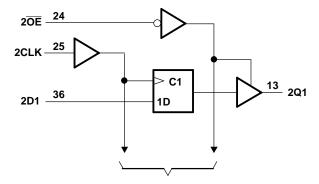
# LOGIC SYMBOL<sup>(1)</sup>



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# LOGIC DIAGRAM (POSITIVE LOGIC) 10E 1 1CLK 48 1D1 47 1D1 47 1D1 2 1Q1

**To Seven Other Channels** 



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## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range			4.6	V
VI	Input voltage range <sup>(2)</sup>		-0.5	4.6	V
Vo	Output voltage range <sup>(2)(3)</sup>		-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>1</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	$V_{O}$ < 0 or $V_{O}$ > $V_{CC}$		±50	mA
I <sub>O</sub>	Continuous output current	$V_{O} = 0$ to $V_{CC}$		±50	mA
	Continuous current through V <sub>CC</sub> or GND			±100	mA
	Maximum numerical states at $T = 5500$ (in still sig)(4)	DGG package		0.85	14/
	Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) <sup>(4)</sup>	DL package		1.2	W
T <sub>stg</sub>	Storage temperature range	i	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed. This value is limited to 4.6 V maximum. (2)

(3)

(4) The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

## Recommended Operating Conditions<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2.7	3.6	V
VIH	High-level input voltage	$V_{CC}$ = 2.7 V to 3.6 V	2		V
V <sub>IL</sub>	Low-level input voltage	$V_{CC}$ = 2.7 V to 3.6 V		0.8	V
VI	Input voltage		0	$V_{CC}$	V
Vo	Output voltage		0	$V_{CC}$	V
	High-level output current	$V_{CC} = 2.7 V$		-12	mA
ЮН	High-level output current	$V_{CC} = 3 V$		-24	IIIA
	Low-level output current	$V_{CC} = 2.7 V$		12	mA
IOL	$V_{CC} = 3 V$			24	IIIA
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

(1) Unused control inputs must be held high or low to prevent them from floating.

# SN74LVC16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

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#### **Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	V <sub>CC</sub> <sup>(1)</sup>	MIN	TYP <sup>(2)</sup> MAX	UNIT	
		I <sub>OH</sub> = -100 μA	MIN to MAX	V <sub>CC</sub> - 0.2			
		10	2.7 V	2.2		V	
V <sub>OH</sub>		I <sub>OH</sub> = -12 mA	3 V	2.4		v	
		I <sub>OH</sub> = -24 mA	3 V	2			
		I <sub>OL</sub> = 100 μA	MIN to MAX		0.2		
V <sub>OL</sub>		I <sub>OL</sub> = 12 mA	2.7 V		0.4	V	
		I <sub>OL</sub> = 24 mA	3 V		0.55		
I <sub>I</sub>		$V_{I} = V_{CC}$ or GND	3.6 V		±5	μΑ	
		V <sub>I</sub> = 0.8 V	0.1/	75			
I <sub>I(hold)</sub>	Data inputs	V <sub>1</sub> = 2 V	3 V	-75		μΑ	
		V <sub>1</sub> = 0 to 3.6 V	3.6 V		±500		
I <sub>OZ</sub>	1	$V_0 = V_{CC}$ or GND	3.6 V		±10	μΑ	
I <sub>CC</sub>		$V_{I} = V_{CC} \text{ or } GND, \qquad I_{O} = 0$	3.6 V		40	μA	
$\Delta I_{CC}$		One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND	3 V to 3.6 V		500	μΑ	
Ci		$V_{I} = V_{CC}$ or GND	3.3 V		3.5	pF	
Co		$V_{O} = V_{CC}$ or GND	3.3 V		7	pF	

(1) For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

(2) All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

## **Timing Requirements**

over recommended operating free-air temperature range (unless otherwise noted)

			± 0.3 V		V <sub>CC</sub> = 2.7 V		UNIT
					MAX	X	
f <sub>clock</sub>	f <sub>clock</sub> Clock frequency		0	100	0	80	MHz
tw	tw Pulse duration, CLK high or low		4		4		ns
t <sub>su</sub>	Setup time, data before CLK↑	High or low	2		3		ns
t <sub>h</sub>	Hold time, data after CLK↑	High or low	1.5		1.5		ns

## **Switching Characteristics**

over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO	то (OUTPUT)		3.3 V 3 V	V <sub>CC</sub> =	2.7 V	UNIT
	(INFOT)	(001F01)	MIN	MAX	MIN	MAX		
f <sub>max</sub>			100		80		MHz	
t <sub>pd</sub>	CLK	Q	1.5	7.5	1.5	8.5	ns	
t <sub>en</sub>	ŌE	Q	1.5	7.5	1.5	8.5	ns	
t <sub>dis</sub>	OE	Q	1.5	7	1.5	8	ns	

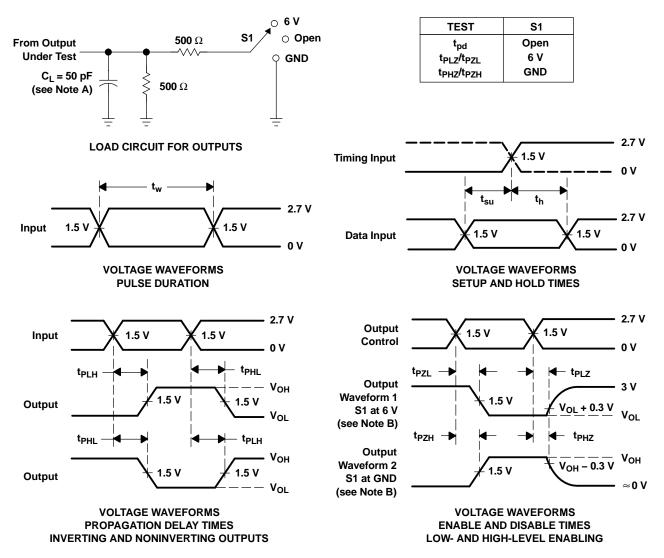
## **Operating Characteristics**

 $V_{CC} = 3.3 \text{ V}, \text{ T}_{A} = 25^{\circ}\text{C}$ 

PARAMETER		TEST CONDITIONS	TYP	UNIT	
C <sub>pd</sub>	Power dissipation capacitance per flip-flop	Outputs enabled	$C_{-} = 50 \text{ pc} \text{ f} = 10 \text{ MHz}$	22	рF
		Outputs disabled	C <sub>L</sub> = 50 pF, f = 10 MHz	9	

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NOTES: A. C<sub>1</sub> includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the ouput is high, except when disabled by the output control.

- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub>  $\leq$  2.5 ns, t<sub>f</sub>  $\leq$  2.5 ns. D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PL7}$  and  $t_{PH7}$  are the same as  $t_{dis}$ .

F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.

G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.

#### Figure 1. Load Circuit and Voltage Waveforms

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