16 V<sub>CC</sub>

15 [] 6Q

14**∏** 6D

13 5D

12 5Q

11 **∏** 4D

10 4Q

9∏ CLK

CD54ACT174...F PACKAGE CD74ACT174...E OR M PACKAGE

(TOP VIEW)

CLR [] 1 1Q [] 2

1D 🛮 3

2D 🛮 4

2Q 🛮 5

3D **1**6

3Q 🛮 7

GND 8

SCHS344 - APRIL 2003

- Inputs Are TTL-Voltage Compatible
- Contain Six Flip-Flops With Single-Rail Outputs
- Buffered Inputs
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- ±24-mA Output Drive Current
  - Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers

## description/ordering information

The 'ACT174 devices are positive-edge-triggered D-type flip-flops with a direct clear ( $\overline{\text{CLR}}$ ) input and are designed for 4.5-V to 5.5-V V<sub>CC</sub> operation.

Information at the data (D) inputs that meets the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

#### ORDERING INFORMATION

TA	PDIP – E Tube Tube		ORDERABLE PART NUMBER	TOP-SIDE MARKING			
	PDIP – E	Tube	CD74ACT174E CD74ACT174				
55°C to 125°C	SOIC – M	Tube	CD74ACT174M	ACT174M			
–55°C to 125°C	301C - W	Tape and reel	CD74ACT174M96	ACT 174IVI			
	CDIP – F	Tube	CD54ACT174F3A	CD54ACT174F3A			

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## FUNCTION TABLE (each flip-flop)

	OUTPUT		
CLR	CLK	D	Q
L	Х	Х	L
Н	$\uparrow$	Н	Н
Н	$\uparrow$	L	L
Н	L	Χ	$Q_0$

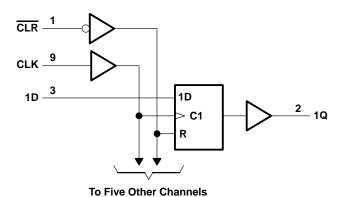


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SCHS344 - APRIL 2003

#### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Input clamp current, $I_{IK}$ ( $V_I < 0 \text{ V or } V_I > V_{CC}$ ) (see Note 1)	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 V or V <sub>O</sub> > V <sub>CC</sub> ) (see Note 1)	±50 mA
Continuous output current, $I_O$ ( $V_O > 0$ V or $V_O < V_{CC}$ )	±50 mA
Continuous current through V <sub>CC</sub> or GND	±150 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2): E package	67°C/W
M package	73°C/W
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 3)

		T <sub>A</sub> = 3	25°C		–55°C to 125°C		C to	UNIT
			MAX	MIN	MAX	MIN	MAX	
Vcc	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2		2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8		0.8	V
٧ <sub>I</sub>	Input voltage	0	VCC	0	VCC	0	VCC	V
٧o	Output voltage	0	VCC	0	VCC	0	VCC	V
IOH	High-level output current		-24		-24		-24	mA
loL	Low-level output current		24		24		24	mA
Δt/Δν	Input transition rise or fall rate		10		10		10	ns/V

NOTE 3: All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SCHS344 - APRIL 2003

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CON	Vcc	T <sub>A</sub> = 25°C		–55°C to 125°C		–40°C to 85°C		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX	
		I <sub>OH</sub> = -50 μA	4.5 V	4.4		4.4		4.4		
Vou	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	$I_{OH} = -24 \text{ mA}$	4.5 V	3.94		3.7		3.8		٧
VOH	v  = v H or v L	$I_{OH} = -50 \text{ mA}^{\dagger}$	5.5 V			3.85				V
		$I_{OH} = -75 \text{ mA}^{\dagger}$	5.5 V					3.85		
		I <sub>OL</sub> = 50 μA	4.5 V		0.1		0.1		0.1	
\/a.	\\.\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	I <sub>OL</sub> = 24 mA	4.5 V		0.36		0.5		0.44	٧
VOL	VI = VIH or VIL	$I_{OL} = 50 \text{ mA}^{\dagger}$	5.5 V				1.65			V
		$I_{OL} = 75 \text{ mA}^{\dagger}$	5.5 V						1.65	
lį	$V_I = V_{CC}$ or GND		5.5 V		±0.1		±1		±1	μΑ
Icc	$V_I = V_{CC}$ or GND,	IO = 0	5.5 V		8		160		80	μΑ
Δl <sub>CC</sub> ‡	$V_{I} = V_{CC} - 2.1 \text{ V}$	·	4.5 V to 5.5 V		2.4		3		2.8	mA
C <sub>i</sub>					10		10		10	pF

<sup>†</sup> Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C. ‡ Additional quiescent supply current per input pin, TTL inputs high, 1 unit load

#### **ACT INPUT LOAD TABLE**

INPUT	UNIT LOAD
Data	0.5
CLR	0.5
CLK	0.83

Unit Load is  $\Delta I_{CC}$  limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

# timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted)

			–55° 125		–40°( 85°	UNIT	
			MIN	MAX	MIN	MAX	
fclock	Clock frequency			80		91	MHz
	Pulse duration	CLR low	4		3.5		ns
t <sub>W</sub>	ruise duration	CLK high or low	6.2		5.4		115
t <sub>su</sub>	Setup time before CLK↑	Data	2		2		ns
th	Hold time, data after CLK↑		2.5		2.2		ns
t <sub>rec</sub>	Recovery time, before CLK↑	CLR↑			1.5		ns

## CD54ACT174, CD74ACT174 HEX D-TYPE FLIP-FLOPS WITH CLEAR

SCHS344 - APRIL 2003

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

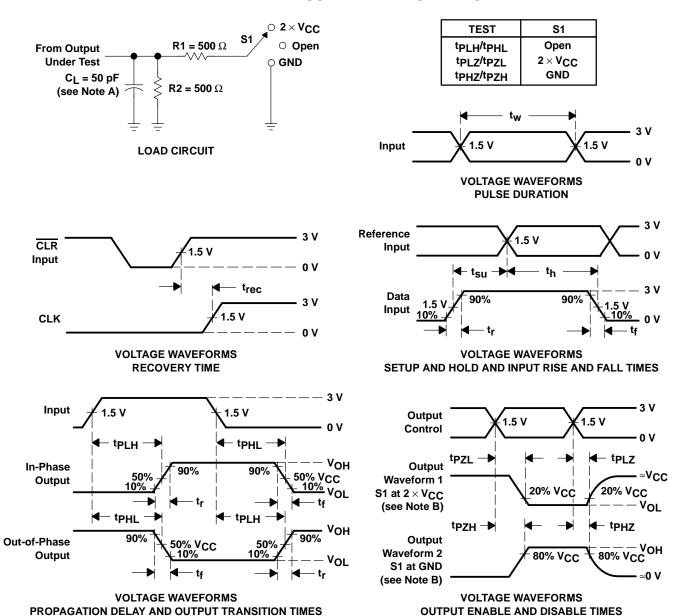
PARAMETER	FROM (INPUT)	TO (OUTPUT)	–55°( 125		–40°( 85°	UNIT	
	(INFOT)	(6611 61)	MIN	MAX	MIN	MAX	
f <sub>max</sub>			80		91		MHz
tPLH	CLK	Any Q	3.5	14	3.6	12.6	nc
<sup>t</sup> PHL	CER	Ally Q	3.5	14	3.6	12.6	ns
<sup>t</sup> PLH	CLR	Any Q	3.9	15.5	4	14.1	ns
<sup>t</sup> PHL	CLR	Ally Q	3.9	15.5	4	14.1	115

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

	PARAMETER	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	37	pF



#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and test-fixture capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \ \Omega$ ,  $t_f = 3 \ ns$ ,  $t_f = 3 \ ns$ . Phase relationships between waveforms are arbitrary.
- D. For clock inputs, f<sub>max</sub> is measured with the input duty cycle at 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F. tpLH and tpHL are the same as tpd.
- G. tp7I and tpZH are the same as ten.
- H. tpLZ and tpHZ are the same as tdis.
- I. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



#### PACKAGE OPTION ADDENDUM

www.ti.com 15-Oct-2009

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD54ACT174F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD74ACT174E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74ACT174EE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74ACT174M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT174M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT174M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT174M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT174ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT174MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74ACT174M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1





#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74ACT174M96	SOIC	D	16	2500	333.2	345.9	28.6

### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



## D (R-PDS0-G16)

#### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



## D (R-PDSO-G16)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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