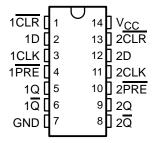
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- Controlled Baseline
 - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree[†]
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- Operating Range 2-V to 5.5-V V_{CC}
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

D OR PW PACKAGE (TOP VIEW)



description/ordering information

The SN74AHC74 dual positive-edge-triggered device is a D-type flip-flop.

A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

ORDERING INFORMATION

TA	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
55°C to 135°C	SOIC - D	Tape and reel	SN74AHC74MDREP	AHC74MEP	
–55°C to 125°C	TSSOP - PW	Tape and reel	SN74AHC74MPWREP	AHC74EP	

[‡] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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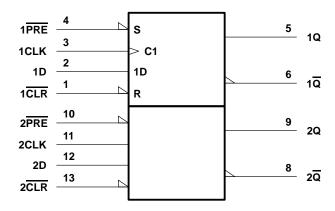
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FUNCTION TABLE (each flip-flop)

	INP	OUTI	PUTS		
PRE	CLR	CLK	D	Q	Q
L	Н	Х	Х	Н	L
Н	L	X	Χ	L	Н
L	L	X	Χ	H [†]	H [†]
Н	Н	\uparrow	Н	Н	L
Н	Н	\uparrow	L	L	Н
Н	Н	L	Χ	Q ₀	\overline{Q}_0

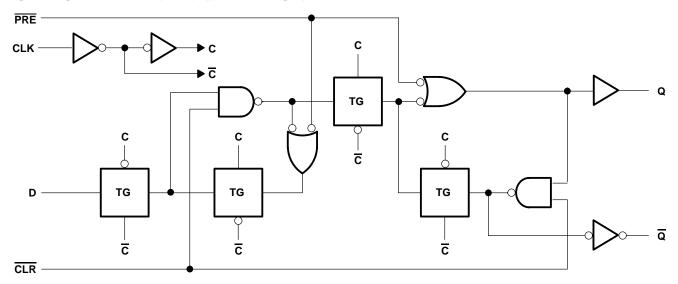
[†] This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

logic symbol‡



[‡]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram, each flip-flop (positive logic)





SN74AHC74-EP DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)	0.5 V to 7 V
Output voltage range, VO (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I _{IK} (V _I < 0)	–20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
PW package	113°C/W
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
VCC	Supply voltage		2	5.5	V
		V _{CC} = 2 V	1.5		
٧ıH	High-level input voltage	V _{CC} = 3 V	2.1		V
		$V_{CC} = 5.5 V$	3.85		
		V _{CC} = 2 V		0.5	
V_{IL}	Low-level input voltage V _{CC} = 3 V	$V_{CC} = 3 V$		0.9	V
		$V_{CC} = 5.5 \text{ V}$		1.65	
٧ _I	Input voltage		0	5.5	V
٧o	Output voltage		0	VCC	V
		V _{CC} = 2 V		-50	μΑ
ІОН	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4	mA
		$V_{CC} = 5 V \pm 0.5 V$		-8	IIIA
		V _{CC} = 2 V		50	μΑ
loL	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4	A
		$V_{CC} = 5 V \pm 0.5 V$		8	mA
A+/A>.	$V_{CC} = 3.3 \text{ V} \pm$			100	ns/V
Δt/Δv	Input transition rise or fall rate	$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		20	115/ V
T _A	Operating free-air temperature		-55	125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74AHC74-EP DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS	Vaa	T,	չ = 25°C	;	MINI	MAY	UNIT
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	UNIT
		2 V	1.9	2		1.9		
	I _{OH} = -50 μA	3 V	2.9	3		2.9		
Voн		4.5 V	4.4	4.5		4.4		V
	I _{OH} = -4 mA	3 V	2.58			2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		
		2 V			0.1		0.1	
	I _{OL} = 50 μA	3 V			0.1		0.1	
V _{OL}		4.5 V			0.1		0.1	V
	$I_{OL} = 4 \text{ mA}$	3 V			0.36		0.5	
	$I_{OL} = 8 \text{ mA}$	4.5 V			0.36		0.5	
lį	$V_I = 5.5 \text{ V or GND}$	0 V to 5.5 V			±0.1		±1	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		20	μΑ
Ci	V _I = V _{CC} or GND	5 V		2	10			pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

			T _A = 2	25°C	MIN	MAX	UNIT
					IVIIIN	IVIAA	UNIT
4 D.	Pulse duration	PRE or CLR low	6		7		no
t _W	ruise duration	CLK	6		7		ns
Γ.	Octors that a harfage OLIVA	Data	6		7		
t _{su}	Setup time before CLK↑	PRE or CLR inactive	5		5		ns
th	Hold time, data after CLK↑		0.5		0.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

			T _A = 25°C		MIN MAX		UNIT
			MIN	MAX	IVIIIV	WAA	UNII
	t _w Pulse duration	PRE or CLR low	5		5		
t _W	Fulse duration	CLK	5		5		ns
	Octor Core haters OLKA	Data	5		5		
t _{su} S	Setup time before CLK↑	PRE or CLR inactive	3 3			ns	
t _h	Hold time, data after CLK↑	_	0.5		0.5		ns

SN74AHC74-EP DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T,	Վ = 25° C	;	MIN	MAX	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIN	IVIAA	UNIT
f			C _L = 15 pF	80	125		70		MHz
f _{max}			C _L = 50 pF	50	75		45		IVITZ
tPLH	<u> </u>	0	C _I = 15 pF		7.6	12.3	1	14.5	ns
t _{PHL}	PRE or CLR	Q or Q	CL = 15 pr		7.6	12.3	1	14.5	110
tPLH	CLK	0	C: - 15 pE		6.7	11.9	1	14	20
t _{PHL}	CLK	Q or \overline{Q} $C_L = 15 pF$	CL = 15 pr		6.7	11.9	1	14	ns
tPLH	DDE OLD	0	C 50 pE		10.1	15.8	1	18	ns
t _{PHL}	PRE or CLR	Q or $\overline{\mathbb{Q}}$	$C_L = 50 \text{ pF}$		10.1	15.8	1	18	115
t _{PLH}	CLK	Q or $\overline{\mathbb{Q}}$	C: - 50 pF		9.2	15.4	1	17.5	no
t _{PHL}	CLK	Q OF Q	C _L = 50 pF		9.2	15.4	1	17.5	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T,	գ = 25°C	;	MIN	MAX	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIV	IVIAA	ONII
			C _L = 15 pF	130	170		110		MHz
fmax			C _L = 50 pF	90	115		75		IVITIZ
t _{PLH}	DDE OLD	0	C _L = 15 pF		4.8	7.7	1	9	ns
t _{PHL}	PRE or CLR	Q or \overline{Q}	OL = 13 pi		4.8	7.7	1	9	113
^t PLH	CLK	0 0	C _L = 15 pF		4.6	7.3	1	8.5	ns
t _{PHL}	CLK	Q or \overline{Q}	OL = 13 pr		4.6	7.3	1	8.5	110
^t PLH	PRE or CLR	Q or Q	C _L = 50 pF		6.3	9.7	1	11	ns
^t PHL	PRE OF CLR	Q or Q	CL = 30 pr		6.3	9.7	1	11	115
^t PLH	CLK	Q or Q	C _L = 50 pF		6.1	9.3	1	10.5	ns
^t PHL	CLK	300	CL = 50 pr		6.1	9.3	1	10.5	110

noise characteristics, $V_{CC} = 5 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^{\circ}\text{C}$ (see Note 4)

	PARAMETER						
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.8	V			
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.8	V			
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}	4.7		V			
V _{IH(D)}	High-level dynamic input voltage	3.5		V			
V _{IL(D)}	Low-level dynamic input voltage		1.5	V			

NOTE 4: Characteristics are for surface-mount packages only.

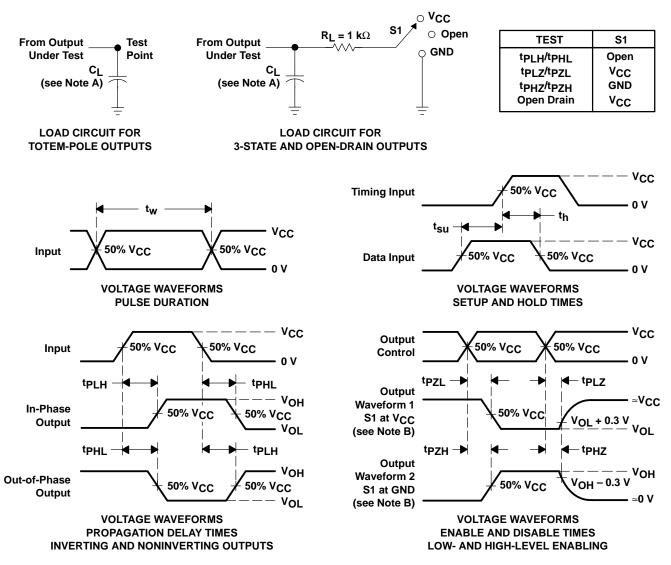
operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
Γ	Power dissipation capacitance	No load, f = 1 MHz	32	pF



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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq 3$ ns. $t_f \leq 3$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms







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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AHC74MDREP	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC74MPWREP	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/03652-01XE	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/03652-01YE	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74AHC74-EP:

Catalog: SN74AHC74Military: SN54AHC74

NOTE: Qualified Version Definitions:

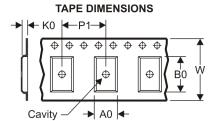
- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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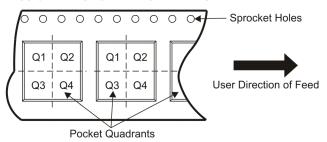
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

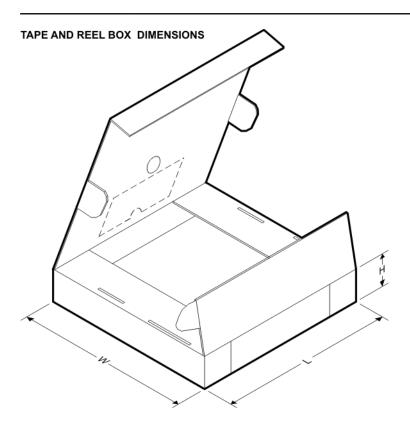
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC74MDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC74MPWREP	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC74MDREP	SOIC	D	14	2500	333.2	345.9	28.6
SN74AHC74MPWREP	TSSOP	PW	14	2000	346.0	346.0	29.0

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