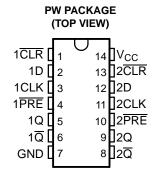


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FEATURES

- Controlled Baseline
 - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of 55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree (1)
- 2-V to 5.5-V V_{CC} Operation
- Max t_{nd} of 13 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 >2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- Supports Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



DESCRIPTION/ORDERING INFORMATION

These dual positive-edge-triggered D-type flip-flops are designed for 2-V to 5.5-V V_{CC} operation.

A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) inputs sets or resets the outputs, regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the data (D) inputs meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	TSSOP - PW	Reel of 2000	SN74LV74AMPWREP	LV74AEP

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

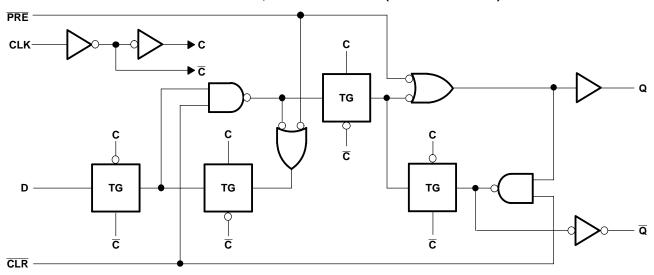


FUNCTION TABLE

	INP	UTS		OUTI	PUTS
PRE	CLR	CLK	D	Q	Q
L	Н	Χ	Χ	Н	L
Н	L	Χ	Χ	L	Н
L	L	Χ	Χ	H ⁽¹⁾	H ⁽¹⁾
Н	Н	\uparrow	Н	Н	L
Н	Н	\uparrow	L	L	Н
Н	Н	L	Χ	Q_0	\overline{Q}_0

(1) This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

LOGIC DIAGRAM, EACH FLIP-FLOP (POSITIVE LOGIC)





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Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
VI	Input voltage range (2)		-0.5	7	V
Vo	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		-0.5	7	V
Vo	Output voltage range (2)(3)		-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	V ₁ < 0		-20	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance (4)			113	°C/W
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ This value is limited to 5.5 V maximum.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.





Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
		V _{CC} = 2 V	1.5		
.,	High lavel innerteedle as	V _{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		V
V_{IH}	High-level input voltage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	$V_{CC} \times 0.7$		V
		V _{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		
		V _{CC} = 2 V		0.5	
\/	Low level input valte as	V _{CC} = 2.3 V to 2.7 V		$V_{\text{CC}}\times 0.3$	V
V_{IL}	Low-level input voltage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		$V_{CC} \times 0.3$	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$V_{CC} \times 0.3$	
V _I	Input voltage		0	5.5	V
Vo	Output voltage		0	V_{CC}	V
		V _{CC} = 2 V		-50	μΑ
	High level cutout current	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		-2	
I _{OH}	High-level output current	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		-6	mA
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		-12	
		V _{CC} = 2 V		50	μΑ
	Low lovel output ourrent	V _{CC} = 2.3 V to 2.7 V		2	
l _{OL}	Low-level output current	V _{CC} = 3 V to 3.6 V		6	mA
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		12	
		V _{CC} = 2.3 V to 2.7 V		200	
Δt/Δν	Input transition rise or fall rate	V _{CC} = 3 V to 3.6 V		100	ns/V
		V _{CC} = 4.5 V to 5.5 V		20	
T _A	Operating free-air temperature		-55	125	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP	MAX	UNIT
	$I_{OH} = -50 \mu A$	2 V to 5.5 V	V _{CC} - 0.1			
V	$I_{OH} = -2 \text{ mA}$	2.3 V	2			V
V _{OH}	$I_{OH} = -6 \text{ mA}$	3 V	2.48			V
	$I_{OH} = -12 \text{ mA}$	4.5 V	3.8			
	$I_{OL} = 50 \mu A$	2 V to 5.5 V			0.1	
V	$I_{OL} = 2 \text{ mA}$	2.3 V			0.4	V
V _{OL}	I _{OL} = 6 mA	3 V			0.44	V
	I _{OL} = 12 mA	4.5 V			0.55	
I _I	V _I = 5.5 V or GND	0 to 5.5 V			±1	μΑ
I _{CC}	$V_1 = V_{CC}$ or GND, $I_0 = 0$	5.5 V			20	μΑ
I _{off}	V_I or $V_O = 0$ to 5.5 V	0			5	μΑ
<u> </u>	$V_{L} = V_{CC}$ or GND	3.3 V		2		n.E
C _i	AI = ACC OL GIAD	5 V		2		pF



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Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 2.5 V \pm 0.2 V (unless otherwise noted) (see Figure 1)

	PARAMETER				MIN	MAX	UNIT	
	FARAMETER		MIN	MAX	IVIIIV	WAX	UNIT	
	Dulas duration	PRE or CLR low	8		9		no	
ι _W	t _w Pulse duration	CLK	8		9		ns	
	Setup time before CLK↑	Data	8		9			
t _{su} Setup time	Setup time before CENT	PRE or CLR inactive	7		7		ns	
t _h	Hold time, data after CLK↑		0.5		0.5		ns	

Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

	PARAMET	T _A = 2	:5°C	MIN	MAX	UNIT		
	PARAMEI	EK	MIN	MAX	IVIIIN	WAX	UNIT	
	t Pulse duration	PRE or CLR low	6		7		no	
'W	Pulse duration	CLK	6		7		ns	
	Setup time hefere CLK [↑]	Data	6		7		ns	
ı _{su} se	Setup time before CLK↑	PRE or CLR inactive	5		5			
t _h	Hold time, data after CLK↑		1.45		2.15		ns	

Timing Requirements

over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

	D. F.	AMETER	$T_A = 2$	25°C	MIN	MAY		
	PAR	MIN	MAX	MIN	MAX	UNIT		
	Dulas duration	PRE or CLR low	5		5			
ι _w	t _w Pulse duration	CLK	5		5		ns	
	Satura tima hafara CLV^	Data	5		5		ns	
t _{su} Seti	Setup time before CLK↑	PRE or CLR inactive	3		3			
t _h	Hold time, data after CLK↑		1.45		2.15		ns	

Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 2.5 V \pm 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T _A = 25°C		MIN	MAX	UNIT	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIN		UNIT
f _{max}			$C_L = 50 pF$	30	70		25		MHz
	PRE or CLR	Q or Q	0 50 -5		13	17.4	1	20	no
^L pd	CLK	QUIQ	$C_L = 50 pF$		14.2	20	1	23	ns





Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T _A = 25°C		MIN MAX		UNIT	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIN	IVIAA	ONII
f _{max}			C _L = 50 pF	50	90		45		MHz
	PRE or CLR	Q or Q	C - 50 pF		9.2	15.8	1	18	no
^L pd	CLK	QUIQ	$C_L = 50 \text{ pF}$		10.2	15.4	1	18	ns

Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T _A = 25°C		MIN	MAX	UNIT	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIN	WAX	UNII
f _{max}			C _L = 50 pF	90	140		75		MHz
4	PRE or CLR	Q or Q	C _ 50 pF		6.6	9.7	1	12	20
l _{pd}	CLK	QUIQ	$C_L = 50 pF$		7.2	9.9	1	13	ns

Noise Characteristics⁽¹⁾

 V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

	PARAMETER	MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.1	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		0	-0.8	V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		3.2		V
V _{IH(D)}	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

⁽¹⁾ Characteristics are for surface-mount packages only.

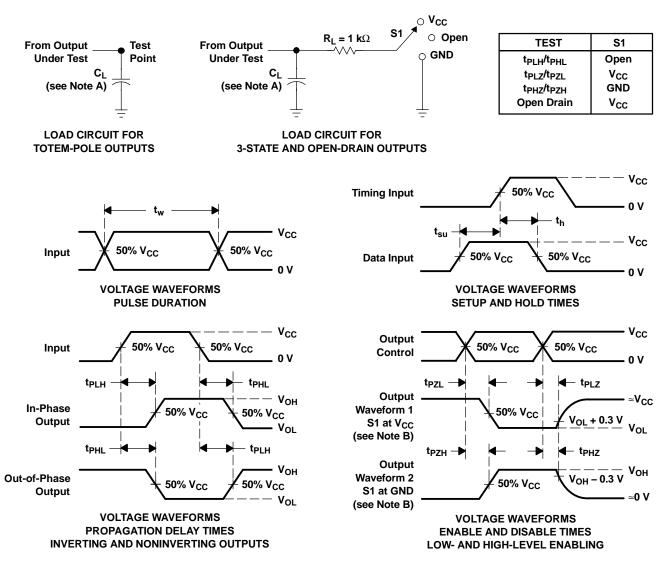
Operating Characteristics

 $T_A = 25^{\circ}C$

PARAMETER			TEST CONDITIONS			UNIT
0	Dower discination conscitones	C	f = 10 MHz	3.3 V	21	~ F
C_{pd}	Power dissipation capacitance	$C_L = 50 \text{ pF},$	I = 10 WIHZ	5 V	23	p⊦

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r \leq$ 3 ns, $t_f \leq$ 3 ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PHL} and t_{PLH} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuits and Voltage Waveforms

9-May-2012

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LV74AMPWREP	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart
V62/06605-01XE	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LV74A-EP:

Catalog: SN74LV74A

Automotive: SN74LV74A-Q1





9-May-2012

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

www.ti.com 30-Jul-2010

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV74AMPWREP	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 30-Jul-2010



*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
S	N74LV74AMPWREP	TSSOP	PW	14	2000	346.0	346.0	29.0

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
 - Sody length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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