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- 3-State Bus Driving Inverting Outputs
- Buffered Control Inputs
- Package Options Include Plastic Small-Outline (DW), Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

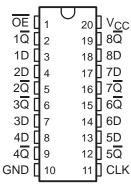
#### description

These octal D-type edge-triggered flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

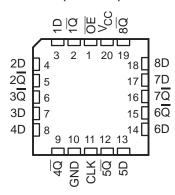
On the positive transition of the clock (CLK) input, the  $\overline{Q}$  outputs are set to the complement of the logic states set up at the data (D) inputs. The 'ALS534A and SN74AS534 have inverted outputs, but otherwise are functionally equivalent to the 'ALS374A and SN74AS374.

A buffered output-enable ( $\overline{OE}$ ) input places the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

SN54ALS534A . . . J PACKAGE SN74ALS534A, SN74AS534 . . . DW OR N PACKAGE (TOP VIEW)



SN54ALS534A . . . FK PACKAGE (TOP VIEW)



OE does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS534A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS534A and SN74AS534 are characterized for operation from 0°C to 70°C.

## FUNCTION TABLE (each flip-flop)

	INPUTS	OUTPUT	
OE	CLK	D	Q
L	$\uparrow$	Н	L
L	$\uparrow$	L	Н
L	H or L	Χ	$\overline{Q}_0$
Н	X	Χ	Z



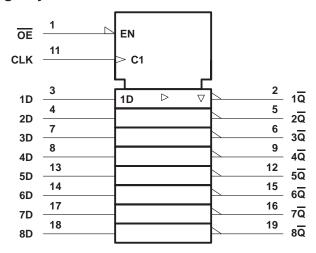
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



## SN54ALS534A, SN74ALS534A, SN74AS534 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

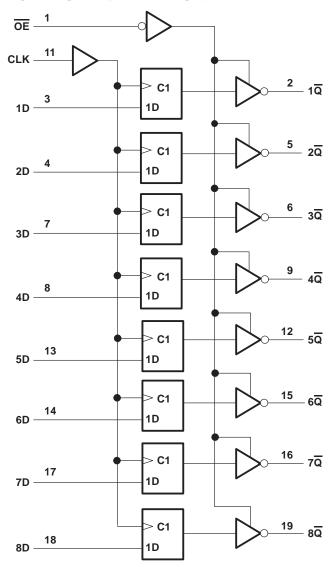
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#### logic symbol<sup>†</sup>



<sup>&</sup>lt;sup>†</sup>This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### logic diagram (positive logic)



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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V <sub>CC</sub>	7 V
Input voltage, V <sub>I</sub>	
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, TA: SN54ALS534A	–55°C to 125°C
SN74ALS534A	0°C to 70°C
Storage temperature range, Teta	

#### recommended operating conditions

		SNS	54ALS53	4A	SN7	74ALS53	4A	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.7			0.8	V
IOH	High-level output current			-1			-2.6	mA
lOL	Low-level output current			12			24	mA
fclock	Clock frequency	0		30	0		35	MHz
t <sub>W</sub>	Pulse duration, CLK high or low	16.5			14			ns
t <sub>su</sub>	Setup time, data before CLK↑	10			10			ns
t <sub>h</sub>	Hold time, data after CLK↑	0			0			ns
TA	Operating free-air temperature	-55		125	0		70	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

D.	DAMETED	TEST CA	ONDITIONS	SN	54ALS53	34A	SN7	74ALS53	4A	UNIT	
	RAMETER	lesi Co	ONDITIONS	MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNII	
٧ <sub>IK</sub>		V <sub>CC</sub> = 4.5 V,	$I_1 = -18 \text{ mA}$			-1.5			-1.5	V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OH} = -0.4 \text{ mA}$	V <sub>CC</sub> -2	2		VCC -2	2			
∨он		V00 - 45 V	$I_{OH} = -1 \text{ mA}$	2.4	3.3					V	
		V <sub>C</sub> C = 4.5 V	$I_{OH} = -2.6 \text{ mA}$				2.4	3.2			
Vol		V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 12 mA		0.25	0.4		0.25	0.4	V	
VOL		VCC = 4.5 V	I <sub>OL</sub> = 24 mA					0.35	0.5	V	
lozh		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V			20			20	μΑ	
lozL		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.4 V			-20			-20	μΑ	
Ιį		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 7 V			0.1			0.1	mA	
ΙΗ		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			20			20	μΑ	
I	CLK, OE	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	V <sub>I</sub> = 0.4 V			-0.1			-0.1	mA	
ll l	D	V <sub>CC</sub> = 5.5 V,	V  = 0.4 V			-0.2			-0.2	IIIA	
IO§		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	-20		-112	-30		-112	mA	
			Outputs high		11	19		11	19		
ICC		V <sub>CC</sub> = 5.5 V	Outputs low		19	28		19	28	mA	
			Outputs disabled		10	31		20	31		

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

<sup>§</sup> The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## SN54ALS534A, SN74ALS534A, SN74AS534 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

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#### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CL R1: R2:	C = 4.5 \ = 50 pF, = 500 Ω, = 500 Ω, = MIN to			UNIT
			SN54AL	S534A	SN74AL	S534A	
			MIN	MAX	MIN	MAX	
f <sub>max</sub>			30		35		MHz
tPLH	CLK	A	3	17	3	12	ns
t <sub>PHL</sub>	OLK	Any Q	4	18	4	16	115
<sup>t</sup> PZH	ŌĒ	Any Q	3	19	3	17	ns
t <sub>PZL</sub>	OE .	Any Q	4	20	4	18	115
<sup>t</sup> PHZ	ŌĒ	Any Q	1	12	1	10	ne
t <sub>PLZ</sub>	OE .	Ally Q	1	25	2	14	ns

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V <sub>CC</sub>	7 V
Input voltage, V <sub>I</sub>	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T <sub>A</sub> : SN74AS534	0°C to 70°C
Storage temperature rang, T <sub>stg</sub>	65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions

			SI	174AS53	34	UNIT
			MIN			
VCC	Supply voltage		4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			V	
$V_{IL}$	Low-level input voltage				0.8	V
IOH	High-level output current				-15	mA
lOL	Low-level output current				48	mA
fclock	Clock frequency		0		125	MHz
	Pulse duration	CLK high	4			
t <sub>W</sub>	ruise duration	CLK low	3			ns
t <sub>su</sub>	Setup time, data before CLK↑		2			ns
t <sub>h</sub>	Hold time, data after CLK↑		2			ns
TA	Operating free-air temperature		0		70	°C

## SN54ALS534A, SN74ALS534A, SN74AS534 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS168B - APRIL 1982 - REVISED JULY 1996

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	DADAMETED	TEST CONF	SN	UNIT			
	PARAMETER	TEST COND	IIIONS	MIN	TYP <sup>†</sup>	MAX	UNII
VIK		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA			-1.2	V
VOH		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	I <sub>OH</sub> = −2 mA	V <sub>CC</sub> -2			V
		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -15 \text{ mA}$	2.4	3.3		V
VOL		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 48 mA		0.34	0.5	V
lozh		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V			50	μΑ
lozL		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V			-50	μΑ
ΙĮ		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 7 V			0.1	mA
lін		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			20	μΑ
1	OE, CLK	V 55V	V: 0.4.V			-0.5	Λ
¹IL	D	$V_{CC} = 5.5 V$	V <sub>I</sub> = 0.4 V			-2	mA
lo‡		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	-30		-112	mA
			Outputs high		77	120	
ICC		$V_{CC} = 5.5 V$	Outputs low		84	128	mA
			Outputs disabled		84	128	

<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

#### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 C <sub>L</sub> = 50 pF R1 = 500 Ω R2 = 500 Ω T <sub>A</sub> = MIN to SN74/	;, <u>2</u> , <u>2</u> ,	UNIT
f <sub>max</sub>			125		MHz
tpLH	CLK	. =	3	8	20
<sup>t</sup> PHL	CLK	Any Q	4	9	ns
<sup>t</sup> PZH	<del></del>	. =	2	6	200
t <sub>PZL</sub>	ŌĒ	Any Q	3	10	ns
<sup>t</sup> PHZ	ŌĒ	Any Q	2	6	ns
<sup>t</sup> PLZ	OE .	Ally Q	2	6	115

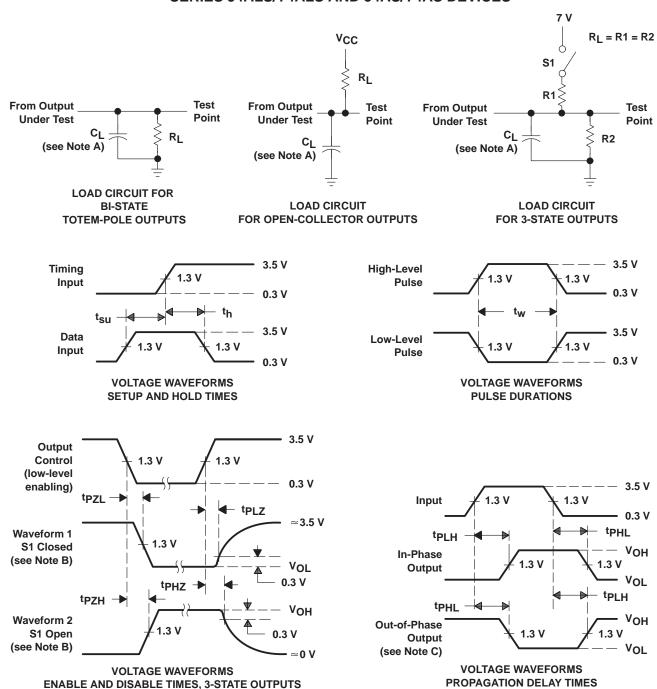
<sup>§</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



<sup>&</sup>lt;sup>‡</sup> The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics:  $PRR \le 1$  MHz,  $t_f = t_f = 2$  ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms





7-Jun-2010

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN54ALS534J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	Samples Not Available
SN74ALS534ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS534ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS534ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS534ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS534ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS534ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS534AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74ALS534AN3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	Samples Not Available
SN74ALS534ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN74ALS534ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS534ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALS534ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74AS534DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	Samples Not Available
SN74AS534DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	Samples Not Available
SN74AS534N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	Samples Not Available
SNJ54ALS534FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	Samples Not Available
SNJ54ALS534J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	Samples Not Available

<sup>(1)</sup> The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.



#### PACKAGE OPTION ADDENDUM

7-Jun-2010

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### OTHER QUALIFIED VERSIONS OF SN74ALS534A:

Military: SN54ALS534A

NOTE: Qualified Version Definitions:

Military - QML certified for Military and Defense Applications



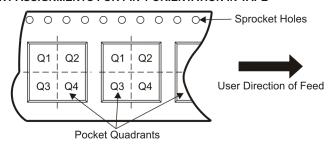
#### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

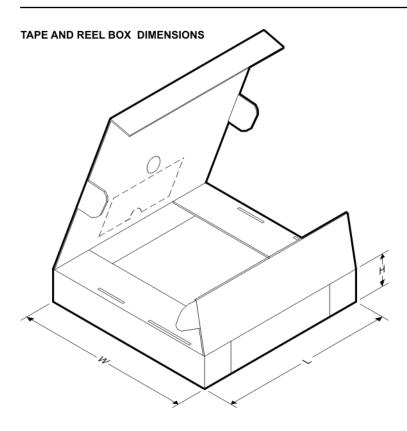
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device		Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS534ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74ALS534ANSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1





\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS534ADWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74ALS534ANSR	SO	NS	20	2000	346.0	346.0	41.0

### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

#### PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



#### **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

## 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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