SN54ABT162823A . . . WD PACKAGE

SN74ABT162823A ... DGG OR DL PACKAGE

SCBS666B - JULY 1996 - REVISED JUNE 2004

- Members of the Texas Instruments Widebus™ Family
- Output Ports Have Equivalent 25-Ω Series Resistors So No External Resistors Are Required
- Typical V_{OLP} (Output Ground Bounce)
 <1 V at V_{CC} = 5 V, T_A = 25°C
- High-Impedance State During Power Up and Power Down
- I_{off} and Power-Up 3-State Support Hot Insertion
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout

description/ordering information

These 18-bit bus-interface flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The 'ABT162823A devices can be used as two 9-bit flip-flops or one 18-bit flip-flop. With the clock-enable (\overline{CLKEN}) input low, the D-type flip-flops enter data on the low-to-high transitions of the clock. Taking \overline{CLKEN} high disables the clock buffer, thus latching the outputs. Taking the clear (\overline{CLR}) input low causes the Q outputs to go low independently of the clock.

	(TOP VI	EW)	_
			_
1CLR	1	56]1CLK
1OE	2		1CLKEN
1Q1 [3	54]1D1
GND [4	53	GND
1Q2 [5	52]1D2
1Q3 [6	51	1D3
V _{CC} [7	50]V _{CC}
1Q4 [8	49]1D4
1Q5 [9	48]1D5
1Q6 [10	47]1D6
GND [11		GND
1Q7 [12	45]1D7
1Q8 [13	44	1D8
1Q9 [14	43]1D9
2Q1 [15	42	2D1
2Q2 [16	41	2D2
2Q3 [17	40	2D3
GND [18	39] GND
2Q4 [19	38	2D4
2Q5 [20	37	2D5
2Q6 [21	36	2D6
V _{CC} [22	35]V _{CC}
2Q7 [23	34	2D7
2Q8 [24	33	2D8
GND [25	32	GND
2Q9 [26	31	2D9
20E [27	30	2CLKEN
2CLR	28	29]2CLK

ORDERING INFORMATION

TA	PACK/	AGE [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SSOP – DL	Tube	SN74ABT162823ADL	
–40°C to 85°C	550P - DL	Tape and reel	SN74ABT162823ADLR	ABT162823A
Т	TSSOP – DGG	Tape and reel	SN74ABT162823ADGGR	ABT162823A
–55°C to 125°C	CFP – WD	Tube	SNJ54ABT162823AWD	SNJ54ABT162823AWD

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN54ABT162823A, SN74ABT162823A **18-BIT BUS-INTERFACE FLIP-FLOPS** WITH 3-STATE OUTPUTS SCBS666B - JULY 1996 - REVISED JUNE 2004

description/ordering information (continued)

A buffered output-enable (\overline{OE}) input places the nine outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components. \overline{OE} does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

These devices are fully specified for hot-insertion applications using Ioff and power-up 3-state. The Ioff circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

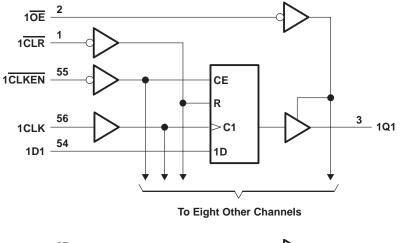
To ensure the high-impedance state during power up or power down, $\overline{\mathsf{OE}}$ shall be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

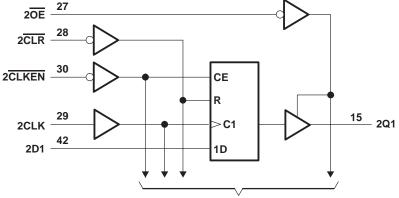
		INPUTS			OUTPUT
OE	CLR	CLKEN	CLK	D	Q
L	L	Х	Х	Х	L
L	Н	L	\uparrow	Н	Н
L	Н	L	\uparrow	L	L
L	Н	L	L	Х	Q ₀
L	Н	Н	Х	Х	Q ₀
н	Х	Х	Х	Х	Z

FUNCTION TABLE (each 9-bit flip-flop)



logic diagram (positive logic)





To Eight Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, Vo	–0.5 V to 5.5 V
Current into any output in the low state, IO	30 mA
Input clamp current, I _{IK} (V _I < 0)	–18 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	64°C/W
DL package	56°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Note 3)

			SN54ABT1	62823A	SN74ABT1	62823A	
			MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2	Å	2		V	
VIL	Low-level input voltage		0.8		0.8	V	
VI	Input voltage	0 0	Vcc	0	VCC	V	
ЮН	High-level output current		1	-3		-12	mA
IOL	Low-level output current		200	8		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled	201	10		10	ns/V
Δt/ΔV _{CC}	Input transition rise or fall rate		Q 200		200		μs/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			Т	A = 25°C	;	SN54ABT1	62823A	SN74ABT1	62823A	
PARAMETER	TEST CO	NDITIONS	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	UNIT
VIK	V _{CC} = 4.5 V,	I _I = -18 mA			-1.2		-1.2		-1.2	V
	V _{CC} = 4.5 V,	I _{OH} = -1 mA	2.5			2.5		2.5		
	V _{CC} = 5 V,	I _{OH} = -1 mA	3			3		3		v
VOH		$I_{OH} = -3 \text{ mA}$	2.4			2.4		2.4		V
	$V_{CC} = 4.5 V$	$I_{OH} = -12 \text{ mA}$	2*					2		
		I _{OL} = 8 mA		0.4			0.8		0.65	V
VOL	$V_{CC} = 4.5 V$	I _{OL} = 12 mA			0.8*				0.8	V
Ц	V _{CC} = 5.5 V,	$V_I = V_{CC} \text{ or } GND$			±1		±1		±1	μA
IOZPU	$V_{CC} = 0 \text{ to } 2.1 \text{ V},$ $V_{O} = 0.5 \text{ V to } 2.7 \text{ V},$			±50		4±50		±50	μA	
IOZPD	$V_{CC} = 2.1 \text{ V to 0},$ $V_{O} = 0.5 \text{ V to 2.7 V},$			±50	CTD	±50		±50	μA	
IOZH [‡]	V _{CC} = 5.5 V,	V _O = 2.7 V			10	20	10		10	μA
^I OZL [‡]	V _{CC} = 5.5 V,	V _O = 0.5 V			-10	PP C	-10		-10	μA
l _{off}	$V_{CC} = 0,$	VI or VO \leq 4.5 V			±100	Y			±100	μA
ICEX	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high			50		50		50	μA
١ _O §	V _{CC} = 5.5 V,	V _O = 2.5 V	-25	-55	-100	-25	-100	-25	-100	mA
	V _{CC} = 5.5 V,	Outputs high			0.5		0.5		0.5	
ICC	$I_{O} = 0,$	Outputs low			80		80		80	mA
	$V_{I} = V_{CC}$ or GND	Outputs disabled			0.5		0.5		0.5	
∆ICC [¶]	$V_{CC} = 5.5 V$, One inp Other inputs at V_{CC}				1.5		1.5	1.5		mA
Ci	VI = 2.5 V or 0.5 V			3.5						pF
Co	V _O = 2.5 V or 0.5 V			9						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

[†] All typical values are at V_{CC} = 5 V.

[‡] The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL-voltage level, rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

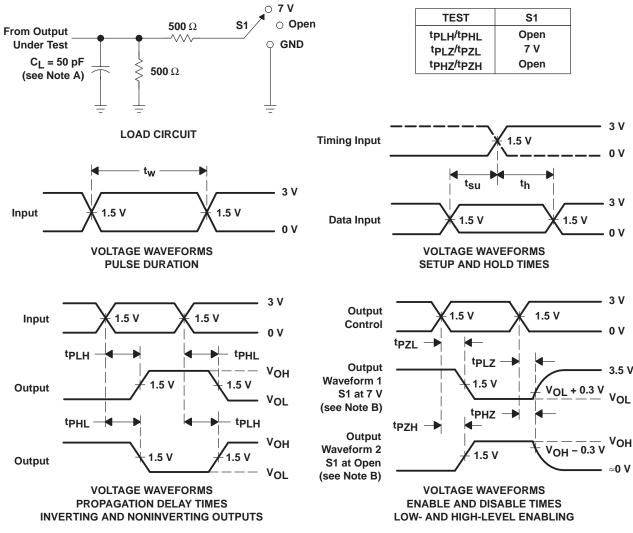
			V _{CC} =	= 5 V, 25°C	SN54ABT1	62823A	SN74ABT1	62823A	UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
fclock	Clock frequency			150		150		150	MHz	
	Delas destina	CLR low	3.3		3.3	N:	3.3			
tw	Pulse duration	CLK high or low	3.3		3.3	N.	3.3		ns	
		CLR inactive	1.6		2 2	5	1.6			
t _{su}	Setup time before CLK↑	Data	2		2		2		ns	
		CLKEN low	2.8		2,8		2.8			
		Data	1.2		21.2		1.2			
^t h	Hold time after CLK↑	CLKEN low	0.6		0.6		0.6		ns	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO	V _{CC} = 5 V, T _A = 25°C			SN54ABT162823A		SN74ABT162823A		UNIT
	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			150			150		150		MHz
^t PLH	CLK	Q	2.3	4.6	6.2	2.3	8.4	2.3	7.5	
^t PHL	CLK		2.8	4.6	6.1	2.8	A 7.1	2.8	6.7	5.7 ns
^t PHL	CLR	Q	2.8	5	6.3	2.8	7.2	2.8	7	ns
^t PZH	OE	0	1.7	3.8	5	1.7	5.8	1.7	5.9	
^t PZL	OE	Q	3	5	6.1	3	7.2	3	7	ns
^t PHZ	OE		2.6	4.8	6.1	2.6	7.3	2.6	6.6	
^t PLZ	OE	Q	1.9	4.6	6.7	1.9	10.2	1.9	9	ns



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PARAMETER MEASUREMENT INFORMATION

NOTES: A. C₁ includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{O} = 50 Ω , $t_{f} \leq$ 2.5 ns. $t_{f} \leq$ 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms





PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
74ABT162823ADGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74ABT162823ADGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT162823ADGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT162823ADL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ABT162823ADLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and pa

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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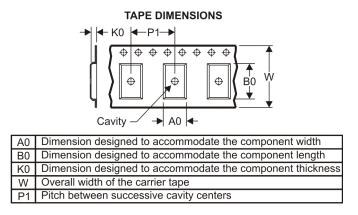
PACKAGE MATERIALS INFORMATION

www.ti.com

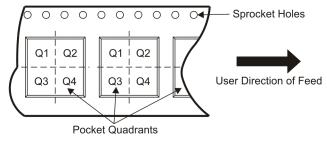
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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT162823ADGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

29-Jul-2011



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT162823ADGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0

MECHANICAL DATA

MSSO001C - JANUARY 1995 - REVISED DECEMBER 2001

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

DL (R-PDSO-G**)



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118



MECHANICAL DATA

MTSS003D - JANUARY 1995 - REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



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