INTEGRATED CIRCUITS

DATA SHEET

74F534Octal D flip-flop, inverting (3-State)

Product specification Supersedes data of 1999 Jan 08 IC15 Data Handbook





Octal D flip-flop, inverting (3-State)

74F534

FEATURES

- 8-bit positive edge-triggered register
- 3-State inverting output buffers
- Common 3-State Output register
- Independent register and 3-State buffer operation

DESCRIPTION

The 74F534 is an 8-bit edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable $(\overline{\text{OE}})$ control gates.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's \overline{Q} output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The

active Low Output Enable (\overline{OE}) controls all eight 3-State buffers independent of the latch operation. When \overline{OE} is Low, the latched or transparent data appears at the outputs. When \overline{OE} is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

TYPE	TYPICAL f _{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F534	165MHz	51mA

ORDERING INFORMATION

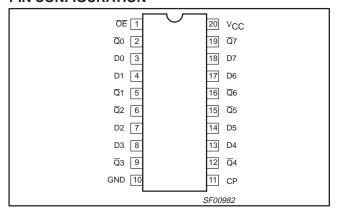
DESCRIPTION	$ \begin{array}{c} \text{COMMERCIAL} \\ \text{RANGE} \\ \text{V}_{\text{CC}} = 5\text{V} \pm \! 10\%, \\ \text{T}_{amb} = 0^{\circ}\text{C to +} 70^{\circ}\text{C} \end{array} $	PKG DWG#	
20-Pin Plastic DIP	N74F534N	SOT146-1	
20-Pin Plastic SOL	N74F534D	SOT163-1	

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

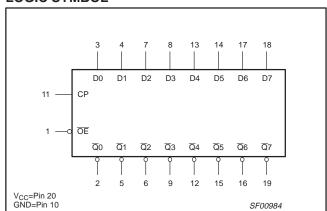
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D7	Data inputs	1.0/1.0	20μA/0.6mA
ŌĒ	Output Enable input (active Low)	1.0/1.0	20μA/0.6mA
СР	Clock Pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
<u>Q</u> 0 - <u>Q</u> 7	Data outputs	150/40	3.0mA/24mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



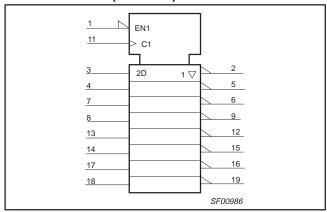
LOGIC SYMBOL



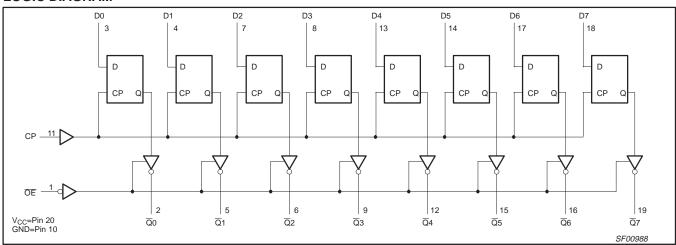
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LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

	INPUTS		INTERNAL	OUTPUTS	OPERATING MODES		
OE	CP Dn		REGISTER	<u>Q</u> 0 − <u>Q</u> 7	OPERATING MODES		
L	↑	1	L	Н	Lood and road register		
L	↑	h	Н	L	Load and read register		
L		Х	NC	NC	Hold		
Н		Х	NC	Z	Disable cutoute		
Н	1	Dn	Dn	Z	Disable outputs		

H = High voltage level

h = High voltage level one setup time prior to the Low-to-High clock transition

= Low voltage level

= Low voltage level one setup time prior to the Low-to-High clock transition

NC= No change

X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↑ = Not a Low-to-High clock transition

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	-0.5 to +7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	−30 to +5.0	mA
V _{OUT}	Voltage applied to output in High output state	−0.5 to +V _{CC}	V
l _{OUT}	Current applied to output in Low output state	48	mA
T _{amb}	Operating free-air temperature range	0 to +70	°C
T _{stg}	Storage temperature	-65 to +125	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		UNIT			
STIVIBUL	PARAMETER	MIN	TYP	MAX	UNII	
V _{CC}	Supply voltage	4.5	5.0	5.5	V	
V _{IH}	High-level input voltage	2.0			V	
V _{IL}	Low-level input voltage			0.8	V	
I _{IK}	Input clamp current			-18	mA	
I _{OH}	High-level output current			-3	mA	
I _{OL}	Low-level output current			24	mA	
T _{amb}	Operating free-air temperature range	0		70	°C	

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

OVMDOL	DADAMETER	TF0T 00	NDITIONO	1				
SYMBOL	PARAMETER	l lesi co	TEST CONDITIONS ¹					UNIT
V	Lieb lovel output voltage	V _{CC} = MIN, V _{II} =	±10%V _{CC}	2.4			V	
V _{OH}	High-level output voltage	V _{IH} = MIN, I _{OH} =		±5%V _{CC}	2.7	3.3		V
V	Law law law at walta as	$V_{CC} = MIN, V_{II} =$	MAX.	±10%V _{CC}		0.35	0.50	V
V _{OL}	Low-level output voltage	$V_{IH} = MIN, I_{OL} = MAX$		±5%V _{CC}		0.35	0.50	V
V _{IK}	Input clamp voltage	$V_{CC} = N$		-0.73	-1.2	V		
I _I	Input current at maximum input voltage	V _{CC} = MA			100	μΑ		
I _{IH}	High-level input current	V _{CC} = MA	$X, V_1 = 2.7$	/			20	μΑ
I _{IL}	Low-level input current	V _{CC} = MA	$X, V_{I} = 0.5$	/			-0.6	mA
l _{OZH}	Off-state output current, High-level voltage applied	V _{CC} = MA	$X, V_0 = 2.7$	V			50	μΑ
I _{OZL}	Off-state output current, Low-level voltage applied	V _{CC} = MA			-50	μΑ		
Ios	Short-circuit output current ³	V _{CC}	-60		-150	mA		
I _{CC}	Supply current (total)	$V_{CC} = MAX$		51	86	mA		

AC ELECTRICAL CHARACTERISTICS

			LIMITS							
SYMBOL	PARAMETER	TEST CONDITIONS		_{amb} = +25°(V _{CC} = +5V 50pF, R _L =		T _{amb} = 0°C V _{CC} = +5 C _L = 50pF,	UNIT			
			MIN	TYP	MAX	MIN	MAX			
f _{MAX}	Maximum Clock frequency	Waveform 1	150	165		135		MHz		
t _{PLH} t _{PHL}	Propagation delay CP to Qn	Waveform 1	3.0 3.0	4.5 4.5	7.0 7.0	2.5 2.5	7.5 7.5	ns		
t _{PZH} t _{PZL}	Output Enable time to High or Low level	Waveform 3 Waveform 4	2.0 2.0	4.5 5.0	7.5 7.5	2.0 2.0	8.5 8.5	ns		
t _{PHZ} t _{PLZ}	Output Disable time from High or Low level	Waveform 3 Waveform 4	2.0 2.0	3.5 3.5	6.5 5.5	2.0 2.0	7.5 6.5	ns		

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	· - · · · · · · · · · · · · · · · · · ·			$T_{amb} = 0^{\circ}C$ $V_{CC} = +5$. $C_{L} = 50pF$,	UNIT		
			MIN	TYP	MAX	MIN	MAX		
t _S (H) t _S (L)	Setup time, Dn to CP	Waveform 2	2.0 2.0			2.5 2.5		ns	
t _h (H) t _h (L)	Hold time, Dn to CP	Waveform 2	0			0		ns	
t _w (H) t _w (L)	CP pulse width, High or Low	Waveform 1	3.0 3.5			3.5 4.0		ns	

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
 Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

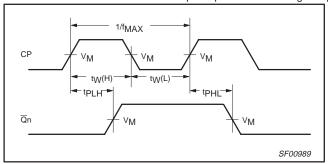
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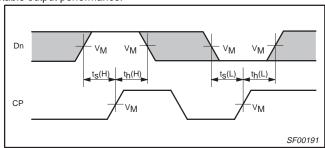
AC WAVEFORMS

For all waveforms, $V_M = 1.5V$

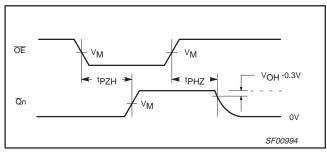
The shaded areas indicate when the input is permitted to change for predictable output performance.



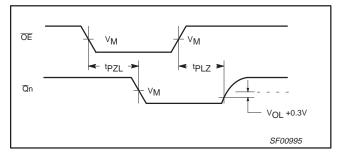
Waveform 1. Propagation Delay, Clock and Enable Inputs to Output, Enable, Clock Pulse Widths, and Maximum Clock Frequency



Waveform 2. Data Setup and Hold Times

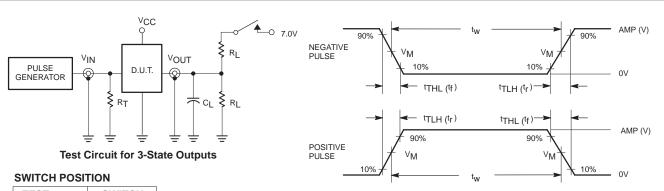


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



TEST	SWITCH
t _{PLZ}	closed
t _{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor;

see AC electrical characteristics for value.

CL = Load capacitance includes jig and probe capacitance;

see AC electrical characteristics for value.

 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INP	UT PU	LSE REQU	REMEN	TS	
family	amplitude	V_{M}	rep. rate	t _w	t _{TLH}	t _{THL}
74F 3.0V		1.5V	1MHz	500ns	2.5ns	2.5ns

Input Pulse Definition

SF00777

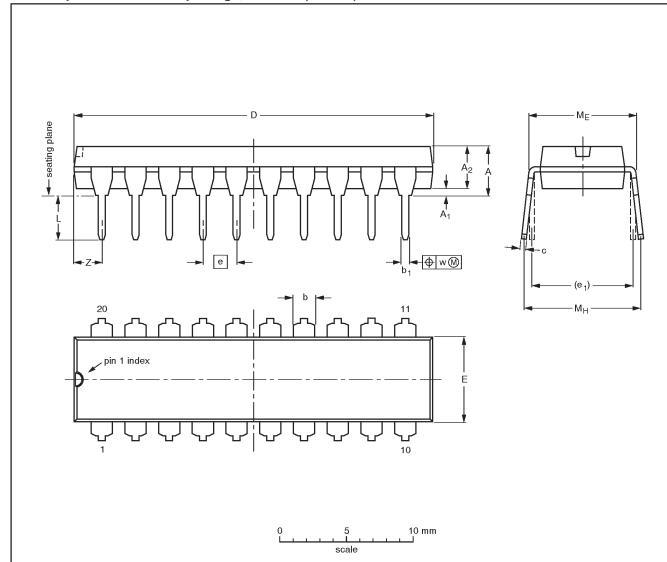
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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	С	D ⁽¹⁾	E ⁽¹⁾	е	e ₁	L	ME	Мн	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

	OUTLINE		REFER	RENCES	EUROPEAN	ISSUE DATE		
	VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE		
	SOT146-1			SC603		92-11-17 95-05-24		

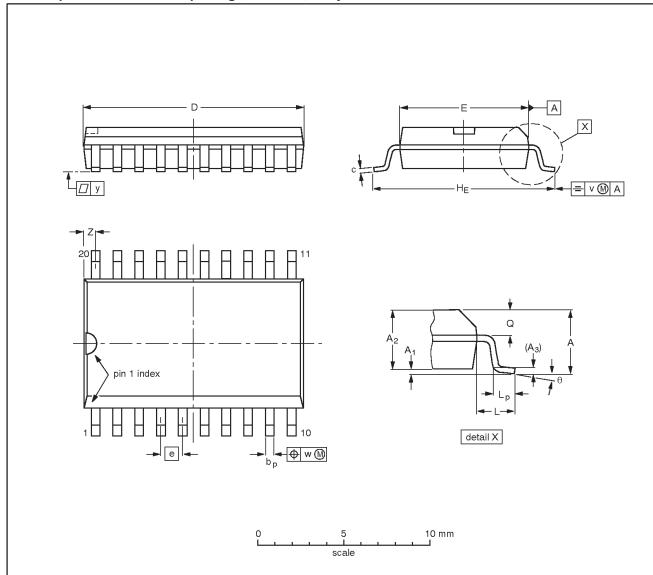
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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	А3	bр	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016		0.01	0.01	0.004	0.035 0.016	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

	OUTLINE		REFER	EUROPEAN ISSUE DATE			
	VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE
	SOT163-1	075E04	MS-013AC				-95-01-24 97-05-22

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NOTES

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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^[1] Please consult the most recently issued datasheet before initiating or completing a design.

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