

DGG OR DL PACKAGE

(TOP VIEW)

1OE

1Q1 🛛 2

1Q2 3

SCES012H-JULY 1995-REVISED SEPTEMBER 2004

56 CLK

55 D1

54 🛛 NC

FEATURES

- Member of the Texas Instruments Widebus™ Family
- EPIC[™] (Enhanced-Performance Implanted CMOS) Submicron Process
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

DESCRIPTION

This 10-bit flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH162820 flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered

while the outputs are in the high-impedance state.

The outputs, which are designed to sink up to 12 mA, include equivalent 26- Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162820 is characterized for operation from -40°C to 85°C.



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	1		-
GND [4	53] GND
2Q1 [5	52] D2
2Q2 [6	51] NC
V _{CC} [7	50] v _{cc}
3Q1 [8	49] D3
3Q2 [9	48] NC
4Q1 [10	47] D4
GND [11	46] GND
4Q2 [12	45] NC
5Q1 [13	44] D5
5Q2 [14	43] NC
6Q1 [15	42] D6
6Q2 [16	41] NC
7Q1 [17	40] D7
GND [18	39] GND
7Q2 [19	38] NC
8Q1 [20	37] D8
8Q2 [21	36] NC
V _{CC} [22	35] v _{cc}
9Q1 [23	34] D9
9Q2 [24	33] NC
GND [25	32] GND
10Q1 [26	31	D10
10Q2 [27	30] NC
2 <mark>0E</mark>	28	29] NC
			I

NC – No internal connection

NOTE: For tape-and-reel order entry, the DGGR package is abbreviated to GR.

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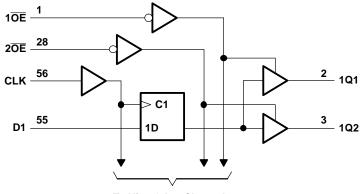


FUNCTION TABLE (each flip-flop)

	INPUTS								
OEn ⁽¹⁾	OEn ⁽¹⁾ CLK D								
L	\uparrow	н	Н						
L	\uparrow	L	L						
L	L	Х	Q ₀						
Н	Х	Х	Z						

(1) n = 1, 2

LOGIC DIAGRAM (POSITIVE LOGIC)



To Nine Other Channels

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	4.6	V
VI	Input voltage range ⁽²⁾	-0.5	4.6	V	
Vo	Output voltage range ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current			±50	mA
	Continuous current through each V_{CC} or	GND		±100	mA
0	Deckage thermal impedance (4)	DGG package		64	0000
θ_{JA}	Package thermal impedance ⁽⁴⁾	DL package		56	°C/W
T _{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) This value is limited to 4.6 V maximum.

(4) The package thermal impedance is calculated in accordance with JESD 51.



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RECOMMENDED OPERATING CONDITIONS⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		1.65	3.6	V
		V _{CC} = 1.65 V to 1.95 V	$0.65 imes V_{CC}$		
V _{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		$V_{CC} = 2.7 V \text{ to } 3.6 V$	2		
		$V_{CC} = 1.65 \text{ V} \text{ to } 1.95 \text{ V}$		$0.35 \times V_{CC}$	
V _{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		$V_{CC} = 2.7 V \text{ to } 3.6 V$		0.8	
VI	Input voltage		0	V _{CC}	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 1.65 V		-2	
	Lieb level evitevit evinent	V _{CC} = 2.3 V		-6	mA
I _{OH}	High-level output current	V _{CC} = 2.7 V		-8	mA
		$V_{CC} = 3 V$		-12	
		V _{CC} = 1.65 V		2	
		V _{CC} = 2.3 V		6	
I _{OL}	Low-level output current	V _{CC} = 2.7 V		8	mA
		$V_{CC} = 3 V$		12	
$\Delta t / \Delta v$	Input transition rise or fall rate	<u> </u>		10	ns/V
T _A	Operating free-air temperature		-40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾ MAX	UNIT
	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} - 0.2		
	I _{OH} = -2 mA	1.65 V	1.2		
	I _{OH} = -4 mA	2.3 V	1.9		
V _{OH}		2.3 V	1.7		V
	I _{OH} = -6 mA	3 V	2.4		
	I _{OH} = -8 mA	2.7 V	2		
	I _{OH} = -12 mA	3 V	2		
	I _{OL} = 100 μA	1.65 V to 3.6 V		0.2	
	I _{OL} = 2 mA	1.65 V		0.45	
	I _{OL} = 4 mA	2.3 V		0.4	
V _{OL}		2.3 V		0.55	V
	I _{OL} = 6 mA	3 V		0.55	
	I _{OL} = 8 mA	2.7 V		0.6	
	I _{OL} = 12 mA	3 V		0.8	
I _I	$V_{I} = V_{CC} \text{ or } GND$	3.6 V		±5	μA
	V _I = 0.58 V	1.65 V	25		
	V _I = 1.07 V	1.65 V	-25		
	V ₁ = 0.7 V	2.3 V	45		
I _{I(hold)}	V _I = 1.7 V	2.3 V	-45		μA
	V _I = 0.8 V	3 V	75		
	V ₁ = 2 V	3 V	-75		
	$V_1 = 0$ to 3.6 V ⁽²⁾	3.6 V		±500	
I _{OZ}	$V_{O} = V_{CC}$ or GND	3.6 V		±10	μA
I _{CC}	$V_{I} = V_{CC} \text{ or } GND$ $I_{O} = 0$	3.6 V		40	μΑ
ΔI _{CC}	One input at V_{CC} - 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V		750	μΑ
C Control inputs	V = V or CND	3.3 V		3.5	۳Ē
C _i Data inputs	$\frac{V_{I}}{V_{I}} = V_{CC} \text{ or GND}$			6	pF
C _o Outputs	$V_{O} = V_{CC}$ or GND	3.3 V		7	pF

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(1) All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. (2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

		V _{CC} =	1.8 V	V _{CC} = 2 ± 0.2	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} = 3 ± 0.3	3.3 V 3 V	UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		(1)		150		150		150	MHz
tw	Pulse duration, CLK high or low	(1)		3.3		3.3		3.3		ns
t _{su}	Setup time, data before CLK [↑]	(1)		1.7		1.8		1.4		ns
t _h	Hold time, data after CLK↑	(1)		1.1		1.1		1		ns

(1) This information was not available at the time of publication.



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SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

PARAMETER		TO	V _{CC} = 1.8 V		V_{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
	(INPUT)	(OUTPUT)	MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			(1)		150		150		150		MHz
t _{pd}	CLK	Q		(1)	1	6.4		6.2	1	5.4	ns
t _{en}	OE	Q		(1)	1	6.9		6.8	1	5.6	ns
t _{dis}	OE	Q		(1)	1	6.2		5.5	1	5	ns

(1) This information was not available at the time of publication.

OPERATING CHARACTERISTICS

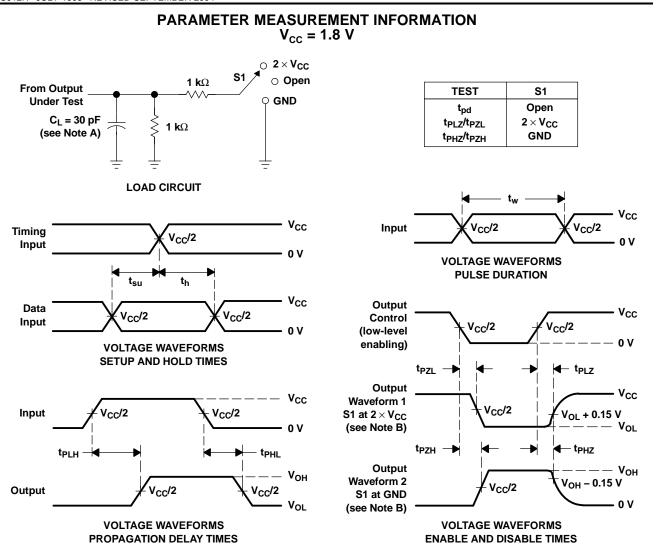
 $T_A = 25^{\circ}C$

	PARAME	ETER	TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT
	Power dissipation	All outputs enabled		(1)	68	66	_
C _{pd}	capacitance per flip-flop	All outputs disabled	$C_{L} = 50 \text{ pF}, \text{ f} = 10 \text{ MHz}$	(1)	39	47	pF

(1) This information was not available at the time of publication.







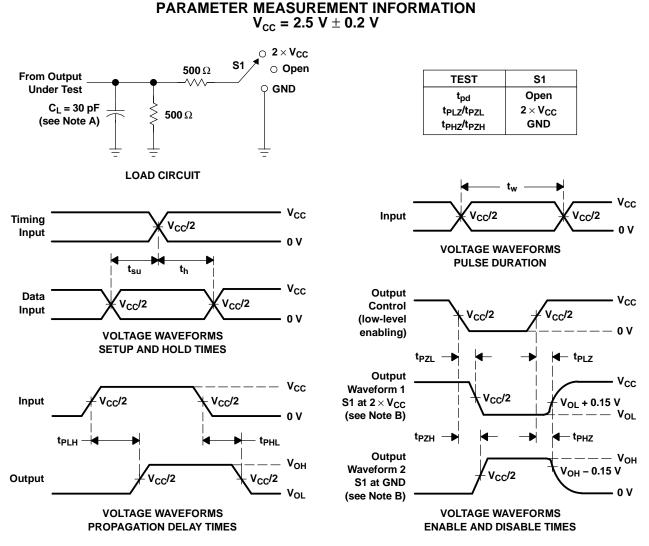
- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_f \leq 2 ns, t_f \leq 2 ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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SN74ALVCH162820 3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS

SCES012H-JULY 1995-REVISED SEPTEMBER 2004

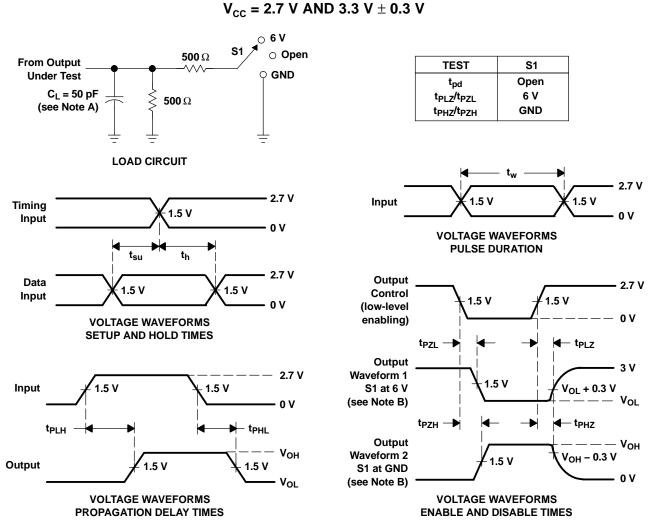


- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_r \leq 2 ns, t_f \leq 2 ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms



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PARAMETER MEASUREMENT INFORMATION

NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_r \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 3. Load Circuit and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
74ALVCH162820DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
74ALVCH162820DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN74ALVCH162820DGGR	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI	
SN74ALVCH162820DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
SN74ALVCH162820DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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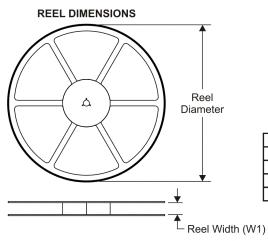
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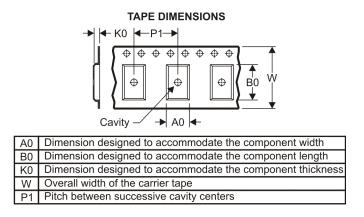
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH162820DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

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PACKAGE MATERIALS INFORMATION

23-Jul-2010



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH162820DLR	SSOP	DL	56	1000	346.0	346.0	49.0

MECHANICAL DATA

MSSO001C - JANUARY 1995 - REVISED DECEMBER 2001

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

DL (R-PDSO-G**)



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118



MECHANICAL DATA

MTSS003D - JANUARY 1995 - REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



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