#### **INTEGRATED CIRCUITS**

## DATA SHEET

# **74LVCH32374A**32-bit edge-triggered D-type flip-flop with 5 V tolerant inputs/outputs; 3-state

Product specification Supersedes data of 1999 Nov 24 2004 May 24





### 32-bit edge-triggered D-type flip-flop with 5 V tolerant inputs/outputs; 3-state

#### 74LVCH32374A

#### **FEATURES**

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- MULTIBYTE flow-trough standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- · Direct interface with TTL levels
- · All data inputs have bushold
- Complies with JEDEC standard JESD8-B/JESD36
- · ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from -40 °C to +85 °C
- Packaged in plastic fine-pitch ball grid array package.

#### **DESCRIPTION**

The 74LVCH32374A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most

advanced CMOS compatible TTL families.

The inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, the outputs can handle 5 V. These features allow the use of these devices in a mixed 3.3 V or 5 V environment.

The 74LVCH32374A is a 32-bit edge-triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. The 74LVCH32374A consists of 4 sections of 8 edge-triggered flip-flops. A clock (pin nCP) input and an output enable input (pin  $n\overline{OE}$ ) are provided per 8-bit section.

The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH nCP transition.

When pin  $n\overline{OE}$  is LOW, the contents of the flip-flops are available at the outputs. When pin  $n\overline{OE}$  is HIGH, the outputs go to the high-impedance OFF-state. Operation of pin  $n\overline{OE}$  does not affect the state of the flip-flops.

The 74LVCH32374A bushold data input circuits eliminate the need for external pull-up resistors to hold unused inputs.

#### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25 \, ^{\circ}\text{C}$ ;  $t_r = t_f \le 2.5 \, \text{ns}$ 

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nCP to nQn	C <sub>L</sub> = 50 pF; V <sub>CC</sub> = 3.3 V	3.4	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time nOE to nQn	$C_L = 50 \text{ pF}; V_{CC} = 3.3 \text{ V}$	3.5	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time nOE to nQn	$C_L = 50 \text{ pF}; V_{CC} = 3.3 \text{ V}$	3.9	ns
f <sub>max</sub>	maximum clock frequency	$C_L = 50 \text{ pF}; V_{CC} = 3.3 \text{ V}$	150	MHz
Cı	input capacitance		5.0	pF
C <sub>PD</sub>	power dissipation per flip-flop	V <sub>CC</sub> = 3.3 V; notes 1 and 2		
		outputs enabled	19	pF
		outputs disabled	12	pF

#### **Notes**

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:

 $f_i$  = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in Volts;

N = total load switching outputs;

 $\Sigma(C_L \times V_{CC}^2 \times f_0)$  = sum of the outputs.

2. The condition is  $V_I = GND$  to  $V_{CC}$ .

## 32-bit edge-triggered D-type flip-flop with 5 V tolerant inputs/outputs; 3-state

#### 74LVCH32374A

#### **ORDERING INFORMATION**

TYPE NUMBER	PACKAGE						
I TPE NUMBER	TEMPERATURE RANGE	BALLS	PACKAGE	MATERIAL	CODE		
74LVCH32374AEC	−40 °C to +85 °C	96	LFBGA96	plastic	SOT536-1		

#### **FUNCTION TABLE**

See note 1.

OPERATING MODE		INPUT	INTERNAL	OUTPUT	
OPERATING MODE	nŌĒ	nCP	nDn	FLIP-FLOP	nQn
Load and read register	L	1	I	L	L
	L	1	h	Н	Н
Load register and disable	Н	1	I	L	Z
outputs	Н	1	h	Н	Z

#### Note

1. H = HIGH voltage level;

h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition;

L = LOW voltage level;

I = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition;

Z = high-impedance OFF-state;

 $\uparrow$  = LOW-to-HIGH CP transition.

#### **PINNING**

BALL	SYMBOL	DESCRIPTION
A1	1Q1	flip-flop output
A2	1Q0	flip-flop output
А3	1 <del>OE</del>	output enable input (active LOW)
A4	1CP	clock input
A5	1D0	data input
A6	1D1	data input
B1	1Q3	flip-flop output
B2	1Q2	flip-flop output
В3	GND	ground (0 V)
B4	GND	ground (0 V)
B5	1D2	data input
B6	1D3	data input
C1	1Q5	flip-flop output
C2	1Q4	flip-flop output
C3	V <sub>CC</sub>	supply voltage
C4	V <sub>CC</sub>	supply voltage
C5	1D4	data input

BALL	SYMBOL	DESCRIPTION
C6	1D5	data input
D1	1Q7	flip-flop output
D2	1Q6	flip-flop output
D3	GND	ground (0 V)
D4	GND	ground (0 V)
D5	1D6	data input
D6	1D7	data input
E1	2Q1	flip-flop output
E2	2Q0	flip-flop output
E3	GND	ground (0 V)
E4	GND	ground (0 V)
E5	2D0	data input
E6	2D1	data input
F1	2Q3	flip-flop output
F2	2Q2	flip-flop output
F3	V <sub>CC</sub>	supply voltage
F4	V <sub>CC</sub>	supply voltage
F5	2D2	data input

# 32-bit edge-triggered D-type flip-flop with 5 V tolerant inputs/outputs; 3-state

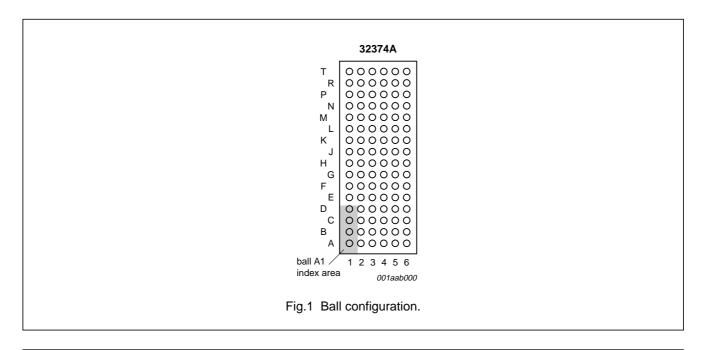
### 74LVCH32374A

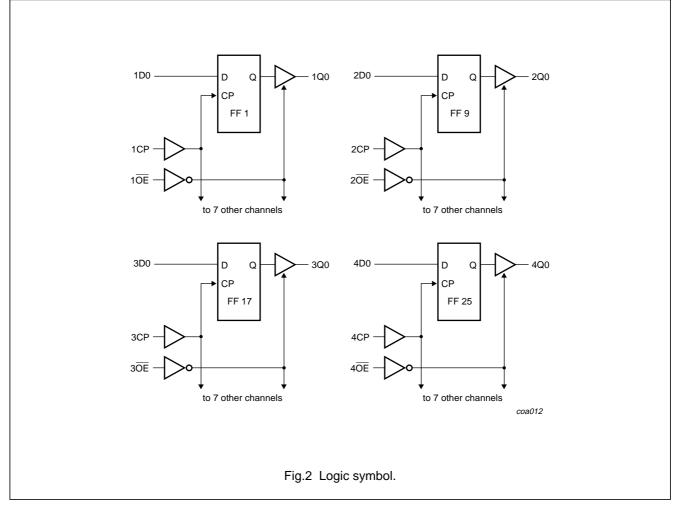
BALL	SYMBOL	DESCRIPTION
F6	2D3	data input
G1	2Q5	flip-flop output
G2	2Q4	flip-flop output
G3	GND	ground (0 V)
G4	GND	ground (0 V)
G5	2D4	data input
G6	2D5	data input
H1	2Q6	flip-flop output
H2	2Q7	flip-flop output
H3	2 <del>OE</del>	output enable input (active LOW)
H4	2CP	clock input
H5	2D7	data input
H6	2D6	data input
J1	3Q1	flip-flop output
J2	3Q0	flip-flop output
J3	3 <del>OE</del>	output enable input (active LOW)
J4	3CP	clock input
J5	3D0	data input
J6	3D1	data input
K1	3Q3	flip-flop output
K2	3Q2	flip-flop output
K3	GND	ground (0 V)
K4	GND	ground (0 V)
K5	3D2	data input
K6	3D3	data input
L1	3Q5	flip-flop output
L2	3Q4	flip-flop output
L3	V <sub>CC</sub>	supply voltage
L4	V <sub>CC</sub>	supply voltage
L5	3D4	data input
L6	3D5	data input

BALL	SYMBOL	DESCRIPTION
M1	3Q7	flip-flop output
M2	3Q6	flip-flop output
М3	GND	ground (0 V)
M4	GND	ground (0 V)
M5	3D6	data input
M6	3D7	data input
N1	4Q1	flip-flop output
N2	4Q0	flip-flop output
N3	GND	ground (0 V)
N4	GND	ground (0 V)
N5	4D0	data input
N6	4D1	data input
P1	4Q3	flip-flop output
P2	4Q2	flip-flop output
P3	V <sub>CC</sub>	supply voltage
P4	V <sub>CC</sub>	supply voltage
P5	4D2	data input
P6	4D3	data input
R1	4Q5	flip-flop output
R2	4Q4	flip-flop output
R3	GND	ground (0 V)
R4	GND	ground (0 V)
R5	4D4	data input
R6	4D5	data input
T1	4Q6	data input
T2	4Q7	clock input
T3	4 <del>OE</del>	output enable input (active LOW)
T4	4CP	clock input
T5	4D7	data input
T6	4D6	data input

### 32-bit edge-triggered D-type flip-flop with 5 V tolerant inputs/outputs; 3-state

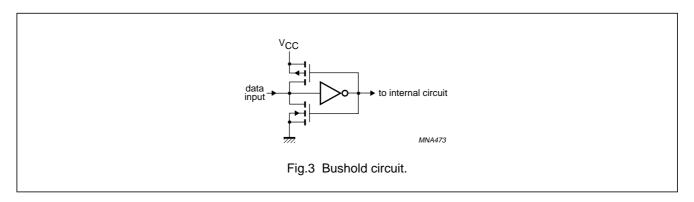
#### 74LVCH32374A





### 32-bit edge-triggered D-type flip-flop with 5 V tolerant inputs/outputs; 3-state

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#### RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage	for maximum speed performance	2.7	3.6	V
		for low voltage applications	1.2	3.6	V
VI	input voltage		0	5.5	V
Vo	output voltage	output HIGH or LOW state	0	V <sub>CC</sub>	V
		output 3-state	0	5.5	V
T <sub>amb</sub>	ambient temperature	in free air	-40	+85	°C
t <sub>r</sub> , t <sub>f</sub>	input rise and fall times	V <sub>CC</sub> = 1.2 V to 2.7 V	0	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	10	ns/V

#### **LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
I <sub>IK</sub>	input diode current	V <sub>I</sub> < 0 V	_	-50	mA
VI	input voltage	note 2	-0.5	+6.5	V
I <sub>OK</sub>	output diode current	$V_O > V_{CC}$ or $V_O < 0$ V	_	±50	mA
Vo	output voltage	output HIGH or LOW state; note 2	-0.5	V <sub>CC</sub> + 0.5	V
		output 3-state; note 2	-0.5	+6.5	٧
Io	output source or sink current	$V_O = 0 \text{ V to } V_{CC}$	_	±50	mA
I <sub>CC</sub> , I <sub>GND</sub>	V <sub>CC</sub> or GND current	note 1	_	±200	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	power dissipation	$T_{amb} = -40  ^{\circ}\text{C} \text{ to } +85  ^{\circ}\text{C}; \text{ note } 3$	_	1000	mW

#### **Notes**

- 1. All supply and ground pins connected externally to one voltage source.
- 2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- 3. Above 70 °C the value of Ptot derates linearly with 1.8 mW/K.

### 32-bit edge-triggered D-type flip-flop with 5 V tolerant inputs/outputs; 3-state

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#### **DC CHARACTERISTICS**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

CVMDO	DADAMETED	TEST CONDIT	IONS	RAINI	TVD	BAAY		
SYMBOL	PARAMETER	OTHER	V <sub>CC</sub> (V)	MIN.	TYP.	MAX.	UNIT	
T <sub>amb</sub> = -40	) °C to +85 °C; note 1			•	•	1		
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	_	_	V	
			2.7 to 3.6	2.0	_	_	V	
V <sub>IL</sub>	LOW-level input voltage		1.2	_	_	GND	V	
			2.7 to 3.6	_	_	0.8	V	
V <sub>OH</sub>	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$						
		$I_{O} = -100  \mu A$	2.7 to 3.6	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	_	V	
		$I_{O} = -12 \text{ mA}$	2.7	V <sub>CC</sub> - 0.5	_	_	V	
		$I_{O} = -18 \text{ mA}$	3.0	V <sub>CC</sub> – 0.6	_	_	V	
		$I_{O} = -24 \text{ mA}$	3.0	V <sub>CC</sub> – 0.8	_	_	V	
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$						
		I <sub>O</sub> = 100 μA	2.7 to 3.6	_	GND	0.20	V	
		I <sub>O</sub> = 12 mA	2.7	_	_	0.40	V	
		I <sub>O</sub> = 24 mA	3.0	_	_	0.55	V	
I <sub>LI</sub>	input leakage current	$V_I = 5.5 \text{ V or GND};$ note 2	3.6	_	±0.1	±5	μΑ	
l <sub>OZ</sub>	3-state output OFF-state current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = 5.5$ V or GND; note 2	3.6	_	±0.1	±5	μΑ	
I <sub>off</sub>	power-off leakage supply current	$V_I$ or $V_O = 5.5 \text{ V}$	0.0	_	±0.1	±10	μΑ	
I <sub>CC</sub>	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A	3.6	_	0.1	40	μА	
$\Delta I_{CC}$	additional quiescent supply current per input pin	$V_I = V_{CC} - 0.6 \text{ V};$ $I_O = 0 \text{ A}$	2.7 to 3.6	_	5	500	μΑ	
I <sub>BHL</sub>	bushold LOW sustaining current	V <sub>I</sub> = 0.8 V; notes 3 and 4	3.0	75	_	-	μΑ	
Івнн	bushold HIGH sustaining current	V <sub>I</sub> = 2.0 V; notes 3 and 4	3.0	-75	_	-	μΑ	
I <sub>BHLO</sub>	bushold LOW overdrive current	notes 3 and 5	3.6	500	_	_	μΑ	
Івнно	bushold HIGH overdrive current	notes 3 and 5	3.6	-500	_	_	μΑ	

#### **Notes**

- 1. All typical values are measured at  $T_{amb}$  = 25 °C.
- 2. For bushold parts, the bushold circuit is switched off when  $V_I > V_{CC}$  allowing 5.5 V on the input pin.
- 3. For data inputs only, control inputs do not have a bushold circuit.
- 4. The specified sustaining current at the data inputs holds the input below the specified V<sub>I</sub> level.
- 5. The specified overdrive current at the data input forces the data input to the opposite logic input state.

# 32-bit edge-triggered D-type flip-flop with 5 V tolerant inputs/outputs; 3-state

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#### **AC CHARACTERISTICS**

GND = 0 V;  $t_r$  =  $t_f \leq$  2.5 ns;  $C_L$  = 50 pF;  $R_L$  = 500  $\Omega.$ 

CVMDOL	PARAMETER	CONDITIONS		BAIL.	TVD	BAAY	
SYMBOL		WAVEFORMS	V <sub>CC</sub> (V)	MIN.	TYP.	MAX.	UNIT
T <sub>amb</sub> = -40	) °C to +85 °C; note1		-	<u> </u>			1
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay	see Figs. 4 and 7	1.2	_	14	_	ns
	nCP to nQn		2.7	1.5	_	6.0	ns
		3.0 to 3.6	1.5	3.4(2)	5.4	ns	
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time nOE to nQn	see Figs. 6 and 7	1.2	_	20	_	ns
			2.7	1.5	_	6.0	ns
			3.0 to 3.6	1.0	3.5(2)	5.2	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	t <sub>PHZ</sub> /t <sub>PLZ</sub> 3-state output disable time	see Figs. 6 and 7	1.2	_	12	_	ns
nOE to nQn	nOE to nQn		2.7	1.5	_	5.1	ns
			3.0 to 3.6	1.5	3.9(2)	4.9	ns
t <sub>W</sub>	nCP pulse width HIGH	HIGH see Fig.4	1.2	_	_	_	ns
			2.7	3.0	_	_	ns
			3.0 to 3.6	3.0	1.5 <sup>(2)</sup>	_	ns
t <sub>su</sub>	set-up time nDn to nCP	see Fig.5	1.2	_	_	_	ns
			2.7	1.9	_	_	ns
			3.0 to 3.6	1.9	0.3(2)	_	ns
t <sub>h</sub>	hold time nDn to nCP	see Fig.5	1.2	_	_	_	ns
			2.7	1.1	_	_	ns
			3.0 to 3.6	1.5	-0.3(2)	_	ns
t <sub>sk(0)</sub>	skew		3.0 to 3.6	_	_	1.0	ns
f <sub>max</sub>	maximum clock pulse	see Fig.4	2.7	80	_	_	MHz
	frequency		3.0 to 3.6	100	150 <sup>(2)</sup>	_	MHz

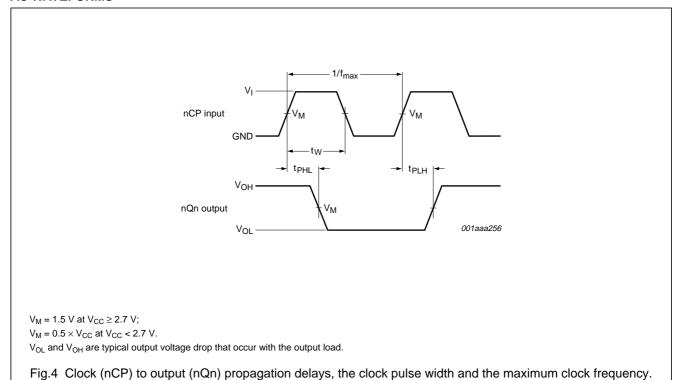
#### Notes

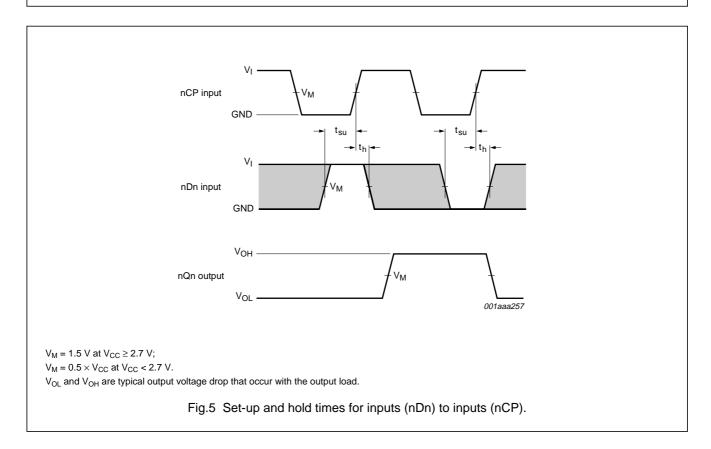
- 1. All typical values are measured at  $T_{amb}$  = 25 °C.
- 2. These typical values are measured at  $V_{CC}$  = 3.3 V.

### 32-bit edge-triggered D-type flip-flop with 5 V tolerant inputs/outputs; 3-state

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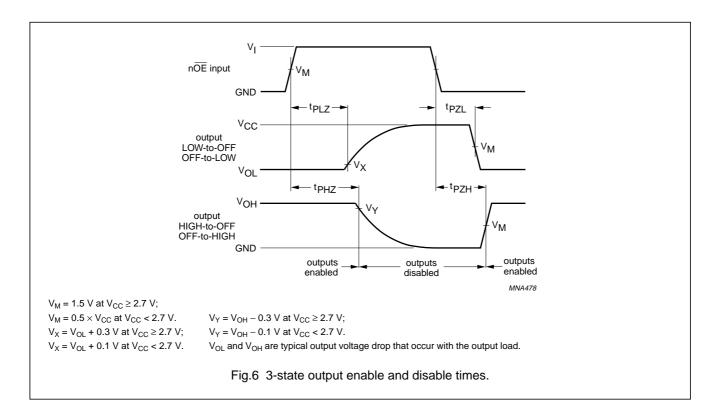
#### **AC WAVEFORMS**

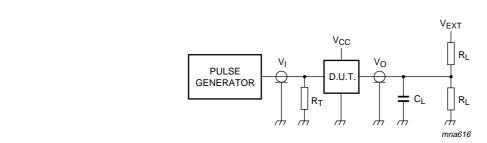




### 32-bit edge-triggered D-type flip-flop with 5 V tolerant inputs/outputs; 3-state

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V <sub>z</sub> -	V.	C	D.	V <sub>EXT</sub>			
V <sub>CC</sub>	V <sub>I</sub>	CL	R <sub>L</sub>	t <sub>PLH</sub> /t <sub>PHL</sub>	t <sub>PZH</sub> /t <sub>PHZ</sub>	t <sub>PZL</sub> /t <sub>PLZ</sub>	
1.2 V	V <sub>CC</sub>	50 pF	$500~\Omega^{(1)}$	open	GND	$2 \times V_{CC}$	
2.7 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$	
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$	

#### Note

1. The circuit performs better when RL =  $1000 \Omega$ .

Definitions for test circuit:

R<sub>L</sub> = Load resistor.

 $C_L$  = Load capacitance including jig and probe capacitance.

 $R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

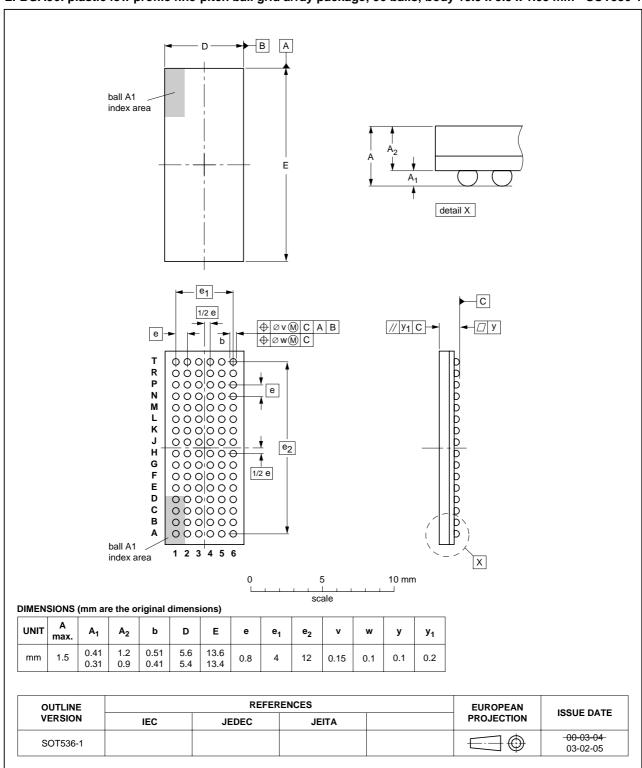
Fig.7 Load circuitry for switching times.

### 32-bit edge-triggered D-type flip-flop with 5 V tolerant inputs/outputs; 3-state

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#### **PACKAGE OUTLINE**

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1



### 32-bit edge-triggered D-type flip-flop with 5 V tolerant inputs/outputs; 3-state

#### 74LVCH32374A

#### **DATA SHEET STATUS**

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

#### **Notes**

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- 2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
- 3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

#### **DEFINITIONS**

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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