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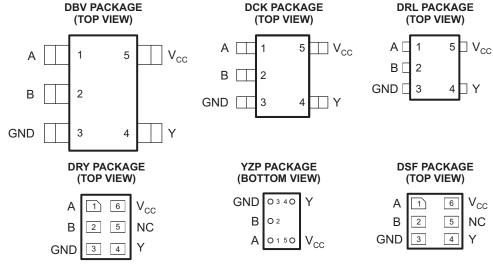
SINGLE 2-INPUT POSITIVE NOR-GATE

Check for Samples: SN74LVC1G02

FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 3.6 ns at 3.3 V
- Low Power Consumption, 10-µA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- Ioff Supports Partial-Power-Down Mode
 Operation

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



NC – No internal connection

See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This single 2-input positive-NOR gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G02 performs the Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

NanoFree[™] package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74LVC1G02

SCES213S - APRIL 1999 - REVISED MARCH 2011

ORDERING INFORMATION

	ORDERING INFORMATION										
T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽²⁾							
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74LVC1G02YZPR	CB_							
	SON – DSF	Reel of 5000	SN74LVC1G02DSFR	СВ							
	SON – DRY	Reel of 5000	SN74LVC1G02DRYR	СВ							
–40°C to 85°C		Reel of 3000	SN74LVC1G02DBVR	C02							
	SOT (SOT-23) – DBV	Reel of 250	SN74LVC1G02DBVT	- C02_							
		Reel of 3000	SN74LVC1G02DCKR	CP							
	SOT (SC-70) – DCK	Reel of 250	SN74LVC1G02DCKT	- CB_							
	SOT (SOT-553) – DRL	Reel of 4000	SN74LVC1G02DRLR	CB_							

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) DBV/DCK/DRL: The actual top-side marking has one additional character that designates the assembly/test site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE								
INP	OUTPUT							
Α	В	Y						
Н	Х	L						
Х	Н	L						
L	L	Н						

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	6.5	V
VI	Input voltage range		-0.5	6.5	V
Vo	Voltage range applied to any output in the hi	-0.5	6.5	V	
Vo	Voltage range applied to any output in the hi	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current		±50	mA	
	Continuous current through V_{CC} or GND			±100	mA
		DBV package		206	
0	Declarse thermolizer edge as (4)	DCK package		252	°C/W
θ_{JA}	Package thermal impedance ⁽⁴⁾	DRL package		142	C/W
		YZP package		132	
T _{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the recommended operating conditions table.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

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Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V	Supply voltage	Operating	1.65	5.5	V
V _{CC}	Supply voltage	Data retention only	1.5		V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
V	Ligh lovel input veltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
V _{IH}	High-level input voltage	V_{CC} = 3 V to 3.6 V	2		V
		V_{CC} = 4.5 V to 5.5 V	$0.7 \times V_{CC}$		
		V_{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
V		V_{CC} = 2.3 V to 2.7 V		0.7	V
V _{IL}	Low-level input voltage	V_{CC} = 3 V to 3.6 V		0.8	V
		V_{CC} = 4.5 V to 5.5 V		$0.3 \times V_{CC}$	
VI	Input voltage		0	5.5	V
Vo	Output voltage		0	V _{CC}	V
		V _{CC} = 1.65 V		-4	
		$V_{CC} = 2.3 V$		-8	
I _{OH}	High-level output current	$V_{CC} = 3 V$		–16	mA
		V _{CC} = 5 V		-24	
		$V_{CC} = 4.5 V$		-32	
		V _{CC} = 1.65 V		4	
		$V_{CC} = 2.3 V$		8	
I _{OL}	Low-level output current	$V_{CC} = 3 V$		16	mA
		V _{CC} = 3 V		24	
		$V_{CC} = 4.5 V$		32	
		V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	
Δt/Δv	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V
		$V_{CC} = 5 V \pm 0.5 V$		5	
T _A	Operating free-air temperature		-40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER	TEST CONDITIONS		V _{cc}	MIN	TYP ⁽¹⁾	MAX	UNIT		
		I _{OH} = -100 μA		1.65 V to 5.5 V	$V_{CC} - 0.1$					
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2					
		$I_{OH} = -8 \text{ mA}$		2.3 V	1.9			V		
V _{OH}		I _{OH} = -16 mA		3 V	2.4			V		
		I _{OH} = -24 mA		3 V	2.3					
I _{OH} = -32 mA				4.5 V	3.8					
		I _{OL} = 100 μA		1.65 V to 5.5 V			0.1			
		I _{OL} = 4 mA		1.65 V			0.45			
V		I _{OL} = 8 mA		2.3 V			0.3	V		
V _{OL}		I _{OL} = 16 mA		3 V		0.4				
		I _{OL} = 24 mA		3 V	0.55					
		I _{OL} = 32 mA		4.5 V			0.55			
I _I	A or B inputs	V _I = 5.5 V or GND		0 to 5.5 V	±5			μA		
I _{off}		$V_1 \text{ or } V_0 = 5.5 \text{ V}$		0			±10	μA		
I _{CC}		$V_{I} = 5.5 \text{ V or GND}$ $I_{O} = 0$		1.65 V to 5.5 V			10	μA		
ΔI _{CC}		One input at $V_{CC} = 0.6 V$, Other inputs	s at V _{CC} or GND	3 V to 5.5 V			500	μA		
Ci		$V_1 = V_{CC}$ or GND		3.3 V		4		pF		

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	PARAMETER FROM (INPUT)		V _{CC} = 1.8 V ± 0.15 V		$V_{CC} = 2.5 V \\ \pm 0.2 V$		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	1.9	7.2	0.8	4.4	0.8	3.6	0.8	3.4	ns

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ or 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	1.8 V 15 V	$V_{CC} = 2.5 V \pm 0.2 V$		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT	
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	2.8	8	1.2	5.5	1	4.5	1	4	ns

Operating Characteristics

 $T_A = 25^{\circ}C$

	PARAMETER	TEST	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	$V_{CC} = 5 V$	UNIT	
		CONDITIONS	TYP	TYP	TYP	TYP		
C_{pd}	Power dissipation capacitance	f = 10 MHz	23	23	23	25	pF	

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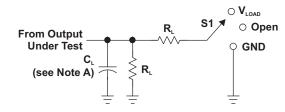


SN74LVC1G02

SCES213S - APRIL 1999-REVISED MARCH 2011

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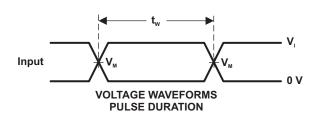
PARAMETER MEASUREMENT INFORMATION

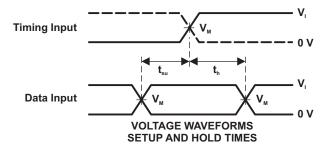


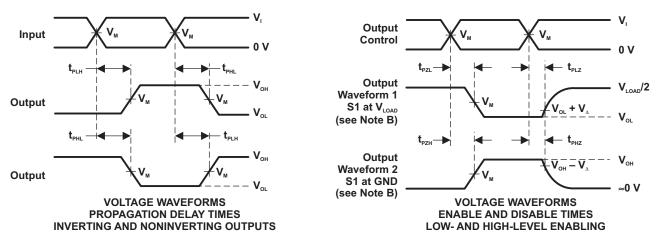
LOAD CIRCUIT

TEST	S1
$t_{_{PLH}}/t_{_{PHL}}$	Open
t_{PLZ}/t_{PZL}	VLOAD
t _{PHZ} /t _{PZH}	GND

	INPUTS		N	N	•	-		
V _{cc}	V	t,/t,	V _M	VLOAD	CL	R	V	
1.8 V ± 0.15 V	V _{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	15 pF	1 Μ Ω	0.15 V	
$2.5~V\pm0.2~V$	V_{cc}	≤2 ns	V _{cc} /2	2 × V _{cc}	15 pF	1 Μ Ω	0.15 V	
$3.3 V \pm 0.3 V$	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 Μ Ω	0.3 V	
$5 V \pm 0.5 V$	V_{cc}	≤2.5 ns	V _{cc} /2	2 × V _{cc}	15 pF	1 Μ Ω	0.3 V	







NOTES: A. C₁ includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z₀ = 50 Ω .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. $t_{\mbox{\tiny PLZ}}$ and $t_{\mbox{\tiny PHZ}}$ are the same as $t_{\mbox{\tiny dis}}.$
- F. $t_{_{\text{PZL}}}$ and $t_{_{\text{PZH}}}$ are the same as $t_{_{\text{en}}}.$
- G. t_{PLH} and t_{PHL} are the same as t_{od} .
- H. All parameters and waveforms are not applicable to all devices.

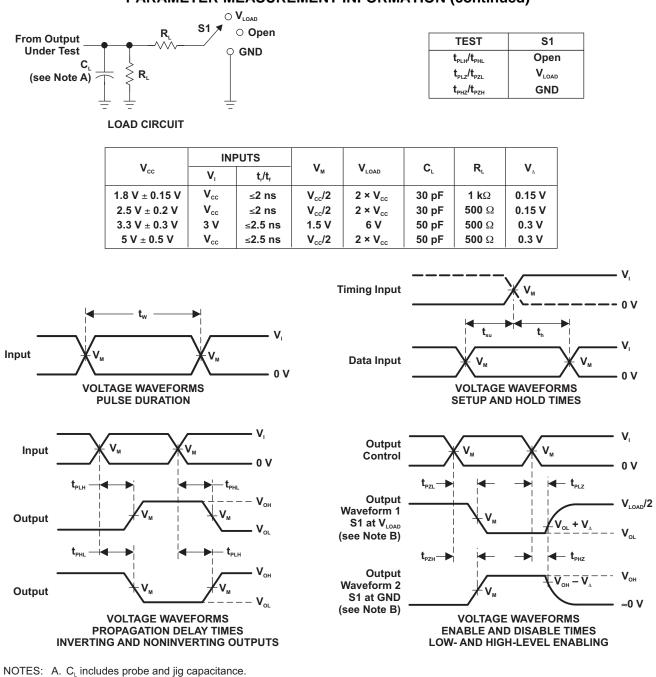
Figure 1. Load Circuits and Voltage Waveforms

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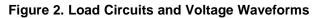
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- - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_o = 50 Ω .
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. $t_{\mbox{\tiny PZL}}$ and $t_{\mbox{\tiny PZH}}$ are the same as $t_{\mbox{\tiny en}}^{\mbox{\tiny OC}}$
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.





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1-Jun-2012

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LVC1G02DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G02DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G02DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G02DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G02DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G02DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G02DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G02DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G02DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G02DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G02DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G02DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G02DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G02DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G02DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G02DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G02YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	



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(1) The marketing status values are defined as follows:
 ACTIVE: Product device recommended for new designs.
 LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
 NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
 PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
 OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G02 :

Enhanced Product: SN74LVC1G02-EP

NOTE: Qualified Version Definitions:

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

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Pin1 Quadrant

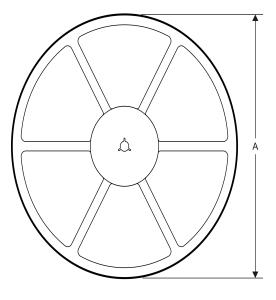
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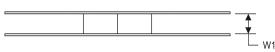
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

Texas Instruments





TAPE AND REEL INFORMATION

SN74LVC1G02DSFR

SN74LVC1G02YZPR

SON

DSBGA

DSF

YZP

6

5

TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal											
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
SN74LVC1G02DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0
SN74LVC1G02DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.2	1.55	4.0	8.0
SN74LVC1G02DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0
SN74LVC1G02DBVT	SOT-23	DBV	5	250	178.0	9.2	3.3	3.2	1.55	4.0	8.0
SN74LVC1G02DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0
SN74LVC1G02DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0
SN74LVC1G02DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0
SN74LVC1G02DCKT	SC70	DCK	5	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0
SN74LVC1G02DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0
SN74LVC1G02DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0
SN74LVC1G02DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0
SN74LVC1G02DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0

5000

3000

180.0

180.0

9.5

8.4

1.16

1.02

1.16

1.52

0.5

0.63

4.0

4.0

8.0

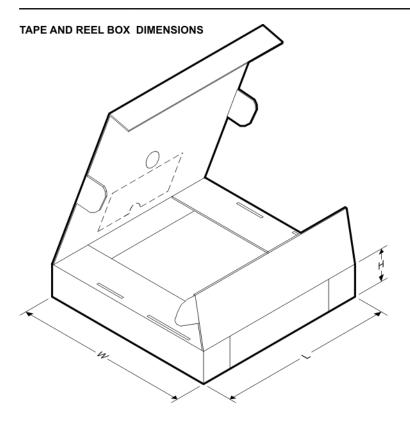
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PACKAGE MATERIALS INFORMATION

14-Mar-2012



All dimensions are nominal	-				-		
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G02DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G02DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G02DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G02DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G02DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G02DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74LVC1G02DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G02DCKT	SC70	DCK	5	250	205.0	200.0	33.0
SN74LVC1G02DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G02DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G02DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G02DRYR	SON	DRY	6	5000	180.0	180.0	30.0
SN74LVC1G02DSFR	SON	DSF	6	5000	180.0	180.0	30.0
SN74LVC1G02YZPR	DSBGA	YZP	5	3000	220.0	220.0	34.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

D. Falls within JEDEC MO-178 Variation AA.



DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters.B. This drawing is subject to change without notice.

- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.



LAND PATTERN DATA



NOTES:

- A. All linear dimensions are in millimeters.B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE



NOTES:

All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994. Α. B. This drawing is subject to change without notice.

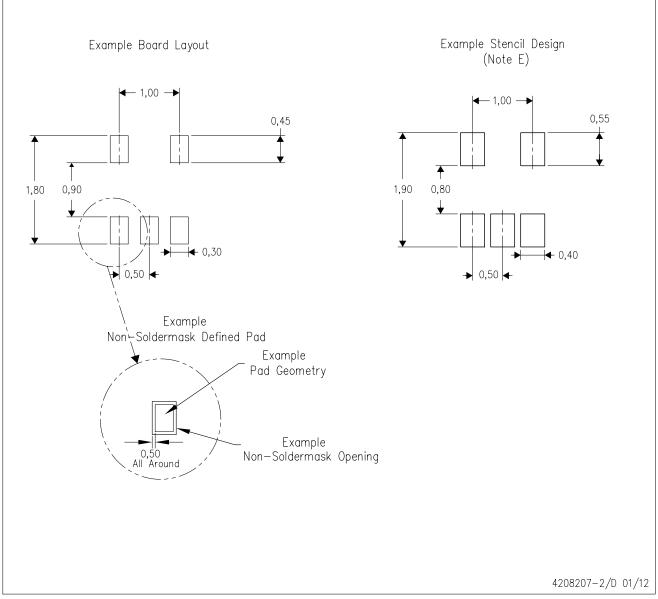
🖄 Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.





DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE

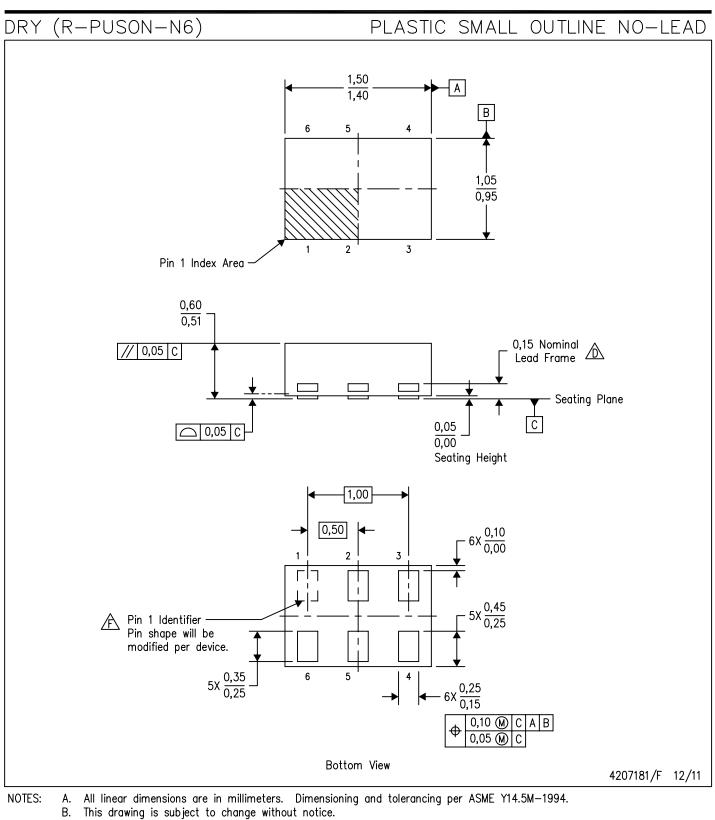


NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



MECHANICAL DATA

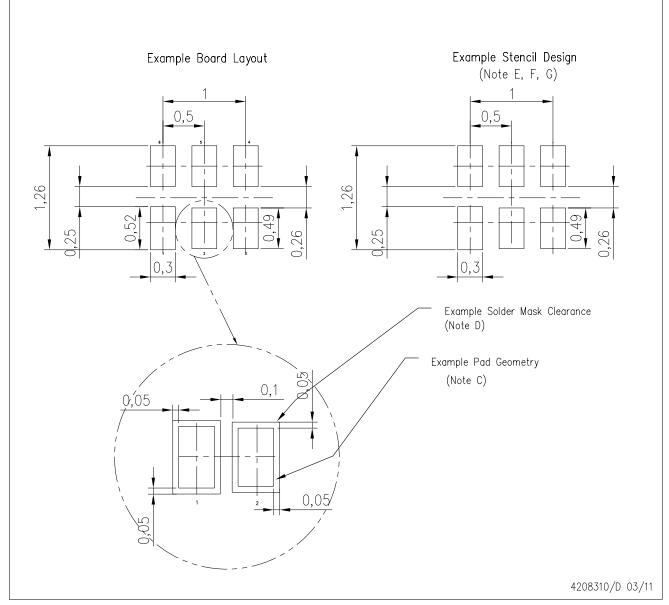


- C. SON (Small Outline No-Lead) package configuration.
- Δ The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
- E. This package complies to JEDEC MO-287 variation UFAD.
- 🖄 See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.



DRY (S-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



MECHANICAL DATA



- - B. This drawing is subject to change without notice.
 C. SON (Small Outline No-Lead) package configuration.
 D. This package complies to JEDEC M0-287 variation X2AAF.





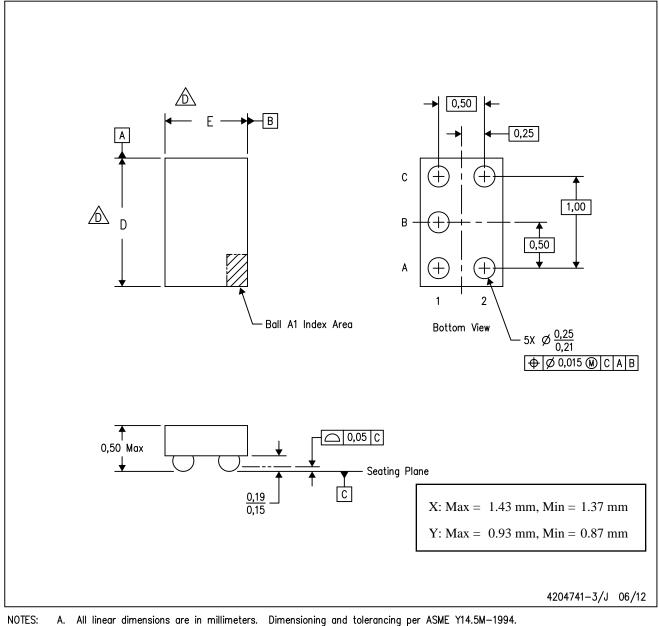
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
- E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
- H. Component placement force should be minimized to prevent excessive paste block deformation.



YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



- Α. Β. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative. E. This package is a Pb-free solder ball design. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.



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