

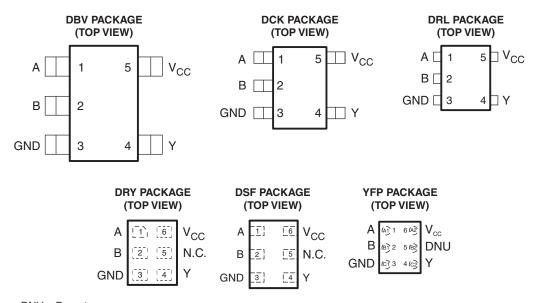
LOW-POWER SINGLE 2-INPUT POSITIVE-NOR GATE

Check for Samples: SN74AUP1G02

FEATURES

- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption (I_{CC} = 0.9 μA Max)
- Low Dynamic-Power Consumption (C_{pd} = 4.3 pF Typ at 3.3 V)
- Low Input Capacitance (C_i = 1.5 pF Typ)
- Low Noise Overshoot and Undershoot <10% of V_{CC}
- I_{off} Supports Partial-Power-Down Mode Operation
- Input Hysteresis Allows Slow Input Transition and Better Switching-Noise Immunity at the Input (V_{hvs} = 250 mV Typ at 3.3 V)

- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{nd} = 4.6 \text{ ns Max at } 3.3 \text{ V}$
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)



DNU – Do not use N.C. – No internal connection See mechanical drawings for dimensions.

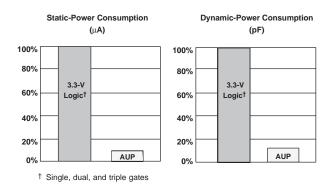
DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in increased battery life (see Figure 1). This product also maintains excellent signal integrity (see Figure 1 and Figure 2).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





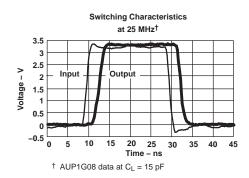


Figure 1. AUP - The Lowest-Power Family

Figure 2. Excellent Signal Integrity

This single 2-input positive-NOR gate performs the Boolean function $Y = \overline{A} + \overline{B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION(1)

T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING (3)	
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YFP (Pb-free)		SN74AUP1G02YFPR	HB_	
	QFN – DRY	Reel of 5000	SN74AUP1G02DRYR	НВ	
-40°C to 85°C	uQFN - DSF	Reel of 5000	SN74AUP1G02DSFR	НВ	
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1G02DBVR	H02_	
	SOT (SC-70) - DCK	Reel of 3000	SN74AUP1G02DCKR	HB_	
	SOT (SOT-553) - DRL	Reel of 4000	SN74AUP1G02DRLR	HB_	

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

FUNCTION TABLE

INP	UTS	OUTPUT
Α	В	Υ
L	L	Н
L	Н	L
Н	L	L
Н	Н	L

LOGIC DIAGRAM (POSITIVE LOGIC)



⁽²⁾ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

⁽³⁾ DBV/DCK/DRL: The actual top-side marking has one additional character that designates the wafer fab/assembly site. YFP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	4.6	V
VI	Input voltage range ⁽²⁾		-0.5	4.6	V
Vo	Voltage range applied to any output in the h	nigh-impedance or power-off state (2)	-0.5	4.6	V
Vo	Output voltage range in the high or low state	e ⁽²⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current			±20	mA
	Continuous current through V _{CC} or GND		±50	mA	
		DBV package		206	
		DCK package		252	
0	Dealer at the small instantian of (3)	DRL package		142	9 0 // //
θ_{JA}	Package thermal impedance ⁽³⁾	DSF package		300	°C/W
		DRY package		234	
		YFP package		132	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The package thermal impedance is calculated in accordance with JESD 51-7.



RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT	
V _{CC}	Supply voltage		0.8	3.6	V	
		V _{CC} = 0.8 V	V _{CC}			
.,	High level input values	V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}		V	
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.6		V	
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	2			
		V _{CC} = 0.8 V		0		
\/	Low lovel input veltage	V _{CC} = 1.1 V to 1.95 V		0.35 × V _{CC}	V	
V_{IL}	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		0.9		
V_{I}	Input voltage		0	3.6	V	
Vo	Output voltage		0	V_{CC}	V	
		V _{CC} = 0.8 V		-20	μΑ	
		V _{CC} = 1.1 V		-1.1		
	High level output ourrent	V _{CC} = 1.4 V		-1.7		
I _{OH}	High-level output current	V _{CC} = 1.65 V		-1.9	mA	
		V _{CC} = 2.3 V		-3.1		
		V _{CC} = 3 V		-4		
		V _{CC} = 0.8 V		20	μΑ	
		$V_{CC} = 1.1 \text{ V}$		1.1		
	Low level output current	V _{CC} = 1.4 V		1.7		
I _{OL}	Low-level output current	V _{CC} = 1.65 V		1.9	mA	
	V _{CC} = 2.3 V			3.1		
		V _{CC} = 3 V		4		
Δt/Δν	Input transition rise or fall rate	V _{CC} = 0.8 V to 3.6 V		200	ns/V	
T _A	Operating free-air temperature		-40	85	°C	

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

	TEST CONDITIONS	v	Т	_A = 25°C	$T_A = -40^{\circ}C$	to 85°C	LINUT			
PARAMETER	R TEST CONDITIONS	V _{cc}	MIN	TYP MAX	MIN	MAX	UNIT			
	I _{OH} = -20 μA	0.8 V to 3.6 V	V _{CC} - 0.1		V _{CC} - 0.1					
	I _{OH} = -1.1 mA	1.1 V	0.75 × V _{CC}		0.7 × V _{CC}					
	$I_{OH} = -1.7 \text{ mA}$	1.4 V	1.11		1.03					
V _{OH}	$I_{OH} = -1.9 \text{ mA}$	1.65 V	1.32		1.3		V			
	$I_{OH} = -2.3 \text{ mA}$	221/	2.05		1.97					
	$I_{OH} = -3.1 \text{ mA}$	2.3 V	1.9		1.85					
	$I_{OH} = -2.7 \text{ mA}$	2.1/	2.72		2.67					
	$I_{OH} = -4 \text{ mA}$	3 V	2.6		2.55					
	I _{OL} = 20 μA	0.8 V to 3.6 V		0.1		0.1				
	I _{OL} = 1.1 mA	1.1 V		0.3 × V _{CC}		$0.3 \times V_{CC}$				
	I _{OL} = 1.7 mA	1.4 V		0.31		0.37				
.,	I _{OL} = 1.9 mA	1.65 V		0.31		0.35	V			
V_{OL}	I _{OL} = 2.3 mA	0.01/		0.31		0.33				
	I _{OL} = 3.1 mA	2.3 V		0.44		0.45				
	I _{OL} = 2.7 mA	2.1/		0.31		0.33				
	I _{OL} = 4 mA	3 V		0.44		0.45				
I _I A or B inputs	V _I = GND to 3.6 V	0 V to 3.6 V		0.1		0.5	μΑ			
I _{off}	V_I or $V_O = 0 V$ to 3.6 V	0 V		0.2		0.6	μΑ			
Δl _{off}	V_I or $V_O = 0$ V to 3.6 V	0 V to 0.2 V		0.2		0.6	μΑ			
I _{CC}	$V_I = GND \text{ or } (V_{CC} \text{ to } 3.6 \text{ V}),$ $I_O = 0$	0.8 V to 3.6 V		0.5		0.9	μА			
ΔI _{CC}	$V_I = V_{CC} - 0.6 V^{(1)},$ $I_O = 0$	3.3 V		40		50	μΑ			
	V – V or CND	0 V		1.5			nF.			
C _i	$V_I = V_{CC}$ or GND	3.6 V		1.5			pF			
C _o	V _O = GND	0 V		3			pF			

⁽¹⁾ One input at V_{CC} – 0.6 V, other input at V_{CC} or GND.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 5 pF$ (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM	то	V	T,	4 = 25°C	3	$T_A = -40^{\circ}C t$	o 85°C	UNIT
PARAMETER	(INPUT)	(OUTPUT)	V _{CC}	MIN	TYP	MAX	MIN	MAX	UNII
			0.8 V		19.3				
			1.2 V ± 0.1 V	2.6	7.3	13	2.1	16.3	
	A or D		1.5 V ± 0.1 V	1.4	5.2	8.9	0.9	10.8	
t _{pd}	A or B	Ť	1.8 V ± 0.15 V	1	4.2	6.8	0.5	8.7	ns
		-	2.5 V ± 0.2 V	1	3	4.6	0.5	5.9	
			3.3 V ± 0.3 V	1	2.4	3.7	0.5	4.6	

Product Folder Link(s): SN74AUP1G02



SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 10 \text{ pF}$ (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM	то	V	T _A	= 25°C	;	$T_A = -40^{\circ}C$ to	o 85°C	UNIT
PARAMETER	(INPUT)	(OUTPUT)	V _{cc}	MIN	TYP	MAX	MIN	MAX	UNII
			0.8 V		22.3				
			1.2 V ± 0.1 V	1.5	8.5	14.9	1	17.9	
	A D		1.5 V ± 0.1 V	1	6.2	10.2	0.5	11.8	20
t _{pd}	A or B	Ť	1.8 V ± 0.15 V	1	5	7.9	0.5	9.5	ns
			2.5 V ± 0.2 V	1	3.6	5.4	0.5	6.5	
			3.3 V ± 0.3 V	1	2.9	4.4	0.5	5	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM	то	V	T,	₄ = 25°C	;	$T_A = -40^{\circ}C t$	o 85°C	UNIT		
PARAMETER	(INPUT)	(OUTPUT)	V _{CC}	MIN	TYP	MAX	MIN	MAX	UNIT		
	0.8 V		25								
			1.2 V ± 0.1 V	3.6	9.9	16.5	3.1	20.6			
	t _{pd} A or B	A == D		V	1.5 V ± 0.1 V	2.3	7.2	11.3	1.8	13.7	20
^L pd		,	1.8 V ± 0.15 V	1.6	5.8	8.9	1.1	11.1	ns		
			2.5 V ± 0.2 V	1	4.3	6.1	0.5	7.7			
			3.3 V ± 0.3 V	1	3.4	5	0.5	6.2			

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM	то	V	T,	₄ = 25°C		T _A = -40°C t	o 85°C	UNIT
PARAMETER	(INPUT)	(OUTPUT)	V _{CC}	MIN	TYP	MAX	MIN	MAX	UNII
		0.8 V		34.6					
		V	1.2 V ± 0.1 V	4.9	13.1	21.1	4.4	26.2	
	A or B		1.5 V ± 0.1 V	3.4	9.5	14.4	2.9	17.4	20
t _{pd}	AUID	ı	1.8 V ± 0.15 V	2.5	7.7	11.2	2	14	ns
			2.5 V ± 0.2 V	1.8	5.7	7.8	1.3	9.8	
			3.3 V ± 0.3 V	1.5	4.7	6.4	1	7.8	

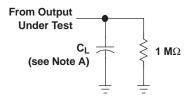
OPERATING CHARACTERISTICS

 $T_{\Delta} = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	V _{cc}	TYP	UNIT
		0.8 V	4.1		
	C. Deven discipation associates	f = 10 MHz	1.2 V ± 0.1 V	4.1	~F
C			1.5 V ± 0.1 V	4.1	
C _{pd}	Power dissipation capacitance		1.8 V ± 0.15 V	4.1	pF
			2.5 V ± 0.2 V	4.2	
			3.3 V ± 0.3 V	4.3	

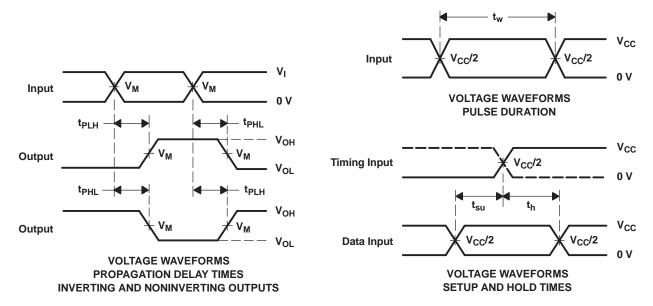


PARAMETER MEASUREMENT INFORMATION (Propagation Delays, Setup and Hold Times, and Pulse Duration)



LOAD CIRCUIT

	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V	V _{CC} = 1.5 V ± 0.1 V	V _{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V \pm 0.2 V	V _{CC} = 3.3 V ± 0.3 V
C _L V _M	5, 10, 15, 30 pF V _{CC} /2 V _{CC}	5, 10, 15, 30 pF V _{CC} /2 V _{CC}	5, 10, 15, 30 pF V _{CC} /2 V _{CC}	5, 10, 15, 30 pF V _{CC} /2 V _{CC}	5, 10, 15, 30 pF V _{CC} /2 V _{CC}	5, 10, 15, 30 pF V _{CC} /2 V _{CC}



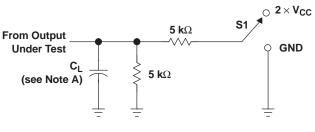
NOTES: A. C_L includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_{O} = 50 Ω , t_{r}/t_{f} = 3 ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D. t_{PLH} and t_{PHL} are the same as t_{pd} .
- E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms



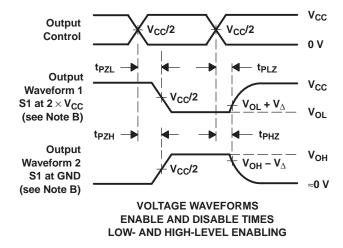
PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



TEST	S1
t _{PLZ} /t _{PZL}	2×V _{CC}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V	V _{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V \pm 0.15 V	V_{CC} = 2.5 V \pm 0.2 V	V _{CC} = 3.3 V ± 0.3 V
C _L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V _M	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2	V _{CC} /2
V _I	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}	V _{CC}
V _∆	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \ \Omega$, $t_r/t_f = 3 \ ns$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

21-Oct-2011

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74AUP1G02DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1G02DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1G02DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1G02DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1G02DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1G02DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1G02DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1G02DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1G02DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1G02DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1G02DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1G02DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1G02DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1G02DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1G02DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1G02DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AUP1G02YFPR	ACTIVE	DSBGA	YFP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	



PACKAGE OPTION ADDENDUM

21-Oct-2011

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

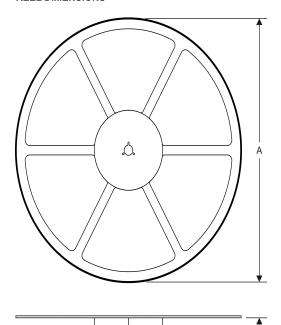
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

www.ti.com 9-May-2012

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G02DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G02DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G02DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G02DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74AUP1G02DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G02DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G02DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G02DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G02YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G02DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G02DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AUP1G02DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1G02DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74AUP1G02DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G02DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
SN74AUP1G02DRYR	SON	DRY	6	5000	180.0	180.0	30.0
SN74AUP1G02DSFR	SON	DSF	6	5000	180.0	180.0	30.0
SN74AUP1G02YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.



DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.



DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE



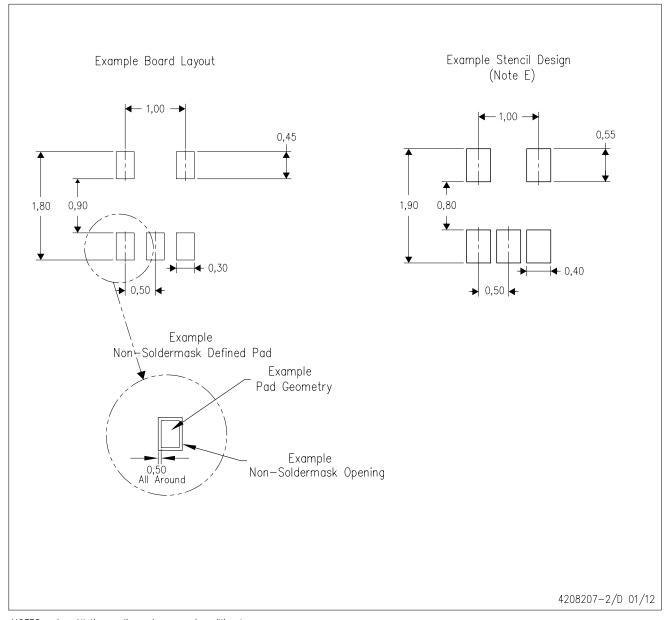
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs.

 Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
- D. JEDEC package registration is pending.



DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over—print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.





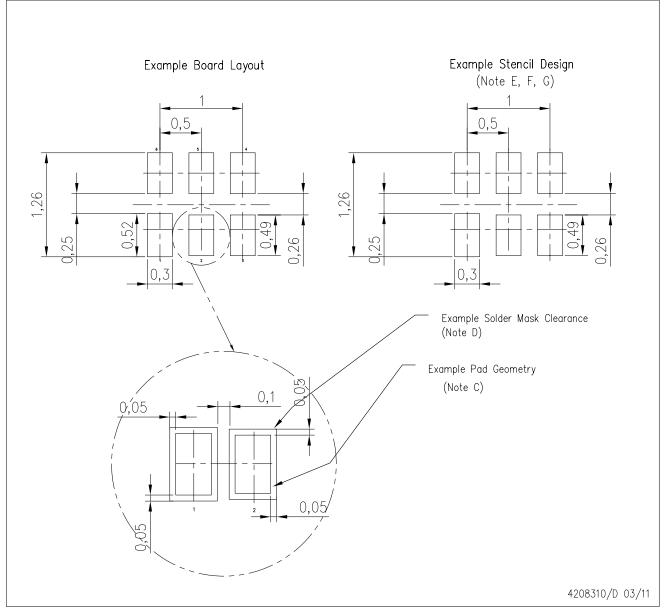
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. SON (Small Outline No-Lead) package configuration.
- The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
- E. This package complies to JEDEC MO-287 variation UFAD.
- $frac{f}{K}$ See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.



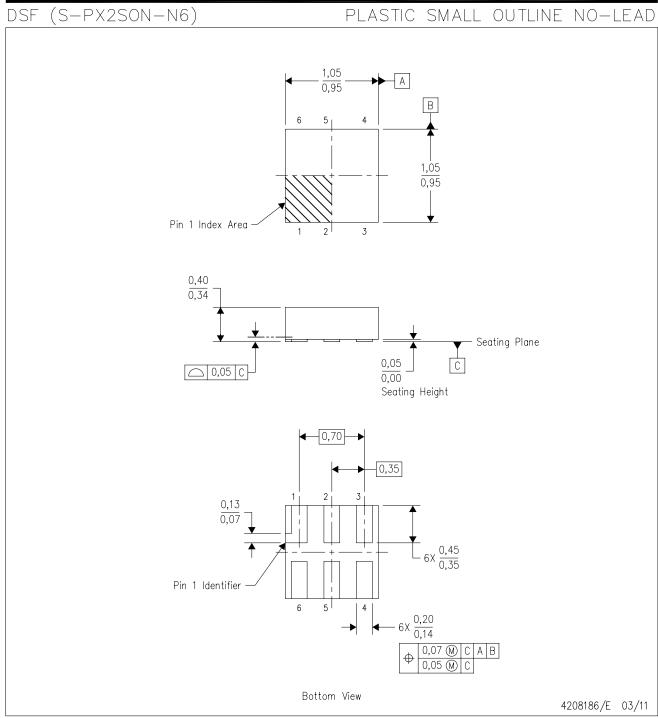
DRY (S-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.





NOTES: All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.

- B. This drawing is subject to change without notice.
 C. SON (Small Outline No-Lead) package configuration.
 D. This package complies to JEDEC MO-287 variation X2AAF.





PLASTIC SMALL OUTLINE NO-LEAD

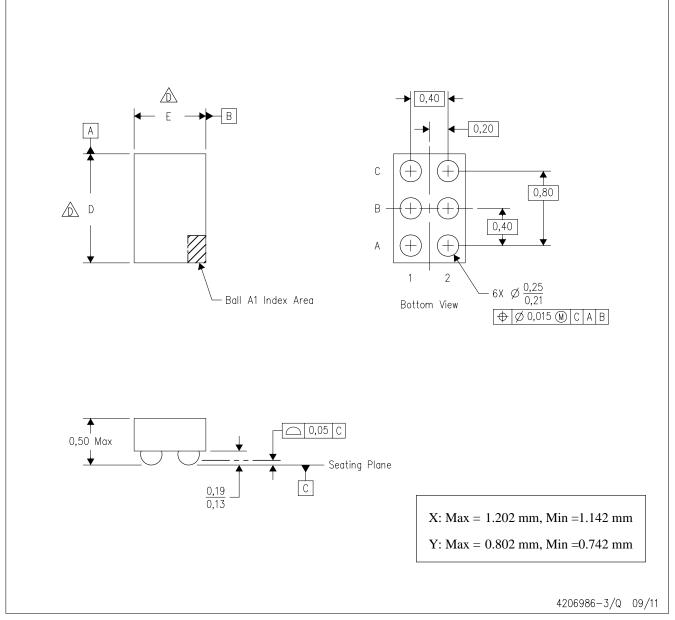


- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
- E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
- H. Component placement force should be minimized to prevent excessive paste block deformation.



YFP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.

The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.

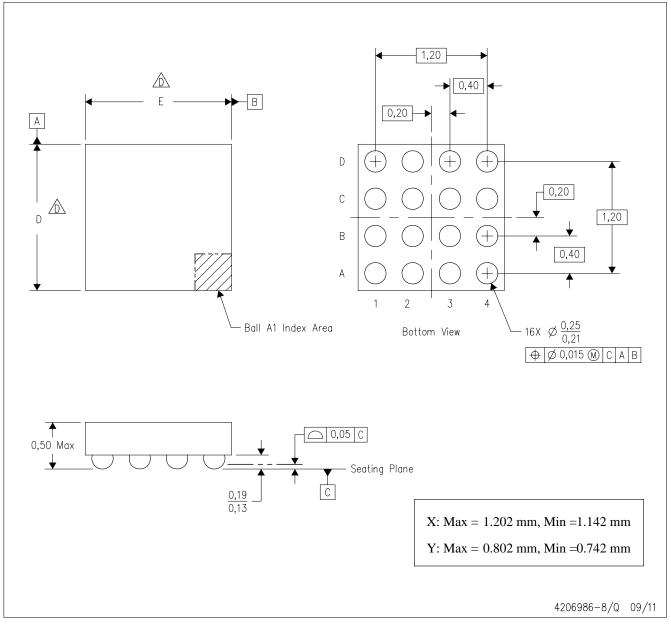
- E. Reference Product Data Sheet for array population. 2 x 3 matrix pattern is shown for illustration only.
- F. This package contains Pb-free balls.

NanoFree is a trademark of Texas Instruments



YFP (S-XBGA-N16)

DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
- E. Reference Product Data Sheet for array population.4 x 4 matrix pattern is shown for illustration only.
- F. This package contains Pb-free balls.

NanoFree is a trademark of Texas Instruments



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