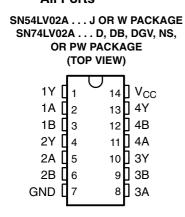
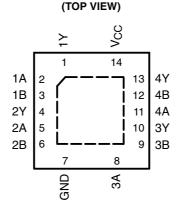
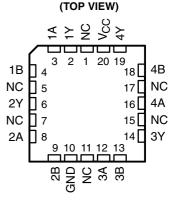
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- 2-V to 5.5-V V<sub>CC</sub> Operation
- Max t<sub>pd</sub> of 6.5 ns at 5 V
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   >2.3 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)





SN74LV02A . . . RGY PACKAGE



SN54LV02A . . . FK PACKAGE

NC - No internal connection

### description/ordering information

The 'LV02A devices are quadruple 2-input positive-NOR gates designed for 2-V to 5.5-V V<sub>CC</sub> operation.

The 'LV02A devices perform the Boolean function  $Y = \overline{A + B}$  or  $Y = \overline{A} \bullet \overline{B}$  in positive logic.

These devices are fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

#### **ORDERING INFORMATION**

T <sub>A</sub>	PACK	AGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	QFN – RGY	Reel of 1000	SN74LV02ARGYR	LV02A
	COIC D	Tube of 50	SN74LV02AD	11/004
	SOIC – D	Reel of 2500	SN74LV02ADR	LV02A
	SOP - NS	Reel of 2000	SN74LV02ANSR	74LV02A
-40°C to 85°C	SSOP – DB	Reel of 2000	SN74LV02ADBR	LV02A
		Tube of 90	SN74LV02APW	
	TSSOP - PW	Reel of 2000	SN74LV02APWR	LV02A
		Reel of 250	SN74LV02APWT	
	TVSOP - DGV	Reel of 2000	SN74LV02ADGVR	LV02A
	CDIP – J	Tube of 25	SNJ54LV02AJ	SNJ54LV02AJ
–55°C to 125°C	CFP – W	Tube of 150	SNJ54LV02AW	SNJ54LV102AW
	LCCC - FK	Tube of 55	SNJ54LV02AFK	SNJ54LV02AFK

<sup>&</sup>lt;sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



# FUNCTION TABLE (each gate)

INP	UTS	OUTPUT
Α	В	Υ
Н	Х	L
Х	Н	L
L	L	Н

### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high-impedance	
or power-off state, V <sub>O</sub> (see Note 1)	–0.5 V to 7 V
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	
Continuous current through V <sub>CC</sub> or GND	
Package thermal impedance, θ <sub>JA</sub> (see Note 3): D package	
(see Note 3): DB package	
(see Note 3): DGV package	
(see Note 3): NS package	
(see Note 3): PW package	
(see Note 4): RGY package	
Storage temperature range, T <sub>sto</sub>	

<sup>&</sup>lt;sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. This value is limited to 5.5 V maximum.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.
  - 4. The package thermal impedance is calculated in accordance with JESD 51-5.

### recommended operating conditions (see Note 5)

			SN54L	.V02A	SN74L	.V02A	
			MIN	MAX	MIN	MAX	UNIT
$V_{CC}$	Supply voltage		2	5.5	2	5.5	V
		V <sub>CC</sub> = 2 V	1.5		1.5		
W	High laveling Avellage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		v
V <sub>IH</sub>	High-level input voltage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V <sub>CC</sub> = 2 V		0.5		0.5	
.,	Lauria de la la contra de la contra del la contra del la contra del la contra de la contra del la contra de la contra del l	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	V
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
VI	Input voltage		0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	0	$V_{CC}$	V
		V <sub>CC</sub> = 2 V	5	-50		-50	μΑ
١.	High lavel autout average	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	90	-2		-2	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 3 V to 3.6 V	0	-6		-6	mA
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		-12		-12	
		V <sub>CC</sub> = 2 V		50		50	μΑ
١.	I am laval ambant amant	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		2		2	
I <sub>OL</sub>	Low-level output current	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		6		6	mA
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		12		12	
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		200		200	
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		100		100	ns/V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		20		20	
$T_A$	Operating free-air temperature		-55	125	-40	85	°C

NOTE 5: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

24244555	TEST SOURITIONS		SN54LV02	2A	SN7	4LV02A		
PARAMETER	TEST CONDITIONS	v <sub>cc</sub>	MIN TYI	MAX	MIN	TYP	MAX	UNIT
	$I_{OH} = -50 \mu\text{A}$	2 V to 5.5 V	V <sub>CC</sub> -0.1		V <sub>CC</sub> -0.1			
.,,	$I_{OH} = -2 \text{ mA}$	2.3 V	2		2			V
V <sub>OH</sub>	$I_{OH} = -6 \text{ mA}$	3 V	2.48	_	2.48			V
	$I_{OH} = -12 \text{ mA}$	4.5 V	3.8		3.8			
	$I_{OL} = 50 \mu A$	2 V to 5.5 V	17/2	0.1			0.1	
N/	I <sub>OL</sub> = 2 mA	2.3 V	d.	0.4			0.4	V
V <sub>OL</sub>	I <sub>OL</sub> = 6 mA	3 V	Ό,	0.44			0.44	V
	I <sub>OL</sub> = 12 mA	4.5 V	a	0.55			0.55	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V	Y <sub>Q</sub>	±1			±1	μΑ
I <sub>CC</sub>	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V	,	20		•	20	μΑ
l <sub>off</sub>	$V_{I}$ or $V_{O} = 0$ to 5.5 V	0		5			5	μΑ
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	1.0	5		1.6		pF

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# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V $\pm$ 0.2 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	LOAD	LOAD T		T <sub>A</sub> = 25°C		SN74LV02A		
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN MAX	MIN	MAX	UNIT
+ .	A or B	V	C <sub>L</sub> = 15 pF		8.3*	12.4*	1* 15*	1	15	no
<sup>t</sup> pd	AUID	r	C <sub>L</sub> = 50 pF		11	16.1	1 19	1	19	ns

<sup>\*</sup> On products compliant to MIL-PRF-38535, this parameter is not production tested.

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	LOAD	T,	<sub>A</sub> = 25°C	;	SN54LV02A	SN74L	V02A	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN MAX	MIN	MAX	UNIT
+ .	A or B	V	C <sub>L</sub> = 15 pF		5.6*	7.9*	1* 9.5*	1	9.5	20
<sup>t</sup> pd	AUID	r	C <sub>L</sub> = 50 pF		7.6	11.4	1 13	1	13	ns

<sup>\*</sup> On products compliant to MIL-PRF-38535, this parameter is not production tested.

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	LOAD	$T_A = 25^{\circ}C$		SN54LV02A	SN74L	V02A		
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN MAX	MIN	MAX	UNIT
t. a	A or B	~	C <sub>L</sub> = 15 pF		3.9*	5.5*	<b>1</b> * 6.5*	1	6.5	ne
t <sub>pd</sub>	AUID	ľ	C <sub>L</sub> = 50 pF		5.3	7.5	8.5	1	8.5	ns

<sup>\*</sup> On products compliant to MIL-PRF-38535, this parameter is not production tested.

### noise characteristics, $V_{CC} = 3.3 \text{ V}$ , $C_L = 50 \text{ pF}$ , $T_A = 25^{\circ}\text{C}$ (see Note 6)

	DADAMETED	SN	SN74LV02A			
	PARAMETER	MIN	TYP	MAX	UNIT	
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>		0.2	8.0	٧	
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>		-0.1	-0.8	٧	
V <sub>OH(V)</sub>	Quiet output, minimum dynamic V <sub>OH</sub>		3.2		٧	
V <sub>IH(D)</sub>	High-level dynamic input voltage	2.31			٧	
V <sub>IL(D)</sub>	Low-level dynamic input voltage			0.99	V	

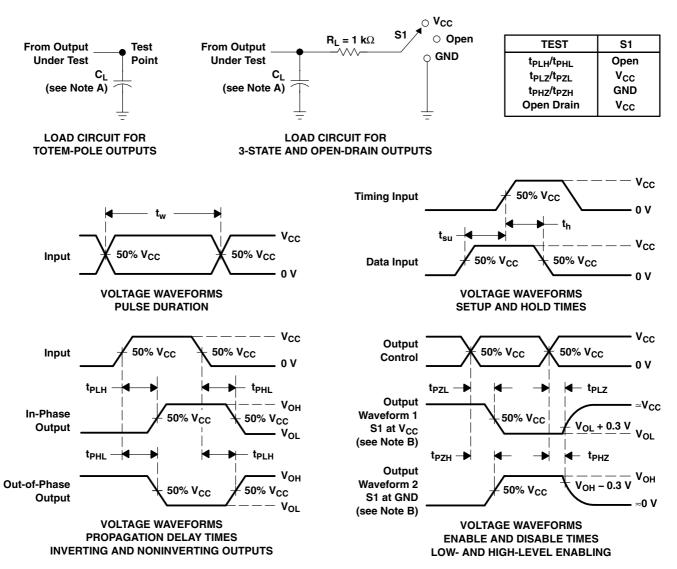
NOTE 6: Characteristics are for surface-mount packages only.

### operating characteristics, T<sub>A</sub> = 25°C

	PARAMETER	TEST CO	V <sub>CC</sub>	TYP	UNIT	
(	Power discinction conscitones	C = 50 pE	f = 10 MHz	3.3 V	8.9	pF
$c_{pd}$	Power dissipation capacitance	$C_L = 50 \text{ pF},$	1 = 10 MHZ	5 V	10.3	рг



#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq 3$  ns.  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms





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### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LV02AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02ADBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02ADBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02ADGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02ADGVRE4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02ADGVRG4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02ANSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02APW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02APWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02APWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02APWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02APWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02APWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02APWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02APWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV02ARGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR



#### PACKAGE OPTION ADDENDUM

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Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins Pa	ackage Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LV02ARGYRG4	ACTIVE	VQFN	RGY	14 ;	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

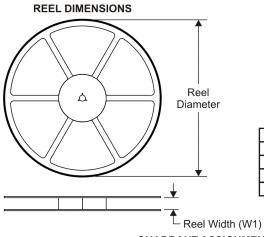
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**PACKAGE MATERIALS INFORMATION** 

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### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV02ADBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LV02ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV02ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV02ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV02APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV02APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV02ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
SN74LV02ADBR	SSOP	DB	14	2000	346.0	346.0	33.0	
SN74LV02ADGVR	TVSOP	DGV	14	2000	346.0	346.0	29.0	
SN74LV02ADR	SOIC	D	14	2500	346.0	346.0	33.0	
SN74LV02ANSR	SO	NS	14	2000	346.0	346.0	33.0	
SN74LV02APWR	TSSOP	PW	14	2000	346.0	346.0	29.0	
SN74LV02APWT	TSSOP	PW	14	250	346.0	346.0	29.0	
SN74LV02ARGYR	VQFN	RGY	14	3000	346.0	346.0	29.0	

### DGV (R-PDSO-G\*\*)

### **24 PINS SHOWN**

### **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194

## D (R-PDSO-G14)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



# D (R-PDSO-G14)

## PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
  - Sody length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



# PW (R-PDSO-G14)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.





NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.



### RGY (S-PVQFN-N14)

### PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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NOTE: All linear dimensions are in millimeters



## RGY (S-PVQFN-N14)

### PLASTIC QUAD FLATPACK NO-LEAD



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <a href="https://www.ti.com">http://www.ti.com</a>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



### **MECHANICAL DATA**

### NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



### DB (R-PDSO-G\*\*)

### PLASTIC SMALL-OUTLINE

### **28 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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