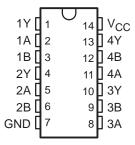
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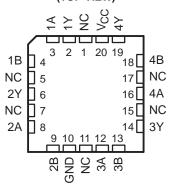
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20-μA Max I_{CC}

SN54HC02...J OR W PACKAGE SN74HC02...D, DB, N, NS, OR PW PACKAGE (TOP VIEW)



- Typical t_{pd} = 8 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1 μA Max

SN54HC02...FK PACKAGE (TOP VIEW)



NC - No internal connection

description/ordering information

The 'HC02 devices contain four independent 2-input NOR gates. They perform the Boolean function $Y = \overline{A} + \overline{B}$ or $Y = \overline{A} \bullet \overline{B}$ in positive logic.

ORDERING INFORMATION

TA	PACKA	GE [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube of 25	SN74HC02N	SN74HC02N
		Tube of 50	SN74HC02D	
	SOIC - D	Reel of 2500	SN74HC02DR	HC02
		Reel of 250	SN74HC02DT	
-40°C to 85°C	SOP - NS	Reel of 2000	SN74HC02NSR	HC02
	SSOP – DB	Reel of 2000	SN74HC02DBR	HC02
		Tube of 90	SN74HC02PW	
	TSSOP - PW	Reel of 2000	SN74HC02PWR	HC02
		Reel of 250	SN74HC02PWT	
	CDIP – J	Tube of 25	SNJ54HC02J	SNJ54HC02J
–55°C to 125°C	CFP – W	Tube of 150	SNJ54HC02W	SNJ54HC02W
	LCCC – FK	Tube of 55	SNJ54HC02FK	SNJ54HC02FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



FUNCTION TABLE (each gate)

INP	UTS	OUTPUT
Α	В	Υ
Н	Χ	L
X	Н	L
L	L	Н

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (se	e Note 1)	±20 mA
Output clamp current, IOK (VO < 0 or VO > VCC	;) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})		±25 mA
Continuous current through V _{CC} or GND		±50 mA
Package thermal impedance, θ _{JA} (see Note 2):	D package	86°C/W
	DB package	96°C/W
	N package	80°C/W
	NS package	76°C/W
	PW package	113°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions (see Note 3)

			S	N54HC0	2	S	N74HC0	2	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2	5	6	2	5	6	V
		V _{CC} = 2 V	1.5			1.5			
VIH	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			V
		V _{CC} = 6 V	4.2			4.2			
		V _{CC} = 2 V			0.5			0.5	
\vee_{IL}	Low-level input voltage	V _{CC} = 4.5 V			1.35			1.35	V
		V _{CC} = 6 V			1.8			1.8	
٧ _I	Input voltage		0		VCC	0		VCC	V
٧o	Output voltage		0		VCC	0		VCC	V
		V _{CC} = 2 V			1000			1000	
Δt/Δν	Input transition rise/fall time	V _{CC} = 4.5 V			500			500	ns
		V _{CC} = 6 V			400			400	
T _A	Operating free-air temperature		-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST OF	MOITIONS	vcc	Т	A = 25°C	;	SN54I	HC02	SN74H	HC02	UNIT
PARAMETER	lesi cc	TEST CONDITIONS		MIN	TYP	MAX	MIN	MAX	MIN	MAX	ONIT
			2 V	1.9	1.998		1.9		1.9		
	V _{OH} V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		4.4		
Voн			6 V	5.9	5.999		5.9		5.9		V
		I _{OH} = -4 mA	4.5 V	3.98	4.3		3.7		3.84		
		$I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.8		5.2		5.34		
			2 V		0.002	0.1		0.1		0.1	
		$I_{OL} = 20 \mu A$	4.5 V		0.001	0.1		0.1		0.1	
V _{OL}	$V_I = V_{IH}$ or V_{IL}		6 V		0.001	0.1		0.1		0.1	V
		$I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26		0.4		0.33	
		$I_{OL} = 5.2 \text{ mA}$	6 V		0.15	0.26		0.4		0.33	
lį	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
Icc	$V_I = V_{CC}$ or 0,	I _O = 0	6 V			2		40		20	μΑ
Ci		_	2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

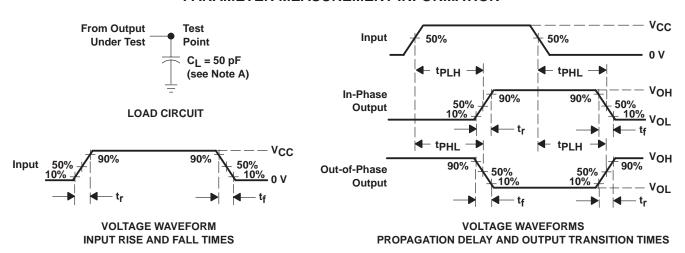
PARAMETER	FROM	TO (OUTPUT)	Vaa	T _A = 25°C			SN54HC02		SN74HC02		UNIT
PARAMETER	(INPUT)		VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V		45	90		135		115	
tpd	t _{pd} A or B	Y	4.5 V		9	18		27		23	ns
				6 V		8	15		23		20
			2 V		38	75		110		95	
t _t		Υ	4.5 V		8	15		22		19	ns
			6 V		6	13		19		16	

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per gate	No load	22	pF

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.

- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_f = 6 ns, t_f = 6 ns.
- C. The outputs are measured one at a time with one input transition per measurement.
- D. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-8404101VCA	ACTIVE	CDIP	J	14	25	TBD	A42	N / A for Pkg Type	
5962-8404101VDA	ACTIVE	CFP	W	14	25	TBD	A42	N / A for Pkg Type	
84041012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
8404101CA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Call TI	
8404101DA	ACTIVE	CFP	W	14	1	TBD	Call TI	Call TI	
JM38510/65101B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/65101BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
JM38510/65101BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
M38510/65101B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/65101BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
M38510/65101BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
SN54HC02J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN74HC02D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC02DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI	
SN74HC02DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC02DBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC02DBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC02DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC02DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC02DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC02DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC02DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74HC02DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC02DTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC02DTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC02N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74HC02N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN74HC02NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74HC02NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC02NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC02PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC02PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC02PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC02PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	
SN74HC02PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC02PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC02PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC02PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC02PWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC02PWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54HC02FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54HC02J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SNJ54HC02W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	

PACKAGE OPTION ADDENDUM



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(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54HC02, SN54HC02-SP, SN74HC02:

Catalog: SN74HC02, SN54HC02

Automotive: SN74HC02-Q1, SN74HC02-Q1

Enhanced Product: SN74HC02-EP, SN74HC02-EP

Military: SN54HC02

Space: SN54HC02-SP

NOTE: Qualified Version Definitions:



23-Mar-2012

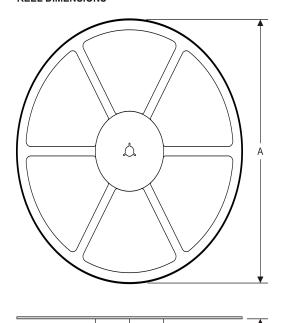
- Catalog TI's standard catalog product
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications
- Space Radiation tolerant, ceramic packaging and qualified for use in Space-based application

PACKAGE MATERIALS INFORMATION

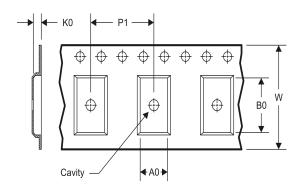
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC02DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74HC02DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC02DT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC02NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC02PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC02PWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC02DBR	SSOP	DB	14	2000	346.0	346.0	33.0
SN74HC02DR	SOIC	D	14	2500	346.0	346.0	33.0
SN74HC02DT	SOIC	D	14	250	346.0	346.0	33.0
SN74HC02NSR	SO	NS	14	2000	346.0	346.0	33.0
SN74HC02PWR	TSSOP	PW	14	2000	346.0	346.0	29.0
SN74HC02PWT	TSSOP	PW	14	250	346.0	346.0	29.0

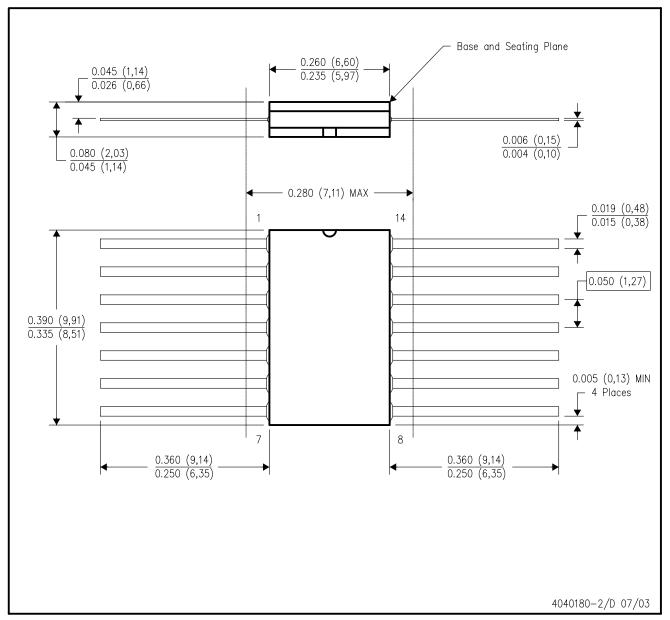
14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB



FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

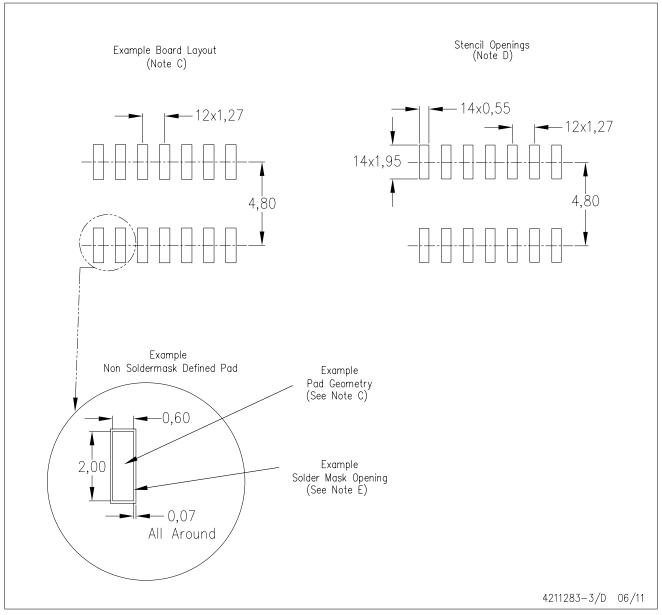


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

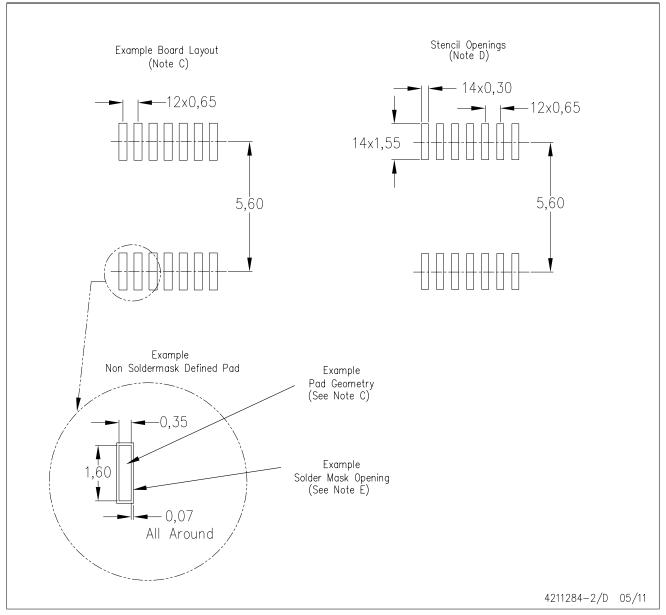


- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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