

74AHC04

Hex inverter

Rev. 03 — 14 November 2007

Product data sheet

1. General description

The 74AHC04 is high-speed Si-gate CMOS devices and is pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7A.

The 74AHC04 is a general purpose hex inverter. Each of the six inverters is a single stage.

2. Features

- Low power dissipation
- Balanced propagation delays
- Inputs accepts voltages higher than V_{CC}
- ESD protection:
 - ◆ HBM JESD22-A114E: exceeds 2000 V
 - ◆ MM JESD22-A115-A: exceeds 200 V
 - ◆ CDM JESD22-C101C: exceeds 1000 V
- Multiple package options
- Specified from -40 °C to $+125\text{ °C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AHC04D	-40 °C to $+125\text{ °C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHC04PW	-40 °C to $+125\text{ °C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHC04BQ	-40 °C to $+125\text{ °C}$	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85\text{ mm}$	SOT762-1

4. Functional diagram

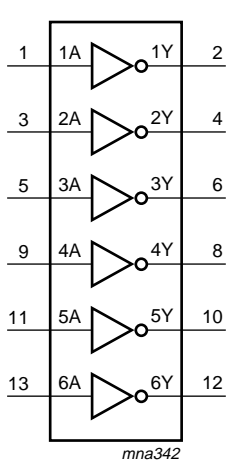


Fig 1. Logic symbol

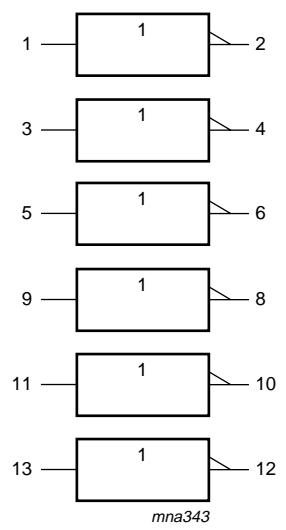


Fig 2. IEC logic symbol

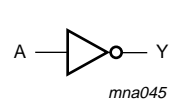


Fig 3. Logic diagram (one inverter)

5. Pinning information

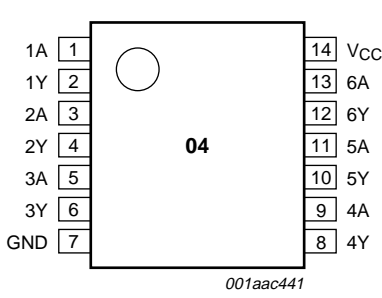


Fig 4. Pin configuration SO14 and TSSOP14

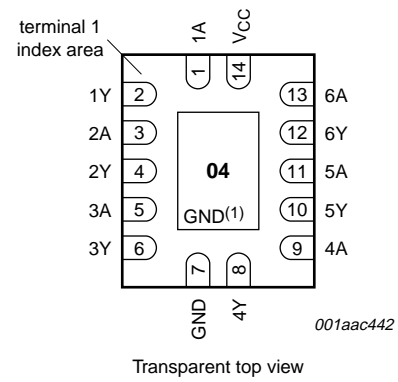


Fig 5. Pin configuration DHVQFN14

(1) The die substrate is attached to the exposed die pad using conductive die attach material. It can not be used as a supply pin or input.

5.1 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A	1	data input
1Y	2	data output
2A	3	data input
2Y	4	data output

Table 2. Pin description ...continued

Symbol	Pin	Description
3A	5	data input
3Y	6	data output
GND	7	ground (0 V)
4Y	8	data output
4A	9	data input
5Y	10	data output
5A	11	data input
6Y	12	data output
6A	13	data input
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level

Input	Output
nA	nY
L	H
H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V	-20	-	mA
V _I	input voltage		[1] -0.5	+7.0	V
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	75	mA
I _{GND}	ground current		-75	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[2] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
 For TSSOP14 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
 For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		2.0	5.0	5.5	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 3.3 V ± 0.3 V	-	-	100	ns/V
		V _{CC} = 5.0 V ± 0.5 V	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.7	-	-	1.7	-	1.7	-	V
		V _{CC} = 3.0 V	2.4	-	-	2.4	-	2.4	-	V
		V _{CC} = 5.5 V	4.4	-	-	4.4	-	4.4	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.3	-	0.3	-	0.3	V
		V _{CC} = 3.0 V	-	-	0.6	-	0.6	-	0.6	V
		V _{CC} = 5.5 V	-	-	1.1	-	1.1	-	1.1	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -50 μA; V _{CC} = 2.0 V	1.8	2.0	-	1.8	-	1.8	-	V
		I _O = -50 μA; V _{CC} = 3.0 V	2.7	3.0	-	2.7	-	2.7	-	V
		I _O = -50 μA; V _{CC} = 4.5 V	4.0	4.5	-	4.0	-	4.0	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.4	-	V
		I _O = -8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.8	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 50 μA; V _{CC} = 2.0 V	-	0	0.2	-	0.2	-	0.2	V
		I _O = 50 μA; V _{CC} = 3.0 V	-	0	0.3	-	0.3	-	0.3	V
		I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.5	-	0.5	-	0.5	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	2.0	-	20	-	40	μA
C _I	input capacitance		-	3	10	-	10	-	10	pF

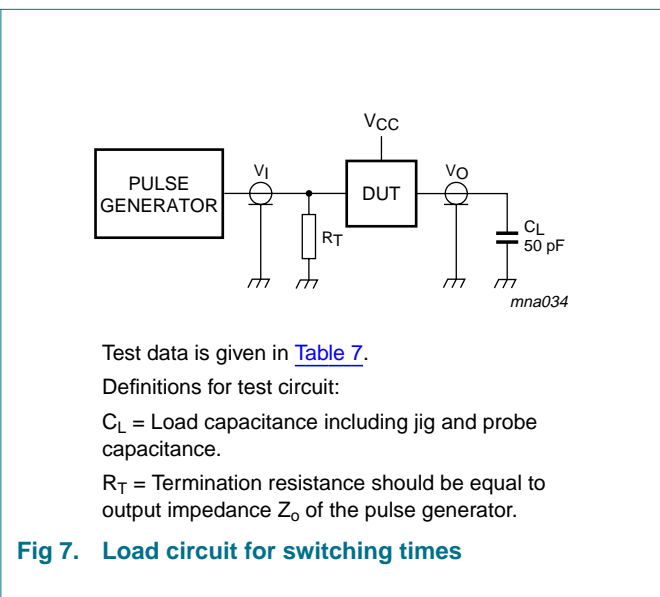
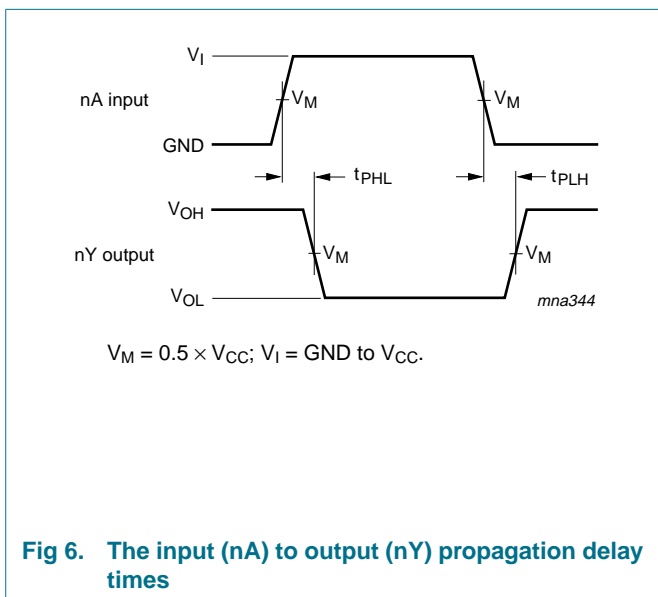
10. Dynamic characteristics

Table 7. Dynamic characteristics
GND = 0 V; For test circuit see Figure 7.

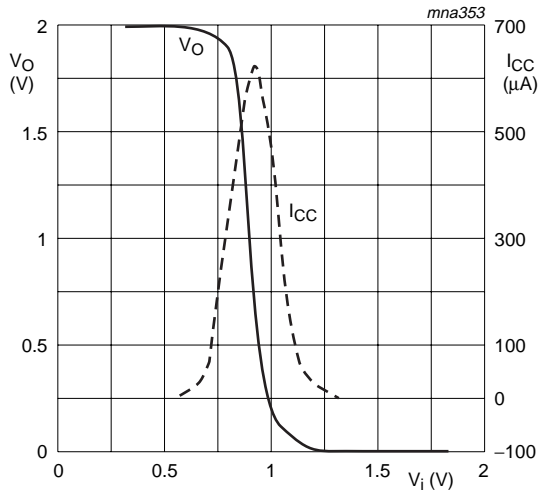
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{pd}	propagation delay	nA to nY; see Figure 6 [1]								
		V _{CC} = 3.0 V to 3.6 V [2]								
		C _L = 15 pF	-	3.0	7.1	1.0	8.5	1.0	9.0	ns
		C _L = 50 pF	-	3.4	10.6	1.0	12.0	1.0	13.5	ns
		V _{CC} = 4.5 V to 5.5 V [3]								
		C _L = 15 pF	-	2.4	5.5	1.0	6.5	1.0	7.0	ns
		C _L = 50 pF	-	3.5	7.0	1.0	8.0	1.0	9.0	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f _i = 1 MHz; V _I = GND to V _{CC} [4]	-	9.1	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [2] Typical values are measured at V_{CC} = 3.3 V.
- [3] Typical values are measured at V_{CC} = 5.0 V.
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms

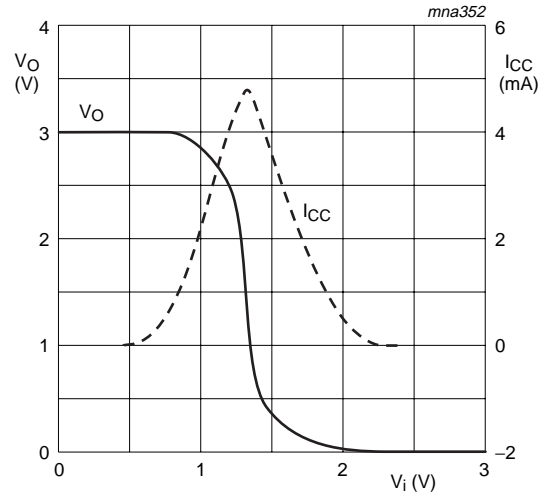


12. Typical transfer characteristics



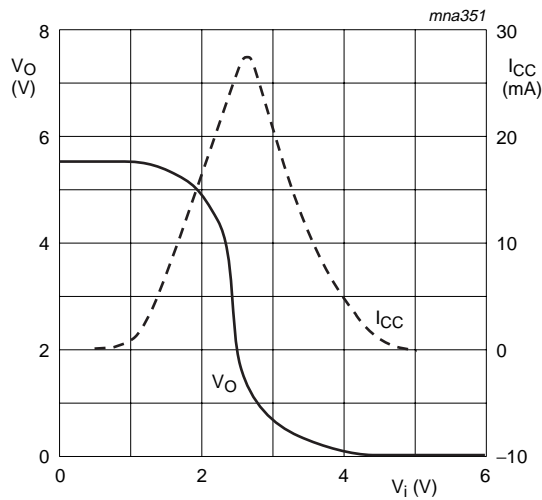
$T_{amb} = 25\text{ }^\circ\text{C}$.

Fig 8. $V_{CC} = 2.0\text{ V}$; $I_O = 0\text{ A}$



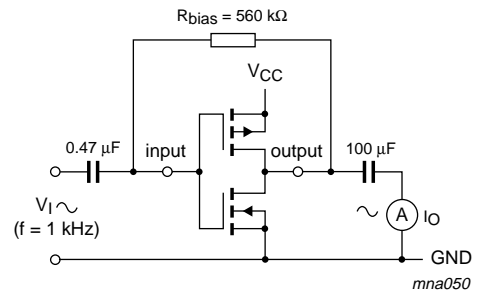
$T_{amb} = 25\text{ }^\circ\text{C}$.

Fig 9. $V_{CC} = 3.0\text{ V}$; $I_O = 0\text{ A}$



$T_{amb} = 25\text{ }^\circ\text{C}$.

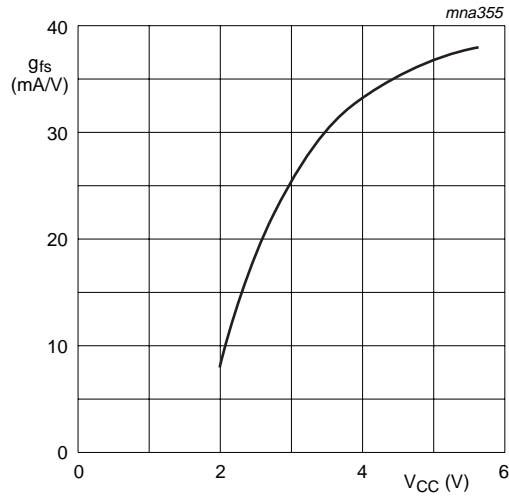
Fig 10. $V_{CC} = 5.5\text{ V}$; $I_O = 0\text{ A}$



$$g_{fs} = \frac{\Delta I_O}{\Delta V_i}$$

$f_i = 1\text{ kHz}$ at V_O is constant

Fig 11. Test set-up for measuring forward transconductance



T_{amb} = 25 °C.

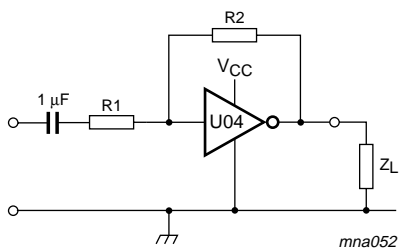
Fig 12. Typical forward transconductance as a function of the supply voltage

13. Application information

Some applications are:

- Linear amplifier (see [Figure 13](#))
- In crystal oscillator design (see [Figure 14](#))

Remark: All values given are typical unless otherwise specified.



Maximum V_{o(p-p)} = V_{CC} - 1.5 V centered at 0.5 × V_{CC}.

$$G_v = -\frac{G_{ol}}{1 + \frac{R1}{R2}(1 + G_{ol})}$$

G_{ol} = open loop gain

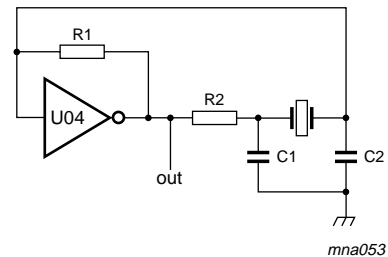
G_v = voltage gain

R1 ≥ 3 kΩ, R2 ≤ 1 MΩ

Z_L > 10 kΩ; G_{ol} = 12 (typical)

Typical unity gain bandwidth product is 5 MHz.

Fig 13. Used as a linear amplifier



C1 = 47 pF (typical)

C2 = 33 pF (typical)

R1 = 1 MΩ to 10 MΩ (typical)

R2 optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} (I_{CC} is typically 5 mA at V_{CC} = 5 V and f_i = 10 MHz).

Fig 14. Crystal oscillator configuration

Table 8. External components for resonator (f < 1 MHz)*All values given are typical and must be used as an initial set-up.*

Frequency	R1	R2	C1	C2
10 kHz to 15.9 kHz	22 M Ω	220 k Ω	56 pF	20 pF
16 kHz to 24.9 kHz	22 M Ω	220 k Ω	56 pF	10 pF
25 kHz to 54.9 kHz	22 M Ω	100 k Ω	56 pF	10 pF
55 kHz to 129.9 kHz	22 M Ω	100 k Ω	47 pF	5 pF
130 kHz to 199.9 kHz	22 M Ω	47 k Ω	47 pF	5 pF
200 kHz to 349.9 kHz	10 M Ω	47 k Ω	47 pF	5 pF
350 kHz to 600 kHz	10 M Ω	47 k Ω	47 pF	5 pF

Table 9. Optimum value for R2

Frequency	R2	Optimum for
3 kHz	2.0 k Ω	minimum required I _{CC}
	8.0 k Ω	minimum influence due to change in V _{CC}
6 kHz	1.0 k Ω	minimum required I _{CC}
	4.7 k Ω	minimum influence by V _{CC}
10 kHz	0.5 k Ω	minimum required I _{CC}
	2.0 k Ω	minimum influence by V _{CC}
14 kHz	0.5 k Ω	minimum required I _{CC}
	1.0 k Ω	minimum influence by V _{CC}
>14 kHz	-	replace R2 by C3 with a typical value of 35 pF

14. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

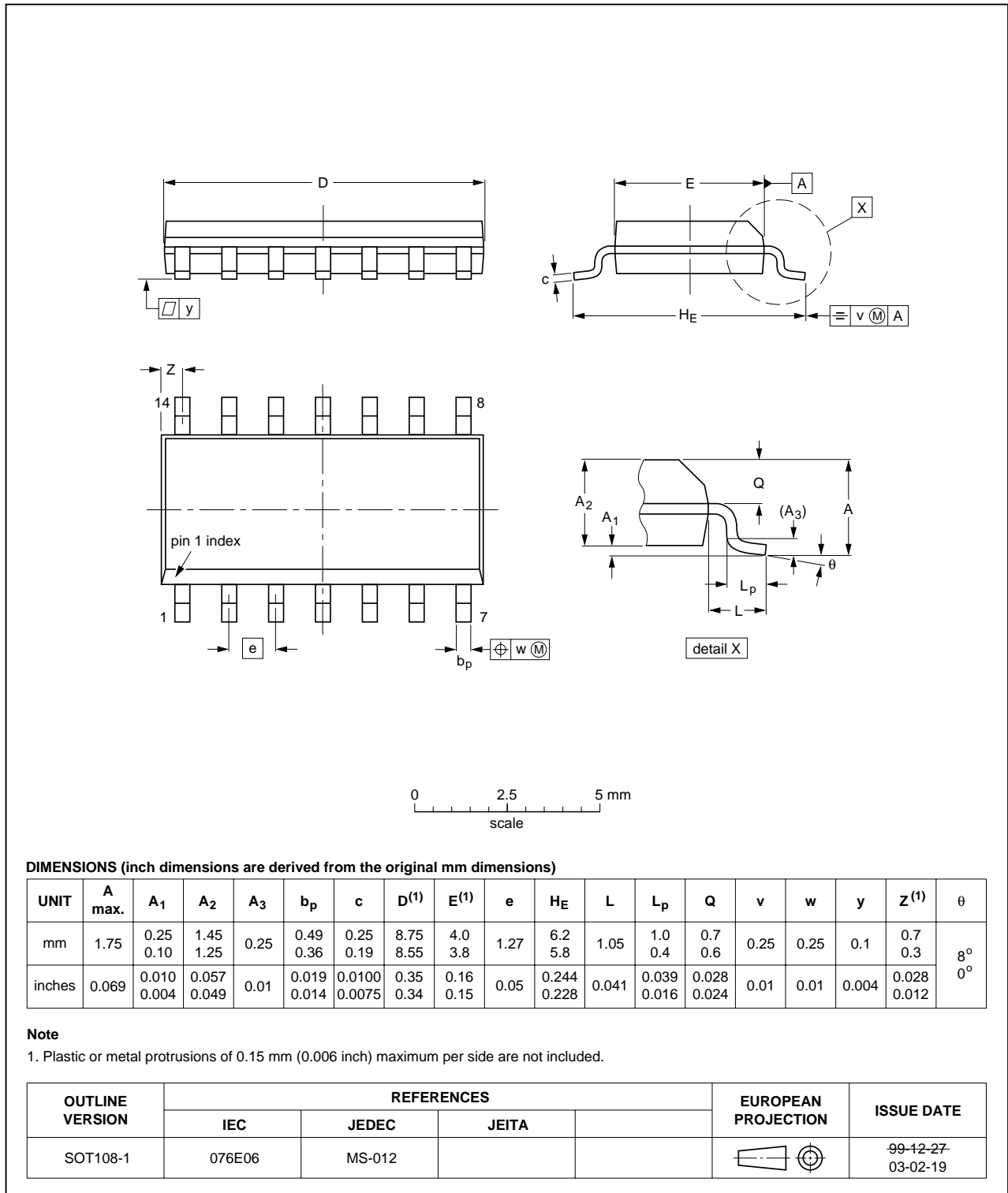


Fig 15. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

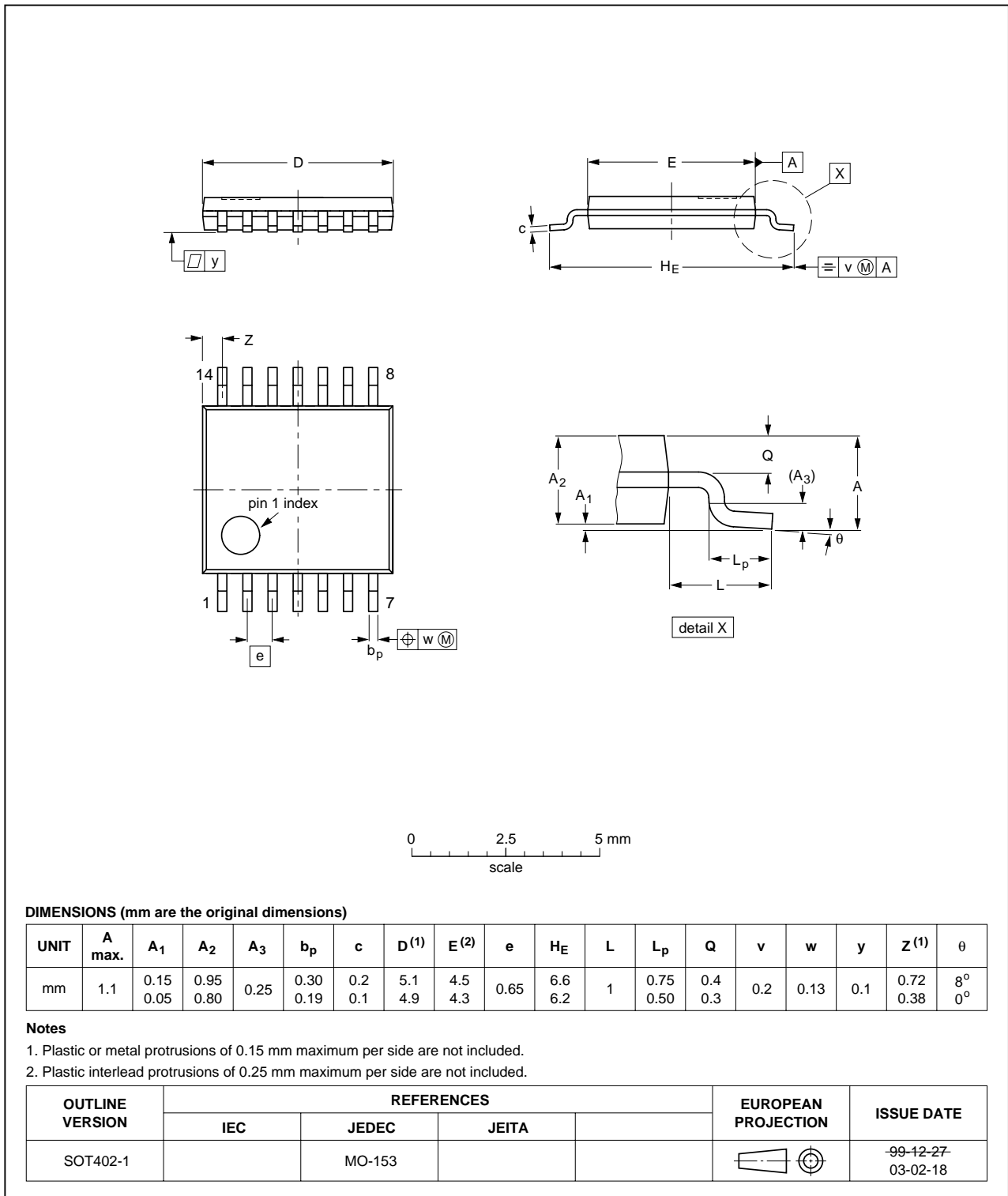


Fig 16. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

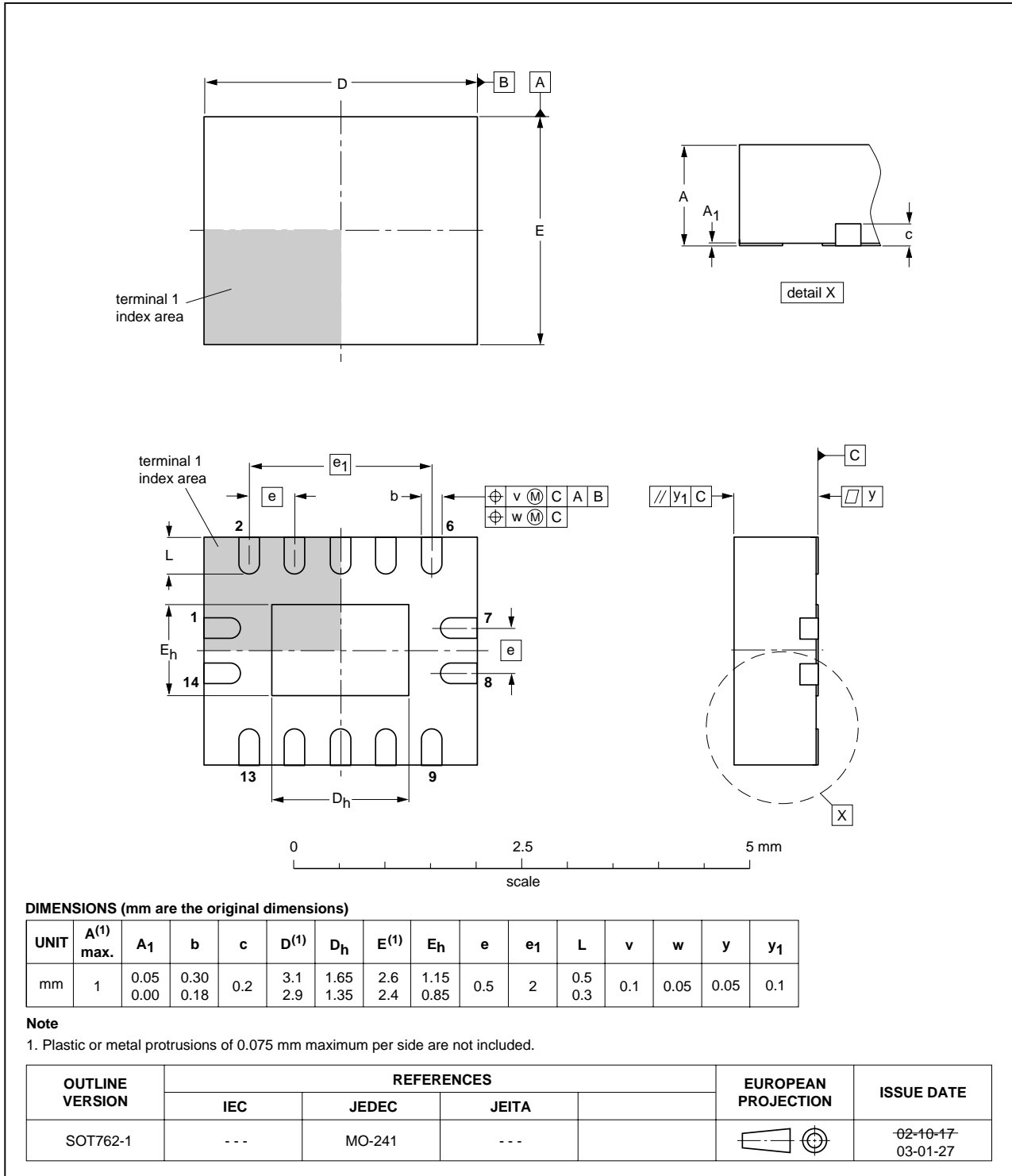


Fig 17. Package outline SOT762-1 (DHVQFN14)

15. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
LSTTL	Low-power Schottky Transistor-Transistor Logic
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
CDM	Charge Device Model
TTL	Transistor-Transistor Logic

16. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHCU04_3	20071114	Product data sheet	-	74AHCU04_2
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 3: DHVQFN14 package added. • Section 8: derating values added for DHVQFN14 package. • Section 14: outline drawing added for DHVQFN14 package. 			
74AHCU04_2	19990927	Product specification	-	74AHCU04_1
74AHCU04_1	19990226	Product specification	-	-

17. Legal information

17.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

17.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

18. Contact information

For additional information, please visit: <http://www.nxp.com>

For sales office addresses, send an email to: salesaddresses@nxp.com

19. Contents

1 General description 1

2 Features 1

3 Ordering information 1

4 Functional diagram 2

5 Pinning information 2

5.1 Pin description 2

6 Functional description 3

7 Limiting values 3

8 Recommended operating conditions 4

9 Static characteristics 4

10 Dynamic characteristics 5

11 Waveforms 5

12 Typical transfer characteristics 6

13 Application information 7

14 Package outline 9

15 Abbreviations 12

16 Revision history 12

17 Legal information 13

17.1 Data sheet status 13

17.2 Definitions 13

17.3 Disclaimers 13

17.4 Trademarks 13

18 Contact information 13

19 Contents 14

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2007.

All rights reserved.

For more information, please visit: <http://www.nxp.com>
 For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 14 November 2007
 Document identifier: 74AHCU04_3