

Low Power Consumption, 10 µA at 1.8 V

Latch-Up Performance Exceeds 100 mA Per

2000-V Human-Body Model (A114-A)

1000-V Charged-Device Model (C101)

±8-mA Output Drive at 1.8 V

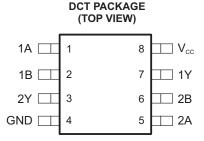
**ESD Protection Exceeds JESD 22** 

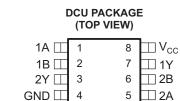
200-V Machine Model (A115-A)

JESD 78. Class II

## FEATURES

- Available in the Texas Instruments NanoFree<sup>™</sup> Package
- Optimized for 1.8-V Operation and Is 3.6-V I/O **Tolerant to Support Mixed-Mode Signal** Operation
- Ioff Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max t<sub>pd</sub> of 1.2 ns at 1.8 V





YEP OR YZP PACKAGE (BOTTOM VIEW)

GND	0450	2A
2Y	0360	2B
1B	0270	1Y
1A	0180	V <sub>cc</sub>

See mechanical drawings for dimensions.

# **DESCRIPTION/ORDERING INFORMATION**

This dual 2-input positive-NAND gate is operational at 0.8-V to 2.7-V V<sub>CC</sub>, but is designed specifically for 1.65-V to 1.95-V V<sub>CC</sub> operation.

The SN74AUC2G00 performs the Boolean function  $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### **ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUC2G00YZPR	UA_
–40°C to 85°C	SSOP – DCT	Reel of 3000	SN74AUC2G00DCTR	U00_
	VSSOP – DCU	Reel of 3000	SN74AUC2G00DCUR	U00_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2)DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site. DCU: The actual top-side marking has one additional character that designates the assembly/test site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.



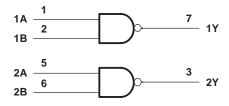
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## SN74AUC2G00 DUAL 2-INPUT POSITIVE-NAND GATE SCES440C-MAY 2003-REVISED JANUARY 2007

## FUNCTION TABLE (EACH GATE)

INPU	JTS	OUTPUT
Α	В	Y
Н	Н	L
L	Х	Н
Х	L	Н

### LOGIC DIAGRAM (POSITIVE LOGIC)



# Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	3.6	V
VI	Input voltage range <sup>(2)</sup>		-0.5	3.6	V
Vo	Voltage range applied to any output in the h	nigh-impedance or power-off state <sup>(2)</sup>	-0.5	3.6	V
Vo	Output voltage range <sup>(2)</sup>		-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>1</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
I <sub>O</sub>	Continuous output current			±20	mA
	Continuous current through $V_{CC}$ or GND			±100	mA
		DCT package		220	
$\theta_{JA}$	Package thermal impedance <sup>(3)</sup>	DCU package		227	°C/W
		YZP package		102	
T <sub>stg</sub>	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

# **Recommended Operating Conditions**<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		0.8	2.7	V
		V <sub>CC</sub> = 0.8 V	V <sub>CC</sub>		
V <sub>IH</sub>	High-level input voltage	$V_{CC} = 1.1 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		V
		$V_{CC}$ = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 0.8 V		0	
VIL	Low-level input voltage	V <sub>CC</sub> = 1.1 V to 1.95 V	0	$0.35 \times V_{CC}$	V
		$V_{CC}$ = 2.3 V to 2.7 V		0.7	
VI	Input voltage		0	3.6	V
Vo	Output voltage		0	V <sub>CC</sub>	V
		V <sub>CC</sub> = 0.8 V		-0.7	
		V <sub>CC</sub> = 1.1 V		-3	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.4 V		-5	mA
		V <sub>CC</sub> = 1.65 V		-8	
		V <sub>CC</sub> = 2.3 V		-9	
		V <sub>CC</sub> = 0.8 V		0.7	
		V <sub>CC</sub> = 1.1 V		3	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.4 V		5	mA
		V <sub>CC</sub> = 1.65 V		8	
		V <sub>CC</sub> = 2.3 V		9	
$\Delta t / \Delta v$	Input transition rise or fall rate			20	ns/V
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## **Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN TYP	<sup>(1)</sup> MAX	UNIT
		I <sub>OH</sub> = -100 μA	0.8 V to 2.7 V	$V_{CC} - 0.1$		
		I <sub>OH</sub> = -0.7 mA	0.8 V	0.	55	
V		$I_{OH} = -3 \text{ mA}$	1.1 V	0.8		V
V <sub>OH</sub>		$I_{OH} = -5 \text{ mA}$	1.4 V	1		v
		$I_{OH} = -8 \text{ mA}$	1.65 V	1.2		
		$I_{OH} = -9 \text{ mA}$	2.3 V	1.8		
		I <sub>OL</sub> = 100 μA	0.8 V to 2.7 V		0.2	
		I <sub>OL</sub> = 0.7 mA	0.8 V	0.	25	
V		I <sub>OL</sub> = 3 mA	1.1 V		0.3	V
V <sub>OL</sub>		I <sub>OL</sub> = 5 mA	1.4 V		0.4	v
		I <sub>OL</sub> = 8 mA	1.65 V		0.45	
		I <sub>OL</sub> = 9 mA	2.3 V		0.6	
I <sub>I</sub>	A or B inputs	$V_I = V_{CC}$ or GND	0 to 2.7 V		±5	μA
I <sub>off</sub>		$V_1 \text{ or } V_0 = 2.7 \text{ V}$	 0		±10	μA
I <sub>CC</sub>		$V_{I} = V_{CC} \text{ or } GND, \qquad I_{O} = 0$	0.8 V to 2.7 V		10	μA
Ci		$V_{I} = V_{CC}$ or GND	2.5 V	:	2.5	pF

(1) All typical values are at  $T_A = 25^{\circ}C$ .

# SN74AUC2G00 DUAL 2-INPUT POSITIVE-NAND GATE

SCES440C-MAY 2003-REVISED JANUARY 2007

### **Switching Characteristics**

over recommended operating free-air temperature range,  $C_L = 15 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 0.8 V	$V_{CC}$ = 1.2 V ± 0.1 V		$V_{CC}$ = 1.5 V ± 0.1 V		V <sub>CC</sub> = 1.8 V ± 0.15 V			$V_{CC}$ = 2.5 V ± 0.2 V		UNIT
	(INFOT)	(001201)	TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Y	8	1	2.5	0.8	1.6	0.6	0.9	1.2	0.5	1	ns

# **Switching Characteristics**

over recommended operating free-air temperature range,  $C_L = 30 \text{ pF}$  (unless otherwise noted) (see Figure 1)

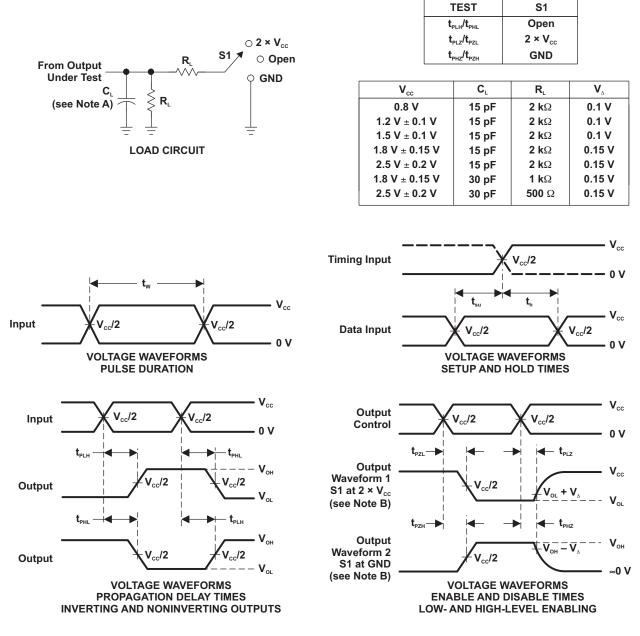
PARAMETER	TER FROM (INPUT)	TO (OUTPUT)		c = 1.8 0.15 \		$\begin{array}{c} V_{CC} \texttt{= 2.5 V} \\ \pm \ \texttt{0.2 V} \end{array}$		UNIT
		(001201)	MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Y	1.2	1.6	2.1	1	1.7	ns

# **Operating Characteristics**

 $T_A = 25^{\circ}C$ 

	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 0.8 V TYP	V <sub>CC</sub> = 1.2 V TYP	V <sub>CC</sub> = 1.5 V TYP	V <sub>CC</sub> = 1.8 V TYP	V <sub>CC</sub> = 2.5 V TYP	UNIT
$\mathbf{C}_{pd}$	Power dissipation capacitance	f = 10 MHz	12	12	12	12	13	pF

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_{L}$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control. C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>o</sub> = 50 Ω,
- slew rate  $\geq$  1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{_{PLZ}}$  and  $t_{_{PHZ}}$  are the same as  $t_{_{dis}}$ .
- F.  $t_{\mbox{\tiny PZL}}$  and  $t_{\mbox{\tiny PZH}}$  are the same as  $t_{\mbox{\tiny en}}.$
- G.  $t_{PIH}$  and  $t_{PHI}$  are the same as  $t_{od}$ .

#### Figure 1. Load Circuit and Voltage Waveforms

### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74AUC2G00DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G00DCTRE4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G00DCTRG4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G00DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G00DCURE4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G00DCURG4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G00YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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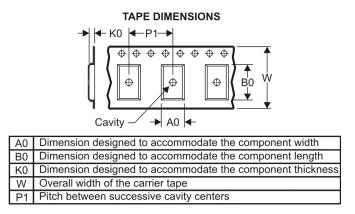
# PACKAGE MATERIALS INFORMATION

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# TAPE AND REEL INFORMATION





## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC2G00DCUR	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G00YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1

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# PACKAGE MATERIALS INFORMATION

6-May-2011



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC2G00DCUR	US8	DCU	8	3000	202.0	201.0	28.0
SN74AUC2G00YZPR	DSBGA	YZP	8	3000	220.0	220.0	34.0

# **MECHANICAL DATA**

MPDS049B - MAY 1999 - REVISED OCTOBER 2002

### DCT (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion

D. Falls within JEDEC MO-187 variation DA.



DCT (R-PDSO-G8) PLASTIC SMALL OUTLINE Example Board Layout Example Stencil Design (Note C,E) (Note D) - 6x0,65 - 6x0,65 8x0,25-8x1,55 3,40 3,40 Non Solder Mask Defined Pad Example Pad Geometry -0,30 (Note C) 1,60 Example -0,07 Non-solder Mask Opening All Around (Note E) 4212201/A 10/11

NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

D. Falls within JEDEC MO-187 variation CA.



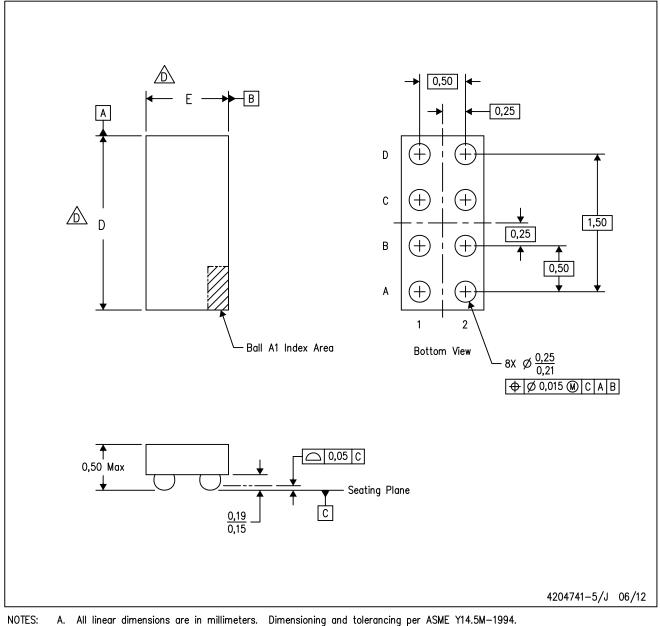


- NOTES: A. All linear dimensions are in millimeters. В. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
  E. This package is a Pb-free solder ball design. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

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