SDAS191A - APRIL 1982 - REVISED DECEMBER 1994

 Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

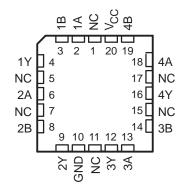
These devices contain four independent 2-input positive-AND gates. They perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The SN54ALS08 and SN54AS08 are characterized for operation over the full military temperature range of -55° C to 125° C. The SN74ALS08 and SN74AS08 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)											
INPUTS OUTPUT											
Α	В	Y									
Н	Н	Н									
L	Х	L									
Х	L	L									

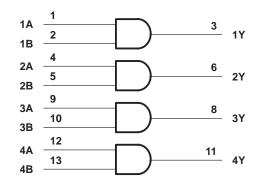
SN54ALS08, SN54AS08 . . . J PACKAGE SN74ALS08, SN74AS08 . . . D OR N PACKAGE (TOP VIEW)

SN54ALS08, SN54AS08 . . . FK PACKAGE (TOP VIEW)

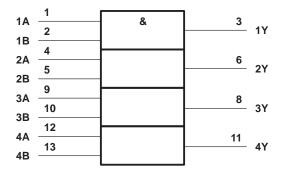


NC - No internal connection

logic diagram (positive logic)



logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, and N packages.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{CC} Input voltage, V _I		
Operating free-air temperature range, TA:	SN54ALS08	 –55°C to 125°C
	SN74ALS08	 0°C to 70°C
Storage temperature range		 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS08)8	SN			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
	Level Second Second and the sec			0.8‡			0.8	V
VIL	Low-level input voltage			0.7§				V
ЮН	High-level output current			-0.4			-0.4	mA
IOL	Low-level output current			4			8	mA
TA	Operating free-air temperature	-55		125	0		70	°C

[‡] Applies over temperature range – 55°C to 70°C

§ Applies over temperature range 70°C to 125°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			SN	154ALSC)8	SN	74ALS	8	
PARAMETER	TEST CONDITIONS			TYP¶	MAX	MIN	TYP¶	MAX	UNIT
VIK	$V_{CC} = 4.5 V,$	I _I = -18 mA			-1.5			-1.5	V
V _{OH}	$V_{CC} = 4.5 V \text{ to } 5.5 V,$	I _{OH} = -0.4 mA	V _{CC} -2	2		V _{CC} -2	2		V
Max		$I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	
VOL	$V_{CC} = 4.5 V$	$I_{OL} = 8 \text{ mA}$					0.35	0.5	V
l	$V_{CC} = 5.5 V,$	$V_{I} = 7 V$			0.1			0.1	mA
Ιн	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μA
١ _{١L}	V _{CC} = 5.5 V,	V _I = 0.4 V			-0.1			-0.1	mA
IO#	V _{CC} = 5.5 V,	V _O = 2.25 V	-20		-112	-30		-112	mA
ІССН	V _{CC} = 5.5 V,	V _I = 4.5 V		1.3	2.4		1.3	2.4	mA
ICCL	V _{CC} = 5.5 V,	$V_{I} = 0$		2.2	4		2.2	4	mA

¶ All typical values are at V_{CC} = 5 V, T_A = 25° C.

The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.



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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	то (оитрит)	CL RL	= 50 pF = 500 Ω = MIN t			UNIT
			MIN	MAX	MIN	MAX	
^t PLH	A or B	V	2	14	4	14	
^t PHL	AUB	ī	2	12.5	3	10	ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, V _{CC} Input voltage, V _I	
Operating free-air temperature range, T _A : SN54AS08	
SN74AS08	0°C to 70°C
Storage temperature range	–65°C to 150°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS08			S	UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
IOH	High-level output current			-2			-2	mA
IOL	Low-level output current			20			20	mA
TA	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	7507.0	TEST CONDITIONS				S	8		
PARAMETER	TEST C	MIN	TYP§	MAX	MIN	TYP§	MAX	UNIT	
VIK	V _{CC} = 4.5 V,	lı = -18 mA			-1.2			-1.2	V
VOH	$V_{CC} = 4.5 V \text{ to } 5.5 V,$	$I_{OH} = -2 \text{ mA}$	V _{CC} -2)		V _{CC} -2	2		V
VOL	$V_{CC} = 4.5 V,$	I _{OL} = 20 mA		0.35	0.5		0.35	0.5	V
lį	V _{CC} = 5.5 V,	$V_{I} = 7 V$			0.1			0.1	mA
IIН	V _{CC} = 5.5 V,	V _I = 2.7 V			20			20	μΑ
١ _{١L}	$V_{CC} = 5.5 V,$	$V_{I} = 0.4 V$			-0.5			-0.5	mA
۱ ₀ ¶	V _{CC} = 5.5 V,	V _O = 2.25 V	-30		-112	-30		-112	mA
Іссн	V _{CC} = 5.5 V,	VI = 4.5 V		5.8	9.3		5.8	9.3	mA
ICCL	V _{CC} = 5.5 V,	$V_{I} = 0$		14.9	24		14.9	24	mA

§ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, IOS.

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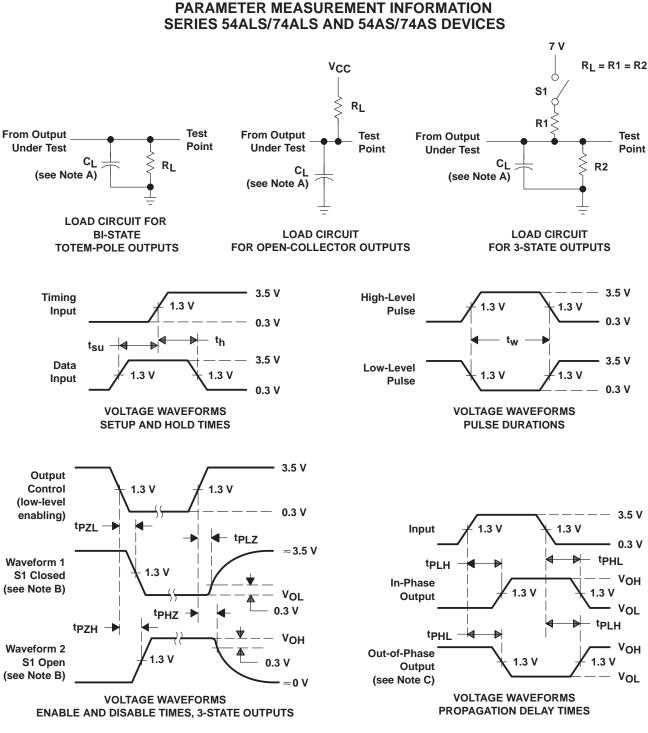
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	то (оитрит)	VC CL RL TA SN54	UNIT			
			MIN	MAX	SN74/ MIN	MAX	
^t PLH	A or B	V	1	6.5	1	5.5	
^t PHL	AUID	T	1	6.5	1	5.5	ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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NOTES: A. CL includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: PRR \leq 1 MHz, t_r = t_f = 2 ns, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-86842012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8684201CA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Call TI	
5962-8684201DA	ACTIVE	CFP	W	14	1	TBD	Call TI	Call TI	
JM38510/37401B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
JM38510/37401BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
M38510/37401B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
M38510/37401BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN54ALS08J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN54AS08J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN74ALS08D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS08DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS08DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS08DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS08DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS08DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS08N	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS08N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN74ALS08NE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74ALS08NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS08NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74ALS08NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS08D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	



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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74AS08DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS08DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS08DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS08DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS08DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS08N	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AS08N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN74AS08NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74AS08NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS08NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74AS08NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54ALS08FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54ALS08J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SNJ54ALS08W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
SNJ54AS08FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54AS08J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SNJ54AS08W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

PACKAGE OPTION ADDENDUM



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25-Jan-2012

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and pa

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54ALS08, SN54AS08, SN74ALS08, SN74AS08 :

• Catalog: SN74ALS08, SN74AS08

• Military: SN54ALS08, SN54AS08

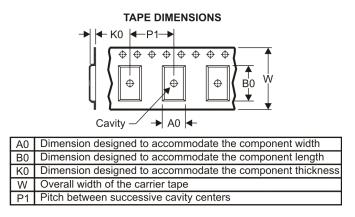
NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All dimensions are nominal Device	Package	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS08DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ALS08NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AS08DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AS08NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1



PACKAGE MATERIALS INFORMATION

11-Mar-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS08DR	SOIC	D	14	2500	346.0	346.0	33.0
SN74ALS08NSR	SO	NS	14	2000	346.0	346.0	33.0
SN74AS08DR	SOIC	D	14	2500	346.0	346.0	33.0
SN74AS08NSR	SO	NS	14	2000	346.0	346.0	33.0

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB



LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N**) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a metal lid.

D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.





NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0-10 Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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